

COMPAQ

***Technical
Reference
Guide***

For

Compaq Deskpro Personal Computers

Covering Models Featuring

Intel Celeron and Pentium III Processors

and

Intel 810, 810e, and 820 Chipsets



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COMPAQ Deskpro Personal Computers
Featuring Intel Celeron and Pentium III Processors
and Intel 810, 810e, and 820 Chipsets

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Chapter 1

INTRODUCTION

1.1 ABOUT THIS GUIDE

This guide provides technical information about Compaq Deskpro EP, Compaq Deskpro EN Small Form Factor (SFF), Desktop (DT), Minitower (MT), and Compaq Deskpro Workstation AP240 RAMBUS and AP250 Series of Personal Computers featuring Intel Celeron or Pentium III processor and using the Intel 810, 810e, or 820 chipset. This document includes information regarding system design, function, and features that can be used by programmers, engineers, technicians, and system administrators.

This guide and any applicable addendums are available online at the following location:

http://www.compaq.com/support/techpubs/technical_reference_guides/index.html

1.1.1 USING THIS GUIDE

The chapters of this guide primarily describe the hardware and firmware elements and primarily deal with the system board and the power supply assembly. The appendices contain general information about standard peripheral devices such as the keyboard as well as any AGP or PCI expansion cards.

1.1.2 ADDITIONAL INFORMATION SOURCES

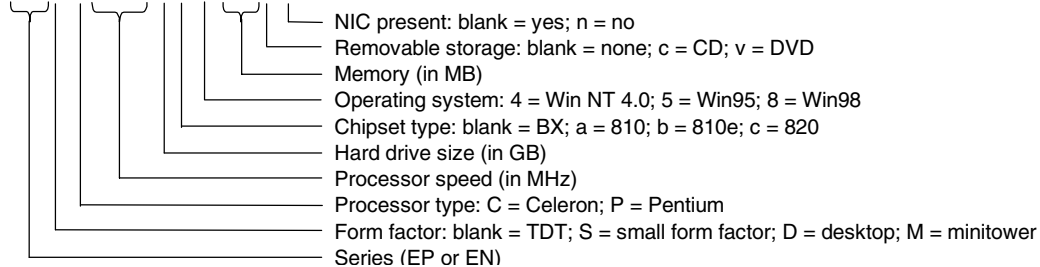
For more information on chipset components mentioned in this guide refer to the indicated manufacturers' documentation, which may be available at the following online sources:

- ◆ Compaq Computer Corporation: <http://www.compaq.com>
- ◆ Intel Corporation: <http://www.intel.com>
- ◆ National Semiconductor Incorporated: <http://www.national.com>
- ◆ Matrox Incorporated: <http://www.matrox.com>

1.2 MODEL NUMBERING CONVENTION

The model numbering convention for Compaq Deskpros is as follows:

XXX/XNNN/Nx/N/NNx/x



1.3 NOTATIONAL CONVENTIONS

1.3.1 VALUES

Hexadecimal values are indicated by a numerical or alpha-numerical value followed by the letter “h.” Binary values are indicated by a value of ones and zeros followed by the letter “b.” Numerical values that have no succeeding letter can be assumed to be decimal.

1.3.2 RANGES

Ranges or limits for a parameter are shown using the following methods:

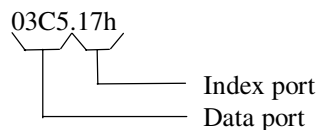
Example A: Bits <7..4> = bits 7, 6, 5, and 4.
Example B: IRQ3-7, 9 = IRQ signals 3 through 7, and IRQ signal 9

1.3.3 SIGNAL LABELS

Signal names are indicated using abbreviations, acronyms, or, if possible, the full signal name in all capital letters. Signals that are meant to be active (asserted) low are indicated with a dash immediately following the name.

1.3.4 REGISTER NOTATION AND USAGE

This guide uses standard Intel naming conventions in discussing the microprocessor’s (CPU) internal registers. Registers that are accessed through programmable I/O using an indexing scheme are indicated using the following format:



In the example above, register 03C5.17h is accessed by writing the index port value 17h to the index address (03C4h), followed by a write to or a read from port 03C5h.

1.3.5 BIT NOTATION

Bit values are labeled with bit <0> representing the least-significant bit (LSb) and bit <7> representing the most-significant bit (MSb) of a byte. Bytes, words, double words, and quad words are typically shown with most-significant portions on the left or top and the least-significant portions on the right or bottom respectively.

1.4 COMMON ACRONYMS AND ABBREVIATIONS

Table 1-1 lists the acronyms and abbreviations used in this guide.

Table 1-1.
Acronyms and Abbreviations

Acronym/Abbreviation	Description
A	ampere
AC	alternating current
ACPI	Advanced Configuration and Power Interface
A/D	analog-to-digital
AGP	Accelerated graphics port
API	application programming interface
APM	advanced power management
AOL	Alert-ON-LAN
ASIC	application-specific integrated circuit
AT	1. attention (commands) 2. 286-based PC architecture
ATA	AT attachment (mode)
AVI	audio-video interleaved
AVGA	Advanced VGA
BCD	binary-coded decimal
BIOS	basic input/output system
bis	second/new revision
BitBLT	bit block transfer
BNC	Bayonet Neill-Concelman (connector)
bps or b/s	bits per second
BSP	Bootstrap processor
BTO	Built to order
CAS	column address strobe
CD	compact disk
CD-ROM	compact disk read-only memory
CDS	compact disk system
CF	carry flag
CGA	color graphics adapter
Ch	channel
CLUT	color look-up table (palette)
cm	centimeter
CMC	cache/memory controller
CMOS	complimentary metal-oxide semiconductor (configuration memory)
Cntrl	controller
Cntrl	control
codec	compressor/decompressor
CPQ	Compaq
CPU	central processing unit
CRT	cathode ray tube
CSM	Compaq system management / Compaq server management
CTO	Configure to order
DAA	direct access arrangement
DAC	digital-to-analog converter
db	decibel
DC	direct current
DCH	DOS compatibility hole
DDC	Display Data Channel
DF	direction flag

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
DIMM	dual inline memory module
DIN	Deutsche IndustriNorm (connector standard)
DIP	dual inline package
DMA	direct memory access
DMI	Desktop management interface
dpi	dots per inch
DRAM	dynamic random access memory
DRQ	data request
EDID	extended display identification data
EDO	extended data out (RAM type)
EEPROM	electrically eraseable PROM
EGA	enhanced graphics adapter
EIA	Electronic Industry Association
EISA	extended ISA
EPP	enhanced parallel port
EIDE	enhanced IDE
ESCD	Extended System Configuration Data (format)
EV	Environmental Variable (data)
ExCA	Exchangeable Card Architecture
FIFO	first in / first out
FL	flag (register)
FM	frequency modulation
FPM	fast page mode (RAM type)
FPU	Floating point unit (numeric or math coprocessor)
FPS	Frames per second
ft	foot
GB	gigabyte
GMCH	Graphics/memory controller hub
GND	ground
GPIO	general purpose I/O
GPOC	general purpose open-collector
GART	Graphics address re-mapping table
GUI	graphics user interface
h	hexadecimal
HW	hardware
hex	hexadecimal
Hz	hertz
ICH	I/O controller hub
IDE	integrated drive element
IEEE	Institute of Electrical and Electronic Engineers
IF	interrupt flag
I/F	interface
in	inch
INT	interrupt
I/O	input/output
IPL	initial program loader
IrDA	InfraRed Data Association
IRQ	interrupt request
ISA	industry standard architecture
JEDEC	Joint Electron Device Engineering Council
Kb / KB	kilobits / kilobytes (x 1024 bits / x 1024 bytes)
Kb/s	kilobits per second
kg	kilogram
KHz	kilohertz
kV	kilovolt

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
lb	pound
LAN	local area network
LCD	liquid crystal display
LED	light-emitting diode
LIF	low insertion force (socket)
LPC	Low pin count
LSI	large scale integration
LSb / LSB	least significant bit / least significant byte
LUN	logical unit (SCSI)
MCH	Memory controller hub
MMX	multimedia extensions
MPEG	Motion Picture Experts Group
ms	millisecond
MSb / MSB	most significant bit / most significant byte
mux	multiplex
MVA	motion video acceleration
MVW	motion video window
<i>n</i>	variable parameter/value
NIC	network interface card/controller
NiCad	nickel cadmium
NiMH	nickel-metal hydride
NMI	non-maskable interrupt
ns	nanosecond
NT	nested task flag
NTSC	National Television Standards Committee
NVRAM	non-volatile random access memory
OEM	original equipment manufacturer
OS	operating system
PAL	1. programmable array logic 2. phase altering line
PC	personal computer
PCI	peripheral component interconnect
PCM	pulse code modulation
PCMCIA	Personal Computer Memory Card International Association
PF	parity flag
PIN	personal identification number
PIO	Programmed I/O
POST	power-on self test
PROM	programmable read-only memory
PTR	pointer
RAM	random access memory
RAS	row address strobe
rcvr	receiver
RF	resume flag
RGB	red/green/blue (monitor input)
RH	Relative humidity
RIMM	RDRAM inline memory module
RMS	root mean square
ROM	read-only memory
RPM	revolutions per minute
RTC	real time clock
R/W	read/write

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
SCSI	small computer system interface
SDRAM	Synchronous Dynamic RAM
SEC	Single Edge-Connector
SECAM	sequential colour avec memoire (sequential color with memory)
SF	sign flag
SGRAM	Synchronous Graphics RAM
SIMD	Single instruction multiple data
SIMM	single in-line memory module
SIT	system information table
SMART	Self Monitor Analysis Report Technology
SMI	system management interrupt
SMM	system management mode
SMRAM	system management RAM
SPD	serial presence detect
SPP	standard parallel port
SRAM	static RAM
SSE	Streaming SIMD extensions
STN	super twist pneumatic
SVGA	super VGA
SW	software
TAD	telephone answering device
TAFI	Temperature-sensing And Fan control Integrated circuit
TAM	telephone answering machine
TCP	tape carrier package
TF	trap flag
TFT	thin-film transistor
TIA	Telecommunications Information Administration
TPE	twisted pair ethernet
TPI	track per inch
TTL	transistor-transistor logic
TV	television
TX	transmit
UART	universal asynchronous receiver/transmitter
UDMA	Ultra DMA
URL	Uniform resource locator
us / μ s	microsecond
USB	Universal Serial Bus
UTP	unshielded twisted pair
V	volt
VESA	Video Electronic Standards Association
VGA	video graphics adapter
vib	vibrato
VLSI	very large scale integration
VRAM	Video RAM
W	watt
WOL	Wake on LAN
WRAM	Windows RAM
ZF	zero flag
ZIF	zero insertion force (socket)

Chapter 2 SYSTEM OVERVIEW

2.1 INTRODUCTION

Compaq Deskpro Personal Computers (Figure 2-1) deliver an outstanding combination of manageability, serviceability, and consistency for enterprise environments. Based on Intel Celeron and Pentium III processors with the Intel 810, 810e, and 820 chipsets, these systems emphasize performance along with industry compatibility. These models feature architectures incorporating the PCI and ISA buses. All models are easily upgradable and expandable to keep pace with the needs of the office enterprise.



Compaq Deskpro EP



Compaq Deskpro EN Small Form Factor



Compaq Deskpro EN or
Compaq Deskpro Workstation AP240 RAMBUS
Desktop and Minitower



Compaq Deskpro Workstation AP250

Figure 2-1. Compaq Deskpro Personal Computers with Monitors

This chapter includes the following topics:

- ◆ Features and options (2.2) page 2-2
- ◆ Mechanical design (2.3) page 2-4
- ◆ System architecture (2.4) page 2-8
- ◆ Specifications (2.5) page 2-13

2.2 FEATURES AND OPTIONS

This section describes the standard features and available options.

2.2.1 STANDARD FEATURES

The following standard features are available on models of all series:

- ◆ Two sockets for system memory
- ◆ AC'97 audio subsystem with Compaq Premier Sound
- ◆ 3.5 inch, 1.44-MB diskette drive
- ◆ CD-ROM drive
- ◆ Extended IDE controller supporting UATA/66 mode for up to four drives
- ◆ Hard drive fault prediction
- ◆ Two serial interfaces
- ◆ Parallel interface
- ◆ APM 1.2 power management support
- ◆ Plug 'n Play compatible (with ESCD support)
- ◆ Intelligent Manageability support
- ◆ Energy Star compliant
- ◆ Security features including:
 - Flash ROM Boot Block
 - Diskette drive disable, boot disable, write protect
 - Power-on password
 - Administrator password
 - Serial/parallel port disable
- ◆ Compaq Enhanced keyboard w/Windows support
- ◆ Mouse

Table 2-1 shows the differences in features between the Deskpro series':

Table 2-1.
Feature Difference Matrix

Deskpro Series	EP	EN SFF	EN or Workstation AP240		Workstation AP250
Form factor	[1]	Low profile-DT	DT	MT	[1]
Chassis type	ATX	proprietary	NLX	NLX	ATX
Chipset	810 or 810e	810, 810e, or 820	[2]	[2]	820
Front panel audio access	No	Yes	No	No	No
Smart Cover Lock/Sensor	No	Yes	Yes	Yes	No
NIC on system board	No	Yes	No	No	No
No. of dedicated ISA slots	1	0	0	2	1
No. of combo PCI/ISA slots	1	1	2	0	1
No. of dedicated PCI slots	4	1	2	5	4

NOTES:

[1] System unit may be configured as desktop or minitower (i.e., "towerable" desktop).

[2] EN system may be 810- or 820-based. Workstation AP240 RAMBUS system 820-based only.

2.2.2 OPTIONS

The following items are available as options for all models and may be included in the standard configuration of some models:

- ◆ System Memory: 16-MB DIMM (non-ECC)
32-MB DIMM (non-ECC)
64-MB DIMM (non-ECC) or RIMM (ECC and non-ECC)
128-MB DIMM (non-ECC) or RIMM (ECC and non-ECC)
256-MB DIMM (non-ECC) or RIMM (ECC and non-ECC)
- ◆ Hard drives/controllers: 20, 22, or 27 GB UATA/66 hard drive
9.1 GB Wide Ultra SCSI hard drive
18.2 GB Ultra3 SCSI hard drive
Wide Ultra SCSI PCI controller
- ◆ Removeable media drives: 32x Max Tray Load CD-ROM drive
40x Max Tray Load CD-ROM drive
PS-120 Power Drive
10x/40x DVD-ROM
6x Slimline DVD-ROM
2x/4x/24x CD-RW drive
52x TrueX CD-ROM drive
PCI Dxr3 DVD Decoder Card
- ◆ Communications cards: Intel PRO/100+ Management Adapter
3COM (3C905C-TX) 10/100 PCI NIC
Compaq 56K PCI modem
- ◆ Graphics cards/memory: Matrox Millennium G400 AGP Graphics Controller
Matrox G400 DVI Daughter Card
ELSA Synergy II AGP Graphics Card
3Dlabs Oxygen GVX1 Graphics Card

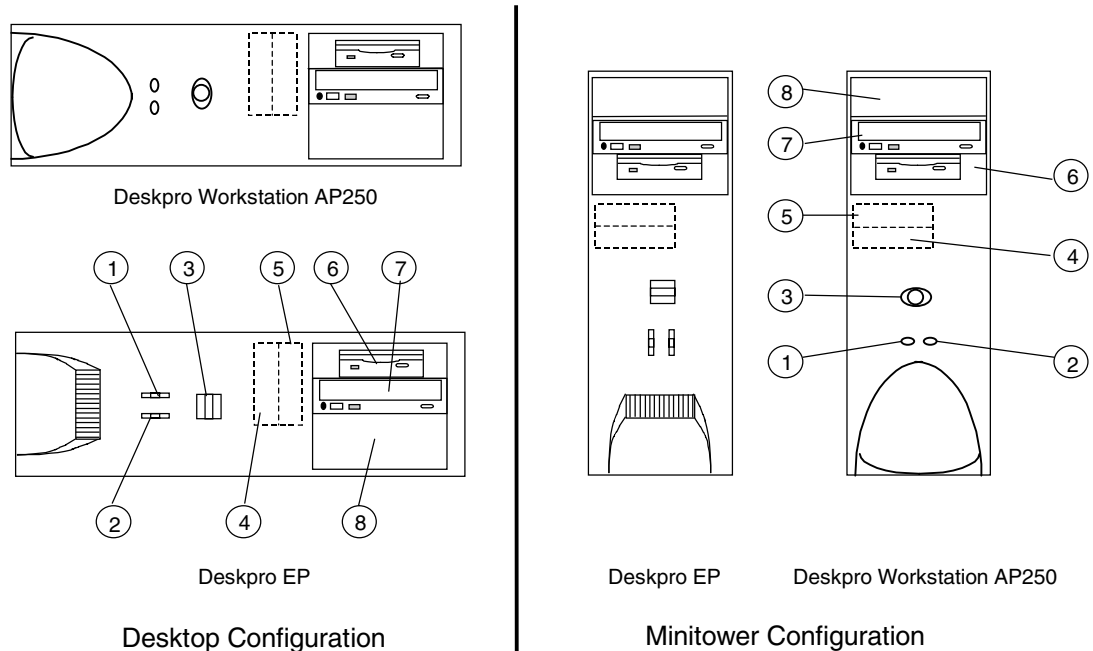
Compaq Deskpro Computers are easily upgraded and enhanced with peripheral devices designed to meet PCI, AGP, and ISA standards. The Compaq Deskpro Personal Computers are compatible with peripherals designed for Plug 'n Play operation.

2.3 MECHANICAL DESIGN

Compaq Deskpros are available in several form factors. The Compaq Deskpro EP and Workstation AP250 Series features an ATX-compatible form factor that may be configured as a desktop or a tower. The Compaq Deskpro EN and Workstation AP240 Series includes two NLX-type form factors, Desktop (DT) and Minitower (MT); and the Deskpro EN Small Form Factor features a space-saving design.

2.3.1 CABINET LAYOUTS

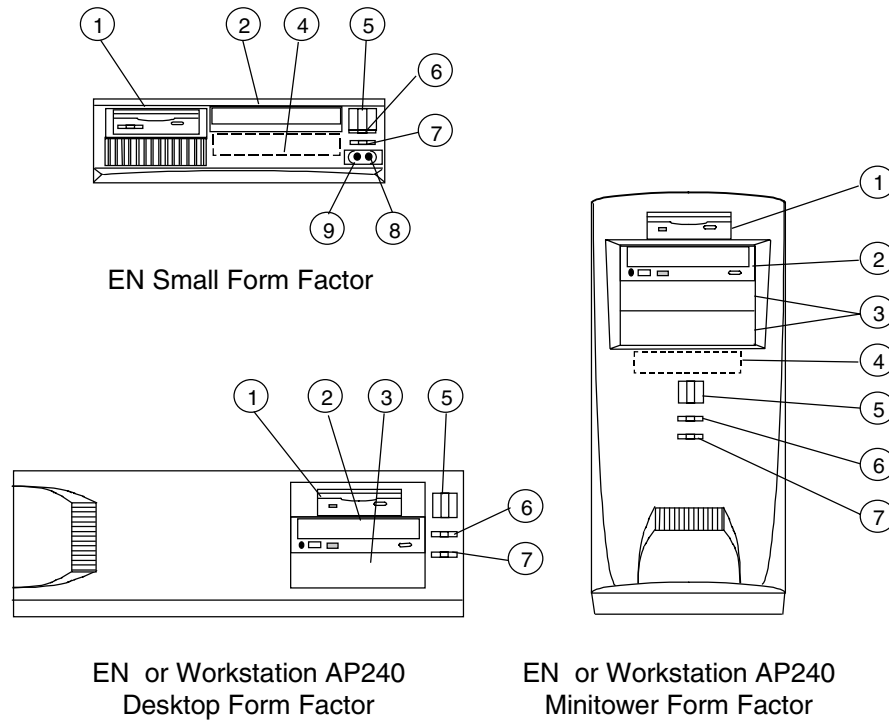
2.3.1.1 Front Views



Item	Description
1	Power On Light
2	Hard Drive Activity Light
3	Power Button
4	3.5" drive bay (1/3 height)
5	Internal Drive in 3.5" drive bay (1/3 height)
6	1.44 MB Diskette Drive in 5.25" drive bay (1/3 height)
7	CD-ROM Drive in 5.25" drive bay (1/3 height)
8	5.25" drive bay (1/2 height)

NOTE: All EP and Workstation AP250 units may be configured as either a desktop or a minitower. Control, indicator, and drivebay locations of the Deskpro Workstation AP250 series are virtually identical with those of the Deskpro EP series.

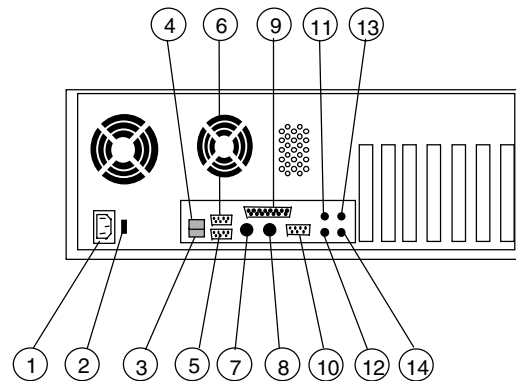
Figure 2-2. Compaq Deskpro EP and Workstation AP250 Series, Front View



Item	Description
1	1.44 MB Diskette Drive (5.25" drive bay)
2	CD-ROM Drive (CDS models) (5.25" drive bay)
3	Internal Drive (5.25") bay
4	Internal Drive (3.5") bay
5	Power Button
6	Power On/Sleep Indicator
7	Hard Drive Activity Indicator
8	Headphone Out Jack
9	Microphone In Jack

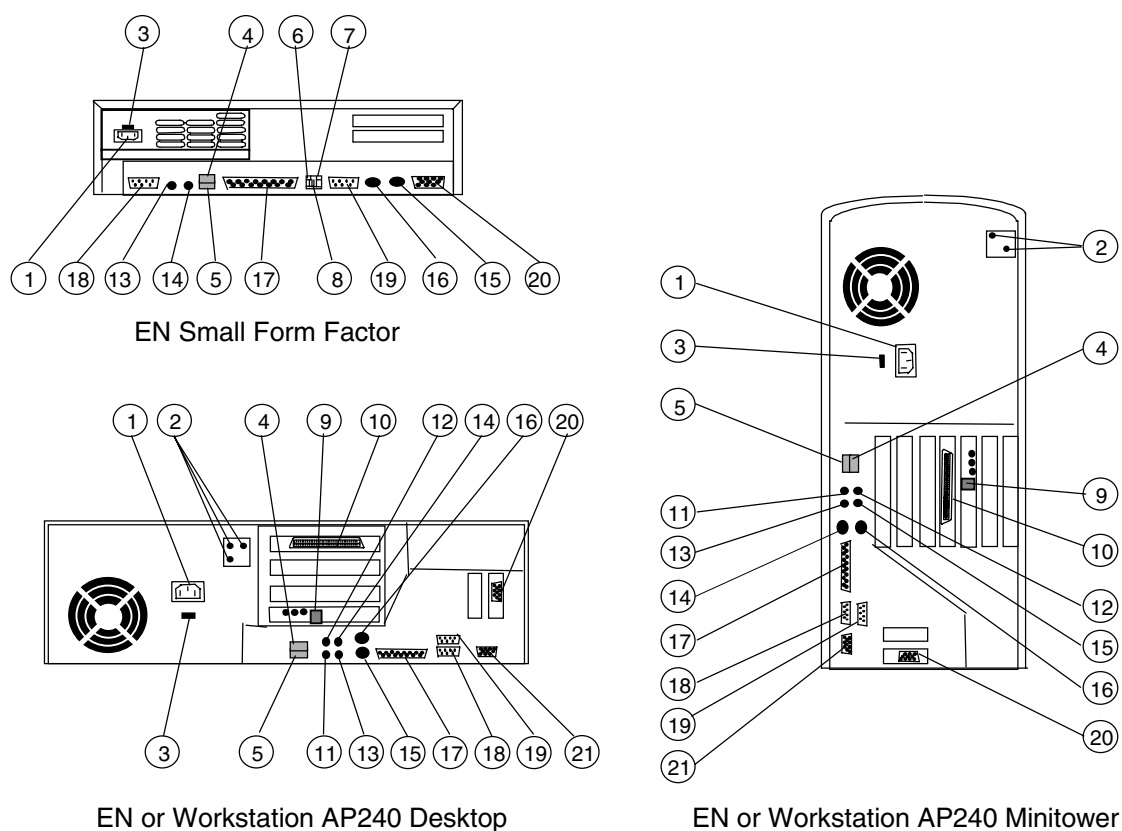
Figure 2-3. Compaq Deskpro EN and Workstation AP240 Series, Front View

2.3.1.2 Rear Views



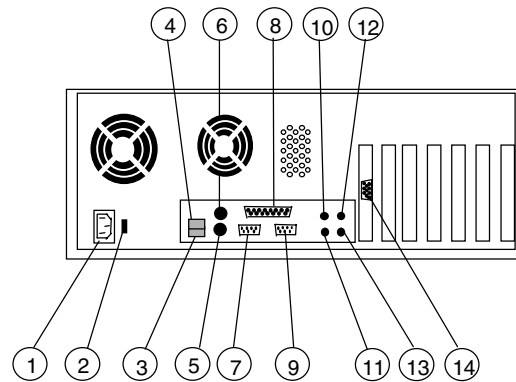
Item	Description
1	AC Line In Connector
2	Line Voltage Select Switch
3	Universal serial bus interface (port A)
4	Universal serial bus interface (port B)
5	Serial interface A (COM1)
6	Serial interface B (COM2)
7	Keyboard connector
8	Mouse connector
9	Parallel interface
10	Monitor connector
11	Microphone input
12	Headphone output
13	Line input
14	Line output

Figure 2–4. Compaq Deskpro EP Series, Rear View



Item	Description
1	AC Line In Connector
2	Smart Cover Lock Screws
3	Line Voltage Switch
4	USB Interface Port B
5	USB Interface Port A
6	100TX speed LED
7	Activity LED
8	Network connector
9	Network interface controller card (some models)
10	SCSI card (some Workstation models only)
11	Audio Headphone Input
12	Audio Microphone Input
13	Audio Line Output
14	Audio Line Input
15	Keyboard Connector
16	Mouse Connector
17	Parallel Interface Connector
18	Serial Interface Connector (COM1)
19	Serial Interface Connector (COM2)
20	Graphics Monitor Connector (820-based systems)
21	Graphics Monitor Connector (810-based systems)

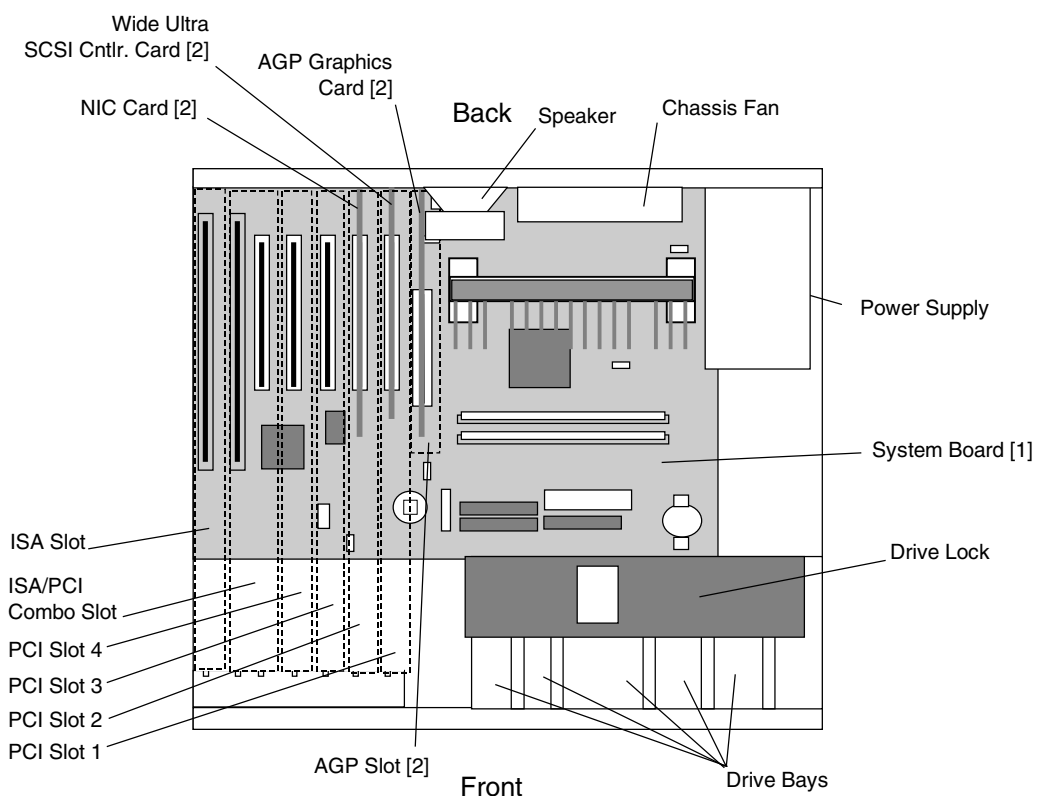
Figure 2-5. Compaq Deskpro EN and Workstations AP240 Series, Rear Views



Item	Description
1	AC Line In Connector
2	Line Voltage Select Switch
3	Universal serial bus interface (port A)
4	Universal serial bus interface (port B)
5	Keyboard connector
6	Mouse connector Serial interface B (COM2)
7	Serial interface A (COM1)
8	Parallel interface
9	Serial interface B (COM2)
10	Microphone input
11	Headphone output
12	Line input
13	Line output
14	Monitor connector

Figure 2–6. Compaq Deskpro Workstation AP250 Series, Rear View

2.3.2 CHASSIS LAYOUTS



NOTES:

- [1] System board of the Deskpro Workstation AP250 series shown.
- [2] Deskpro Workstation AP250 only.

Figure 2–7. Compaq Deskpro EP or Workstation AP250 Chassis Layout, Top View (Desktop Configuration)

For serviceability the Deskpro EN systems feature an expansion card cage that allows easy removal of the backplane and expansion cards as a single assembly. The tilt drive cage tilts up for easy removal/replacement of drives. For detailed information on servicing the chassis refer to the multimedia training CD-ROM and/or the maintenance and service guide for these systems.

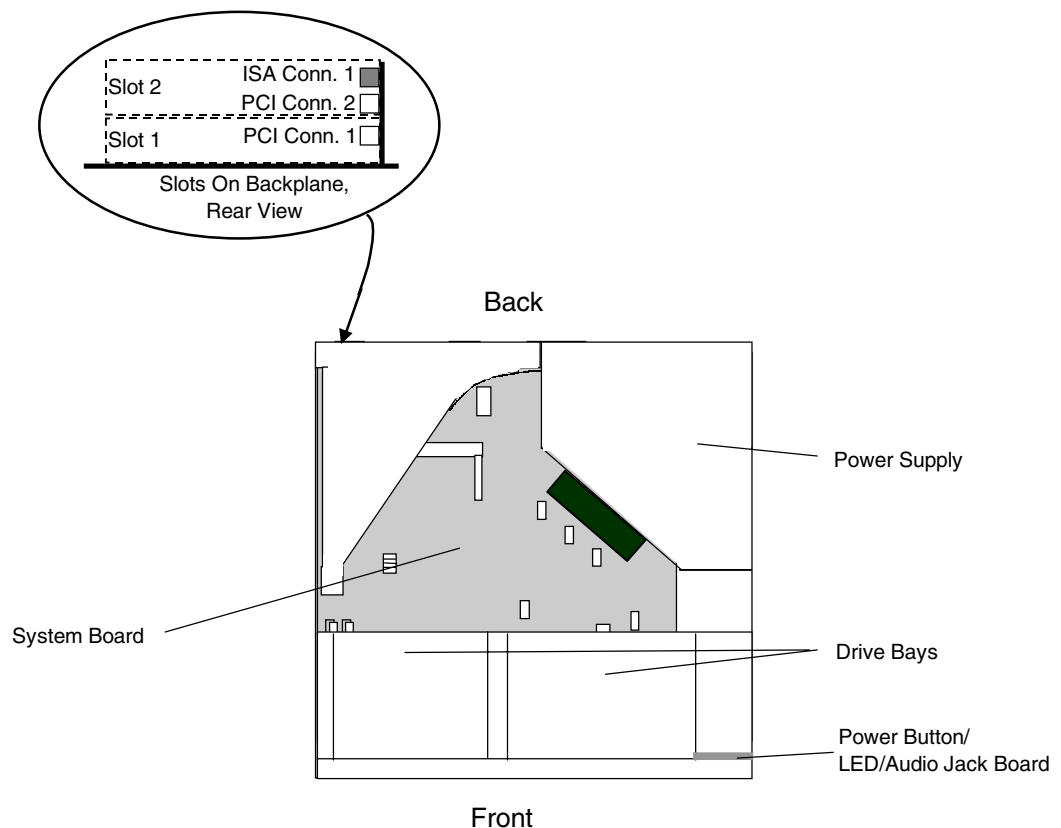
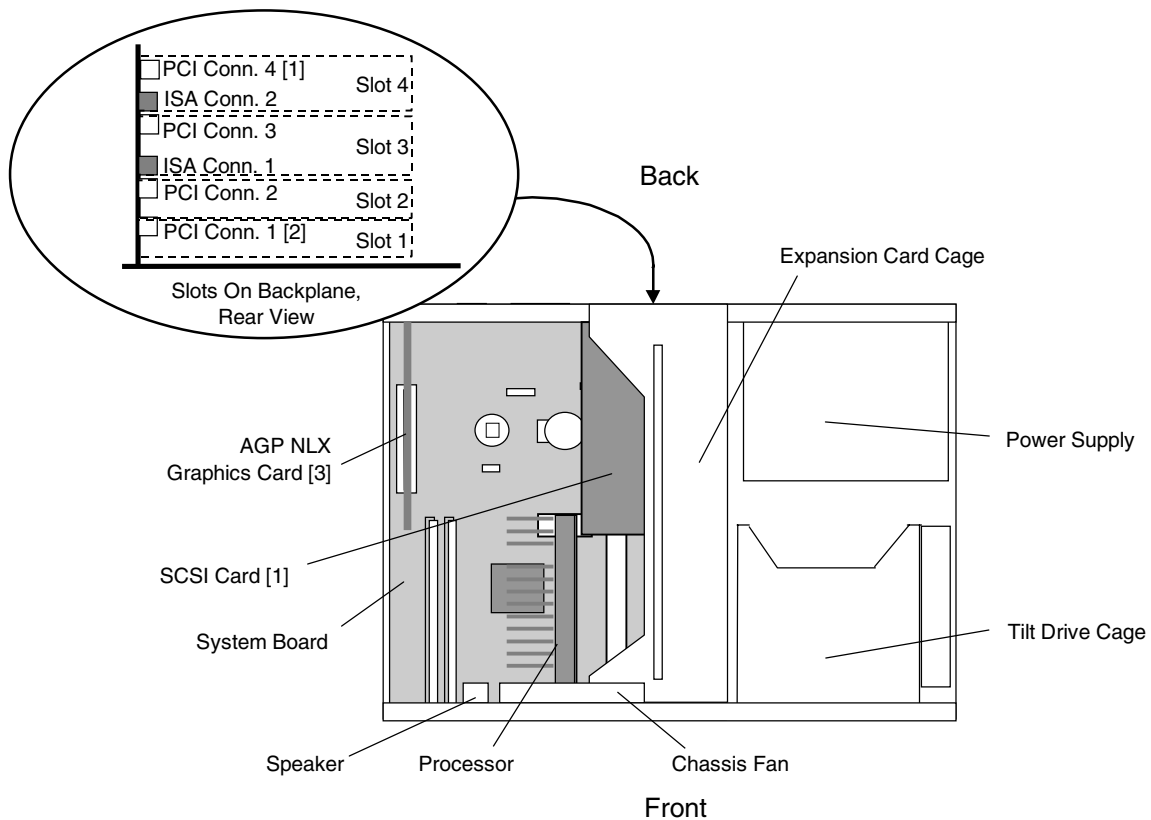


Figure 2-8. Compaq Deskpro EN SFF Chassis Layout, Top View

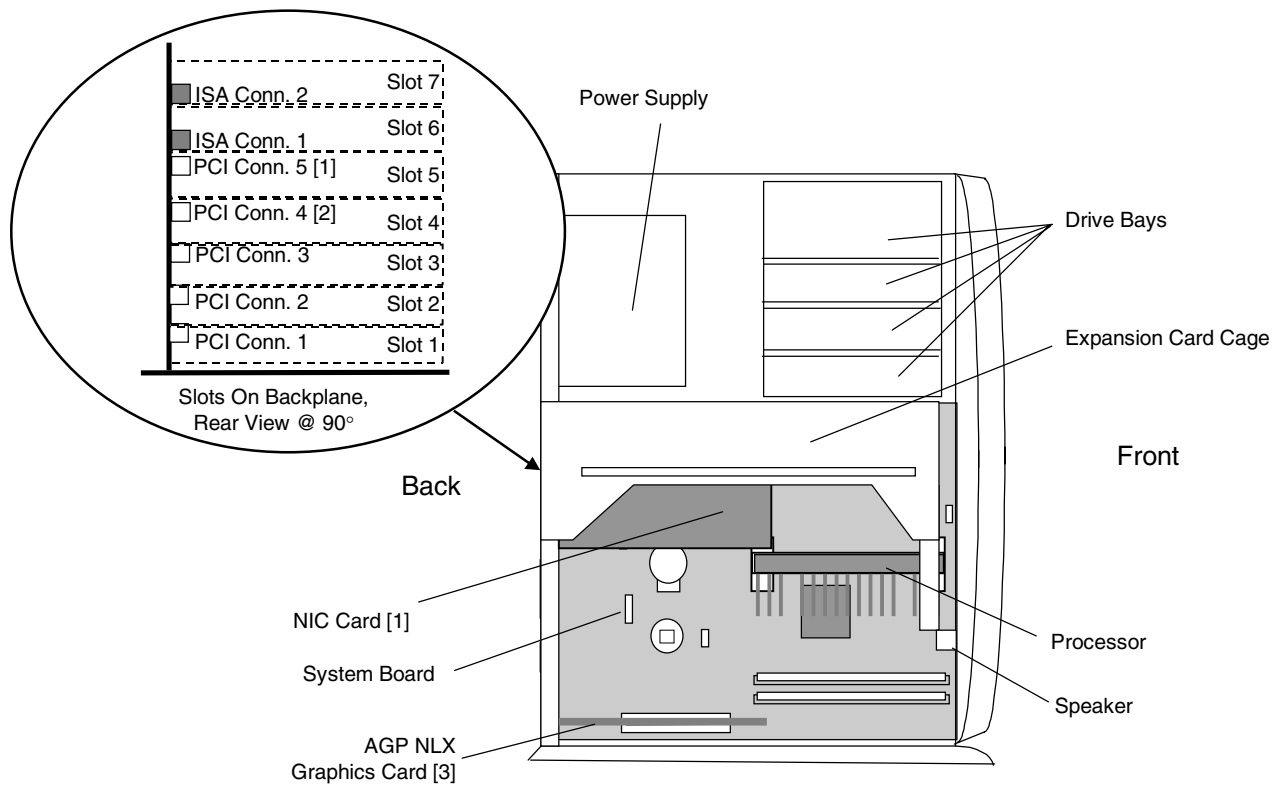
Figures 2-9 and 2-10 show the layout of key assemblies within the desktop and minitower chassis respectively. For serviceability these systems feature an expansion card cage that allows easy removal of the backplane and expansion cards as a single assembly. The desktop form factor also features a drive cage that tilts up for easy access. For detailed information on servicing the chassis refer to the multimedia training CD-ROM and/or the maintenance and service guide for this system.



NOTES:

- [1] Populated by SCSI controller card on some models.
- [2] Populated by network interface controller card on some models.
- [3] 820-based systems only.

Figure 2-9. Compaq Deskpro EN or Workstation AP240 Desktop Chassis Layout, Top View

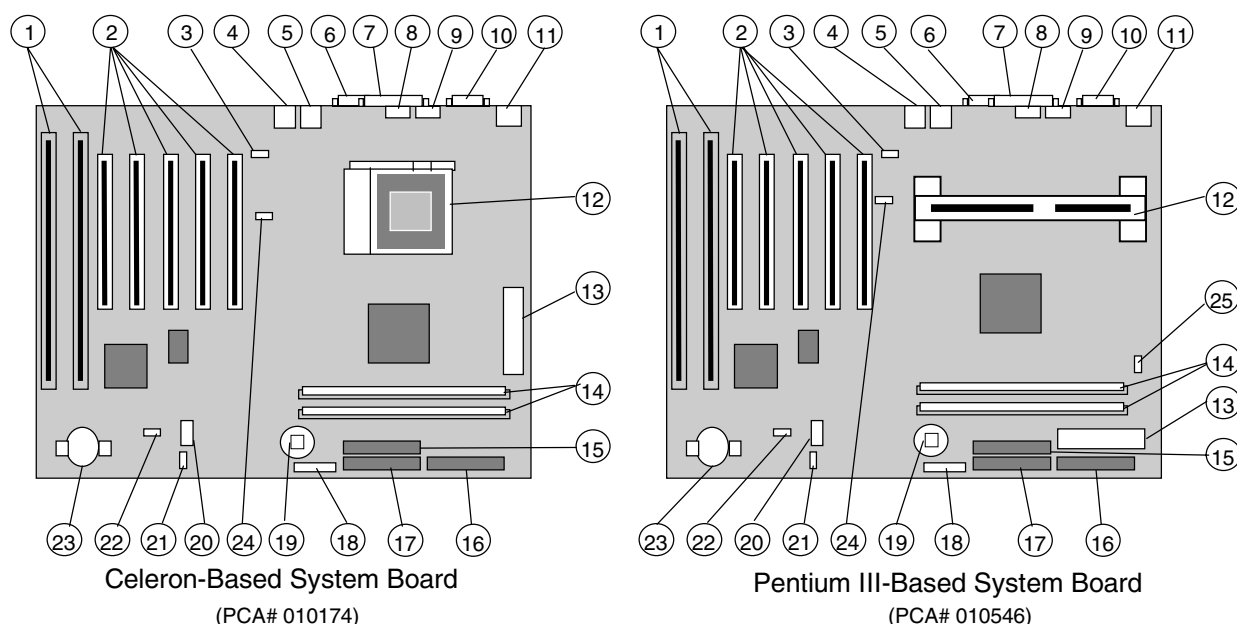


NOTES:

- [1] Populated by network interface controller card on some models.
- [2] Populated by SCSI controller card on some models.
- [3] 820-based systems only.

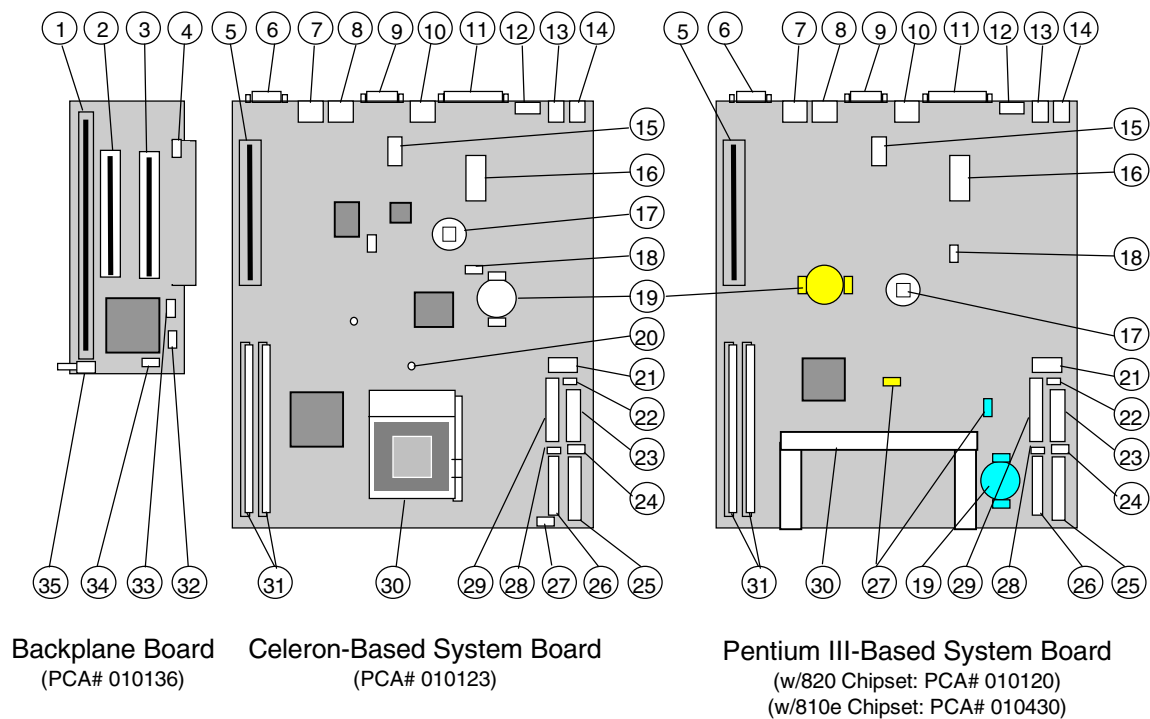
Figure 2-10. Compaq Deskpro EN or Workstation AP240 Minitower Chassis Layout, Left Side View

2.3.3 BOARD LAYOUTS



Item	Description
1	ISA expansion connectors
2	PCI expansion connectors
3	Chassis speaker header
4	Audio line out (bottom), audio line in (top)
5	Audio headphones (bottom), audio microphone (top)
6	Graphics monitor connector
7	Parallel I/F connector
8	Mouse connector
9	Keyboard connector
10	Serial I/F connectors: COM1 (bottom), COM2 (top)
11	Universal serial bus I/F connectors: port A (bottom), port B (top)
12	Processor connector
13	Power supply connector
14	DIMM sockets
15	IDE secondary connector
16	Diskette drive connector
17	IDE primary connector
18	Power switch/LED connector
19	CMOS clear button
20	Alert-On-LAN (AOL) header
21	Wake-on-LAN (WOL) header
22	Password enable jumper
23	RTC/CMOS Battery
24	Chassis fan header
25	Fan header for boxed processor

Figure 2-11. Compaq Deskpro EP System Board Layouts



Item	Description	Item	Description
1	ISA expansion connector (slot 2)	19	CMOS battery
2	PCI expansion connector (slot 2)	20	AUX power LED
3	PCI expansion connector (slot 1)	21	Front panel power/audio connector
4	AOL connector (P12)	22	Speaker connector
5	Backplane (riser) connector	23	Diskette drive connector
6	Graphics monitor connector	24	CD audio out connector
7	Keyboard connector	25	IDE (secondary) connector
8	Mouse connector	26	CD ROM (IDE secondary) connector
9	Serial I/F (COM2) connector	27	Boxed processor fan connector
10	Network I/F connector	28	Sec. IDE (CD-ROM) slave jumper
11	Parallel I/F connector	29	IDE (primary) connector
12	Universal Serial Ports (top, B; bottom, A)	30	Processor connector
13	Audio line in jack	31	Memory expansion sockets
14	Audio line out jack	32	CD audio out connector
15	Serial I/F (COM1) header [1]	33	WOL connector
16	Power supply connector	34	SCSI LED connector
17	CMOS clear switch	35	Smart Cover Sensor switch
18	Password enable jumper	36	

NOTES:

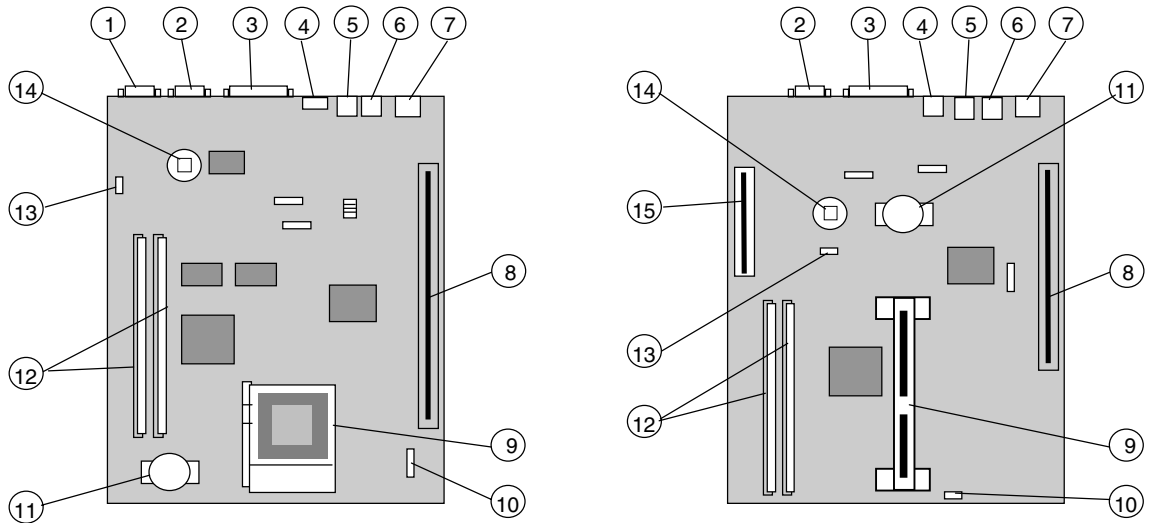
[1] Connects to chassis-mounted DB-9 connector through cable assembly.

■ Component location on PCA# 010430 board.

■ Component location on PCA# 010120 board.

Figure 2-12. Compaq Deskpro EN SFF Backplane/System Board Layouts

Figure 2-6 shows the location of connectors and switches for the Deskpro EN desktop and minitower system boards. Note that either board may be used in either formfactor.



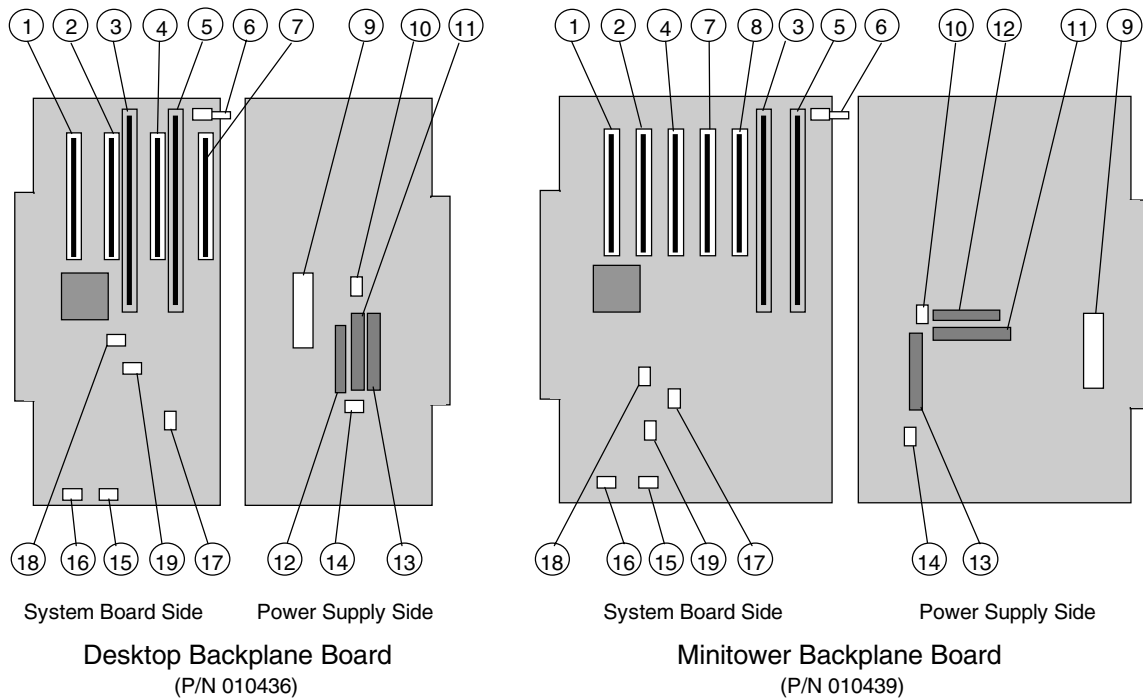
Celeron-Based System Board
(PCA # 010127)

Pentium III-Based System Board
(PCA # 010693)

Item	Function	Item	Function
1	Graphics monitor connector	7	(bottom) USB Port A I/F
2	Serial I/F (COM1 bottom, COM2 top)	8	Backplane connector
3	Parallel I/F	9	Processor connector
4	(top) Mouse connector	10	Boxed fan connector
4	(bottom) Keyboard connector	11	Battery for CMOS
5	(top) Audio Line Input	12	Memory expansion sockets
5	(bottom) Audio Line Output	13	Password enable/disable jumper
6	(top) Audio Mic Input	14	CMOS Clear button
6	(bottom) Audio Headphone Output	15	AGP Slot (NLX-type)
7	(top) USB Port B I/F	--	--

Figure 2-13. Compaq Deskpro EN Desktop/Minitower System Board Layouts

Figure 2-7 shows the connector and switch locations for the two types of backplane boards.

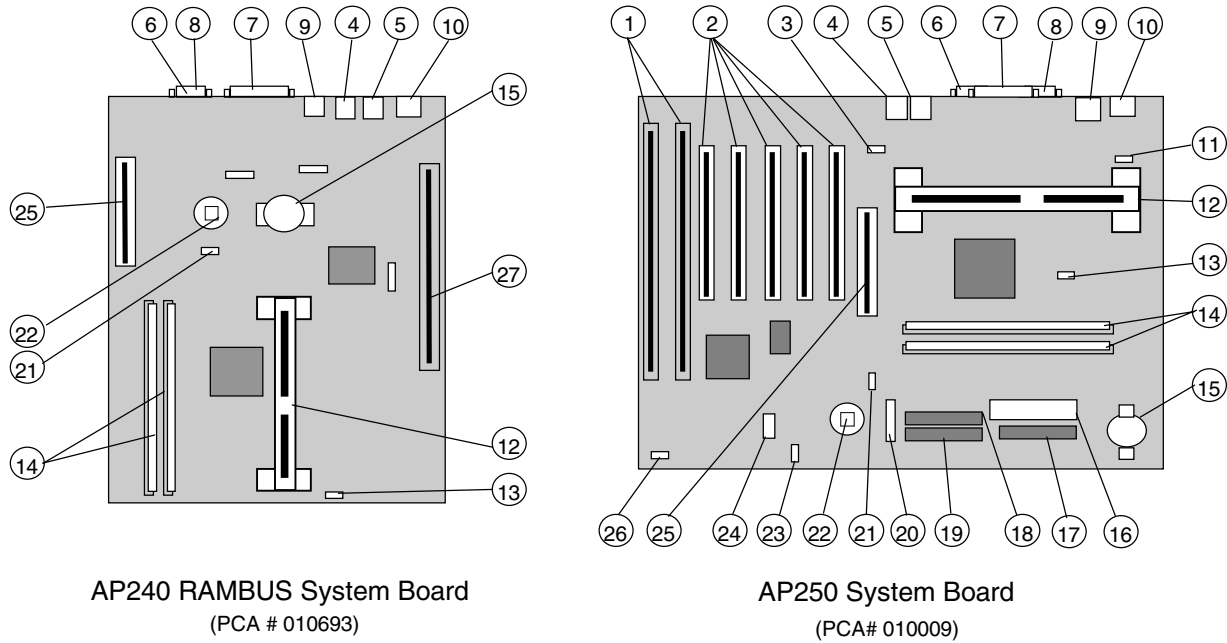


Item	Function	Item	Function
1	PCI connector J20 (slot 1)	10	CD audio connector P7
2	PCI connector J21 (slot 2)	11	Secondary EIDE connector P21
3	ISA connector J10 [1]	12	Diskette drive connector P10
4	PCI connector J22 (slot 3) [2]	13	Primary EIDE connector P20
5	ISA connector J11 [3]	14	Power button/LED header P5
6	Smart Cover Sensor switch	15	Chassis fan header P8
7	PCI connector J23 (slot 4) [4]	16	Speaker header P6
8	PCI connector J24 (slot 5)	17	SCSI LED header P29
9	Power supply connector P1	18	WOL header P9
--	--	19	AOL header P12

NOTES:

- [1] Shares slot with item 4 on desktop backplane (combo slot 1)
- [2] Shares slot with item 3 on desktop backplane (combo slot 1)
- [3] Shares slot with item 7 on desktop backplane (combo slot 2)
- [4] Shares slot with item 5 on desktop backplane (combo slot 2)
- [5] Later production units use the 009663-001 board

Figure 2-14. Compaq Deskpro EN Desktop/Minitower Backplane Board Layouts



Item	Description
1	ISA expansion connectors
2	PCI expansion connectors
3	Chassis speaker header
4	Audio line out (bottom), audio line in (top)
5	Audio headphones (bottom), audio microphone (top)
6	Serial I/F connector (COM2)
7	Parallel I/F connector
8	Serial I/F connector (COM1)
9	Mouse connector (top), keyboard connector (bottom)
10	Universal serial bus I/F connectors: port A (bottom), port B (top)
11	Chassis fan connector
12	Processor slot
13	Boxed processor fan connector
14	RIMM sockets
15	Battery
16	Power supply connector
17	Diskette drive connector
18	IDE secondary connector
19	IDE primary connector
20	Power switch/LED connector
21	Password clear jumper
22	CMOS clear button
23	Wake-on-LAN (WOL) connector
24	Alert-On-LAN (AOL)/SOS connector
25	AGP slot
26	CD-ROM audio connector
27	Backplane connector

Figure 2-15. Compaq Deskpro Workstation System Board Layouts

2.4 SYSTEM ARCHITECTURE

Compaq Deskpro Personal Computers feature Intel processors and chipsets and are available in three basic architectures:

- ◆ Celeron processor with 810 chipset (Figure 2-16)
- ◆ Pentium III processor with 810e chipset (Figure 2-17)
- ◆ Pentium III processor with 820 chipset (Figure 2-18)

The three architectures provide very similar I/O capabilities but have key differences in the processor/memory/graphics subsystems.

Celeron-based systems employ the Intel 810 chipset. The 810 chipset uses an 82810-DC100 Graphics/Memory Controller Hub (GMCH) that integrates an AGP 2X graphics controller. The 82810 GMCH also provides support for two SDRAM DIMMs of system memory.

Pentium III-based systems feature the Intel 810e or 820 chipset. The 810e chipset uses the 82810e-DC100 GMCH designed to support the Pentium III processor with SDRAM and an integrated AGP 2X graphics controller. The 820 chipset uses an 82820 Memory Controller Hub (MCH) that includes a Direct Rambus controller that supports two RIMMs of RDRAM for system memory. The 82820 MCH includes an AGP interface that supports AGP 4X transfers with a compliant graphics controller card installed in the AGP slot.

The 810, 810e, and 820 chipsets utilize an 82801 I/O Controller Hub (ICH) that provides two IDE interfaces, two USB interfaces, and a PCI bus controller. The 33-MHz 32-bit PCI bus provides support for the network interface controller (if present), and PCI expansion cards.

Table 2-1 lists differences between system architectures:

Table 2-2. Architectural Comparison			
	Celeron/ 810-Based	Pentium III/ 810e-Based	Pentium III/ 820-Based
Systems used on	EP, EN SFF/DT/MT	EP, EN SFF	EN SFF/DT/MT, Workstations
FSB Speeds supported	66, 100 MHz	100, 133 MHz	100, 133 MHz
Hard Drive Type (std)	UATA/66	UATA/66	UATA/66 or Wide Ultra SCSI
System Memory:			
Type	PC100 SDRAM	PC100 SDRAM	PC600 / PC700 RDRAM [1]
ECC/non-ECC	Non-ECC	Non-ECC	ECC or Non-ECC
No. of sockets	2	2	2
Graphics Controller	Integrated AGP 2X	Integrated AGP 2X	Matrox G400 AGP 4X Graphics Cntlr. [2]

NOTE:

[1] PC600 RDRAM used on systems w/533 MHz (or slower) processor.

PC700 RDRAM used on systems w/600 MHz (or faster) processor.

[2] Graphics controller embedded on EN SFF system board, separate card on EP, EN DT/MT systems. Workstations may be configured with ELSA or 3Dlabs controller card.

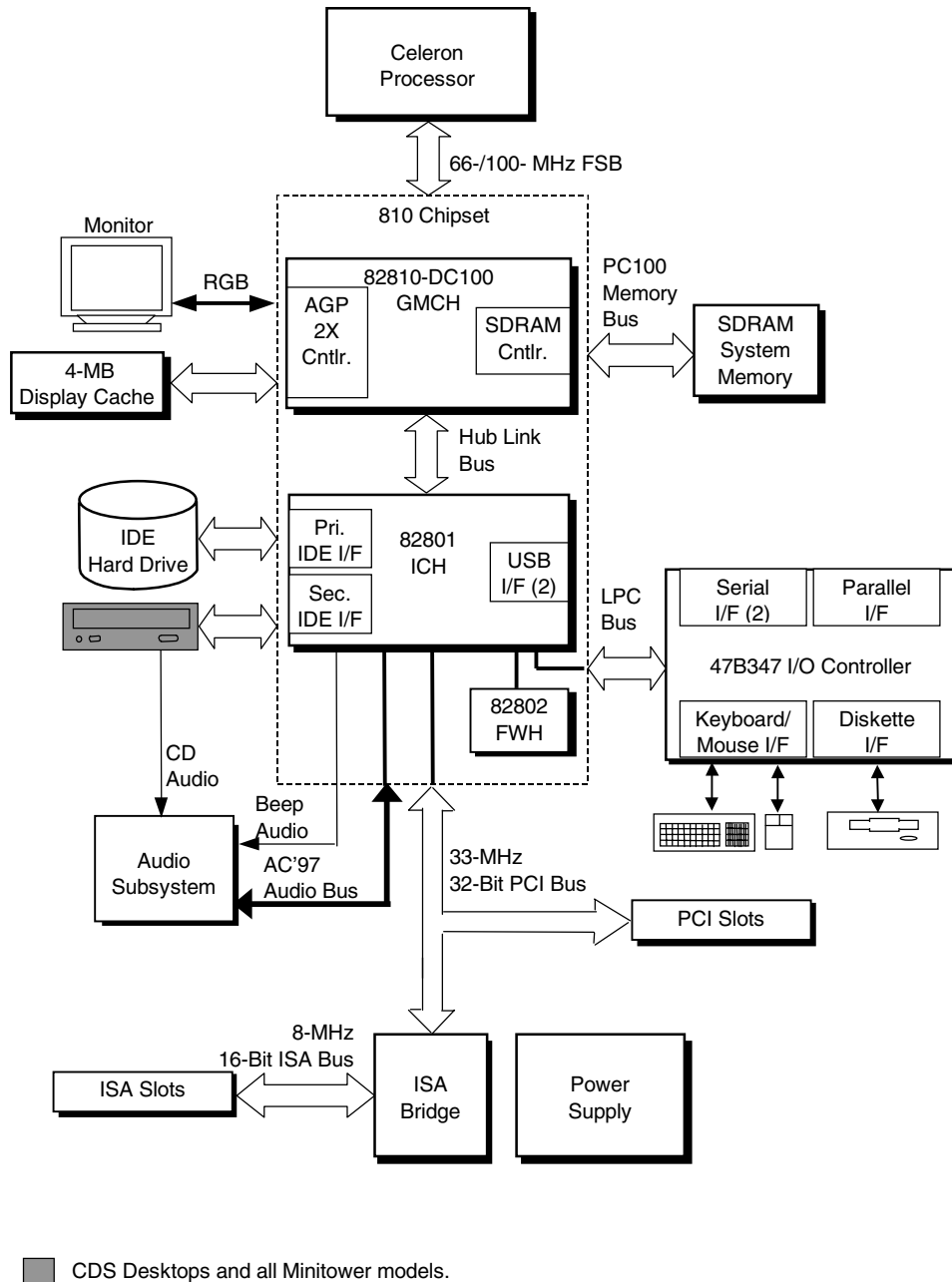


Figure 2-16. Celeron Processor / 810 Chipset-Based Architecture, Block diagram

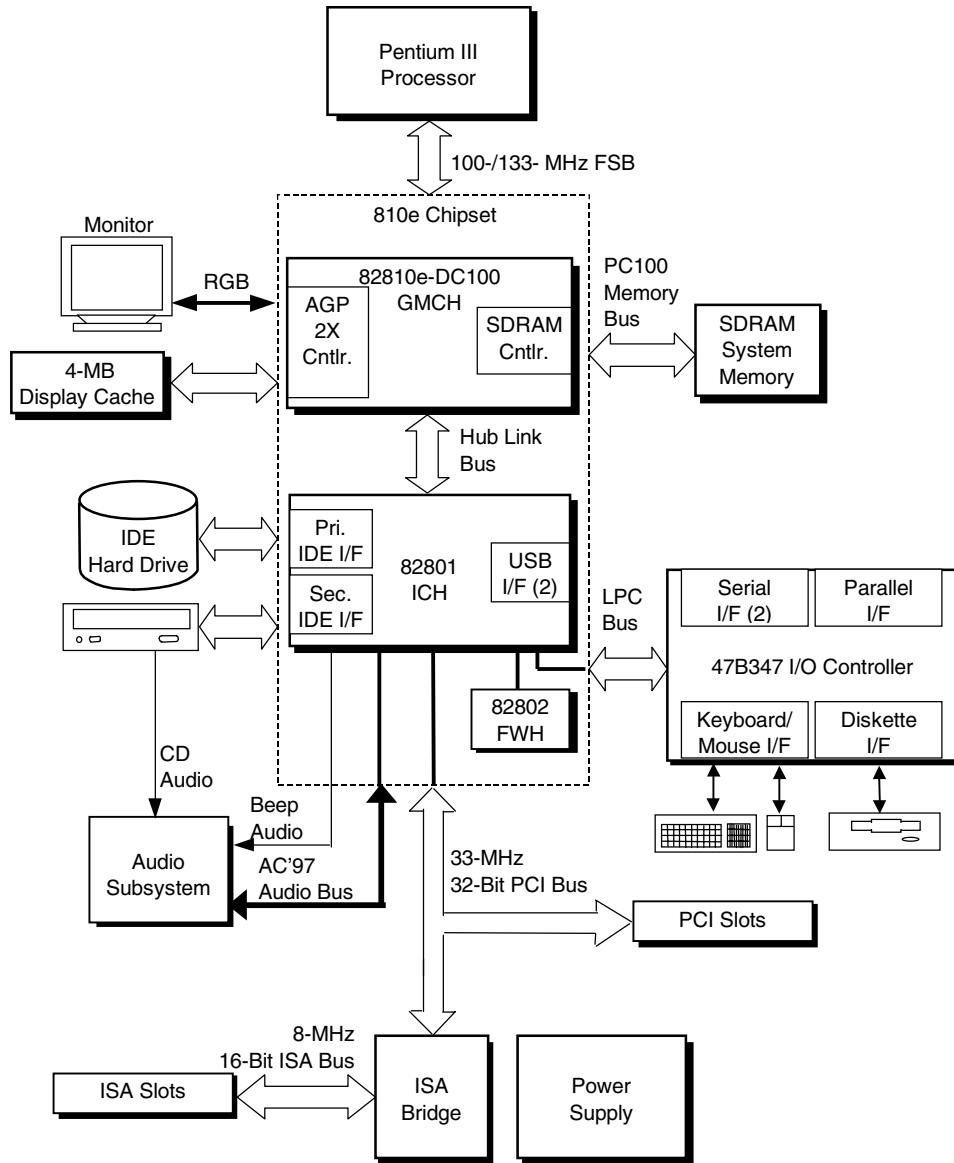
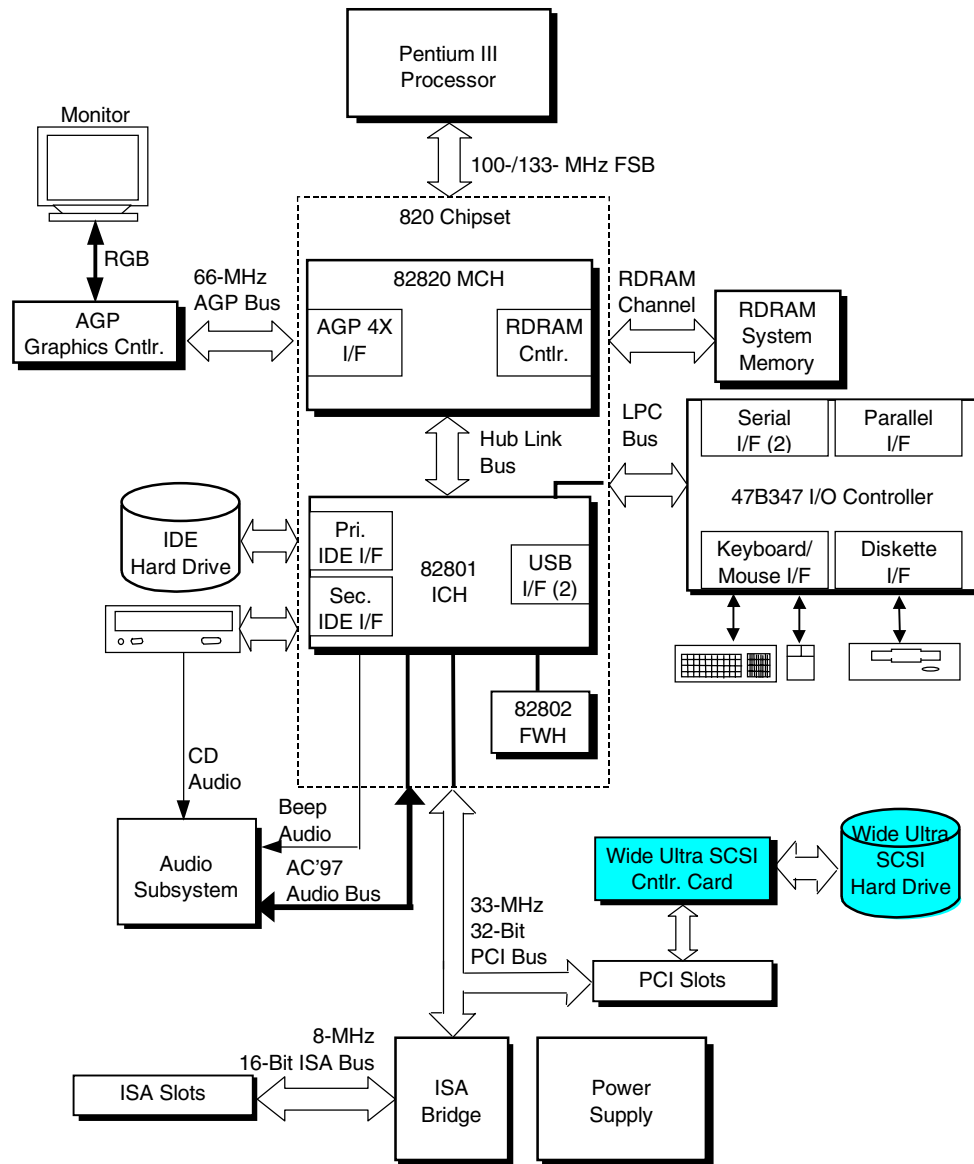


Figure 2–17. Pentium III Processor / 810e Chipset-Based Architecture, Block diagram



Select Deskpro Workstation models only.

Figure 2-18. Pentium III Processor / 820 Chipset-Based Architecture, Block diagram

2.4.1 PROCESSORS

The Compaq Deskpro family includes models based on Celeron and Pentium III processors. These processors are backward-compatible with software written for the Pentium II, Pentium MMX, Pentium Pro, Pentium, and x86 microprocessors. Both processor architectures include a floating-point unit and first and secondary caches providing enhanced performance for multimedia applications.

2.4.1.1 Celeron Processor

Select Compaq Deskpro systems use the Intel Celeron processor in a 370-pin PPGA package with a heat sink and mounted in a PPGA370 zero-insertion-force (ZIF) socket (Figure 2-19). The Celeron processor provides economical performance and is compatible with software written for previous generation processors such as Pentium II, Pentium MMX, Pentium, and x86 processors. Featuring a Pentium-type core architecture, the Celeron processor integrates a dual-ALU CPU with a floating-point unit, 32-KB first-level cache, and 128-KB second level cache, all of which operate at full processing (CPU) speed. The Celeron processor includes MMX technology for enhanced multimedia performance.

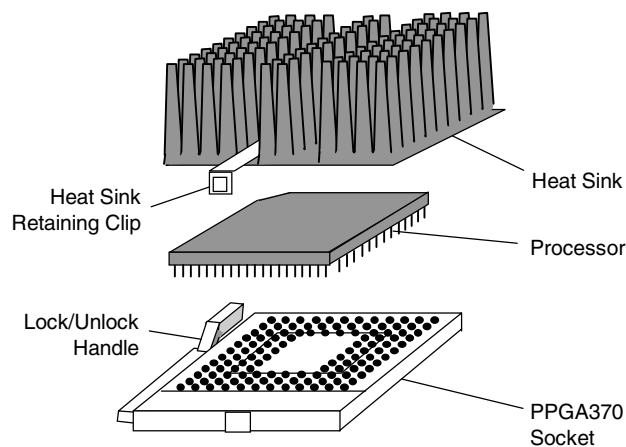


Figure 2-19. Celeron Processor Assembly And Mounting

The ZIF-type PPGA370 socket allows easy changing/upgrading of the Celeron processor. Raising the Lock/Unlock handle of the socket in the vertical position allows the processor to be removed or inserted into the socket. Lowering the Lock/Unlock handle in the down (horizontal) position locks the processor in place. Factory configurations use processors fitted with passive heat sinks. Upgrade (boxed) processors may be fitted with a heat sink/fan assembly with a power cable that attaches to a fan-power header provided on the system board. The processor clock frequency is automatically set by chipset logic, eliminating the need for setting DIP switches when upgrading the processor.

2.4.1.2 Pentium III Processor

The Intel Pentium III processor used on select Compaq Deskpros is contained in a single edge connector cartridge (SECC2) with heat sink and installs in a Slot-1 (SC242) connector (Figure 2-20). Currently the maximum performance processor for Compaq Deskpros, the Pentium III processor is compatible with software written for Celeron, Pentium II, Pentium MMX, Pentium, and x86 processors.

The Pentium III processor core integrates a dual-ALU CPU with a floating-point unit and 32-KB first-level cache operating at processing (CPU) speed. First-generation (.25-micron) processors feature a 512-KB write-through secondary cache operating at half processing speed. Second-generation (.18-micron) processors feature 256 kilobytes of secondary cache included on the CPU die operating at full processor speed. The Pentium III processor includes MMX technology for enhanced multimedia performance. Also included are 70 additional streaming SIMD extensions (SSE) for enhancing 3D graphics and speech processing performance.

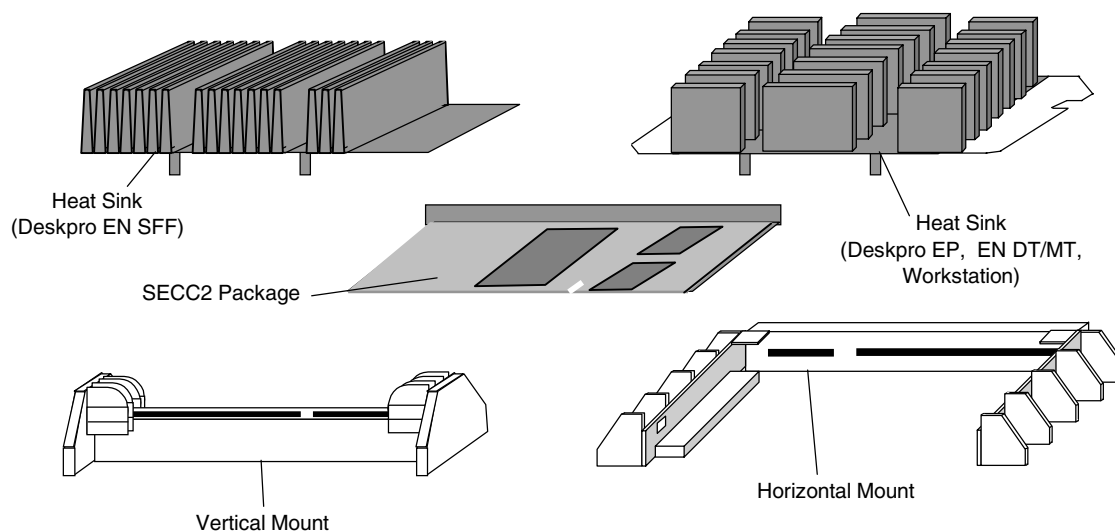


Figure 2-20. Pentium III Processor Assembly and Mounting

The Pentium III is mounted vertically in Compaq Deskpro EP, EN DT/MT, and all DeskproWorkstation systems and horizontally in Compaq Deskpro EN Small Form Factor systems. The electrical (Slot 1/SC242) interface is similar to that used on Pentium II-based systems although a different cartridge retention mechanism (unique to the Pentium III) is employed. These systems feature automatic selection of the processor clock frequency, eliminating the need for setting DIP switches when upgrading the processor.

2.4.2 CHIPSETS

Compaq Deskpros employ Intel chipsets designed to compliment the processor and provide the central point for a system's data transactions. Three types of chipsets are employed:

- ◆ 810 Chipset supporting the Celeron processor
- ◆ 810e Chipset supporting the Pentium III processor
- ◆ 820 Chipset supporting the Pentium III processor

Each chipset is composed of a memory controller hub (MCH), an I/O controller hub (ICH), and a firmware hub (FWH). The MCH defines the chipset type, since the same ICH and FWH components are used for all three chipsets. Table 2-3 shows the functions provided by the chipsets.

Table 2-3.
Chipset Comparison

Chipset Name	Component Type	Function
810	82810-DC100 GMCH	AGP 2X graphics controller (i740 equivalent) SDRAM controller supporting 2 PC100 DIMMs 66-/100-MHz FSB
	82801AA ICH	PCI bus I/F LPC bus I/F SMBus I/F IDE I/F with UATA/66 support AC '97 controller RTC/CMOS IRQ controller Power management logic USB I/F (2)
	82802 FWH	Loaded with Compaq BIOS Random number generator
810e	82810e-DC100 GMCH	AGP 2X graphics controller (i740 equivalent) SDRAM controller supporting 2 PC100 DIMMs 100-/133-MHz FSB
	82801AA ICH	Same as for 810 Chipset
	82802 FWH	Same as for 810 Chipset
820	82820 MCH	AGP 4X I/F RDRAM controller supporting 2 RIMMs 100-/133-MHz FSB
	82801AA ICH	Same as for 810 Chipset
	82802 FWH	Same as for 810 Chipset

2.4.3 SUPPORT COMPONENTS

Input/output functions not provided by the chipset are handled by other support components. Some of these components also provide “housekeeping” and various other functions as well. Table 2-4 shows the functions provided by the support components.

Table 2-4. Support Component Functions	
Component Name	Function
LPC47B34x I/O Controller	Keyboard and pointing device I/F Diskette I/F Serial I/F (COM1 and COM2) Parallel I/F (LPT1, LPT2, or LPT3) AGP, PCI reset generation ISA serial IRQ converter Power button logic Slow speed detection S3 regulator controller GPIO ports
Intel 82380 or ITE 8889	PCI/ISA bridge ISA bus controller
AD1881 Audio Codec	Audio mixer Digital-to-analog converter Analog-to-digital converter Analog I/O: Mic input Line input CD input Line output
82559 Ethernet Controller [1]	Network interface controller PHY interface

NOTE:

[1] Deskpro EN SFF only

2.4.4 SYSTEM MEMORY

These systems utilize one of two types of memory depending on the architecture:

- ◆ Synchronous RAM (PC100 SDRAM, non-ECC only) on systems employing the 810 or 810e chipset
- ◆ Direct Rambus RAM (RDRAM, ECC or non-ECC) on systems employing the 820 chipset

Systems using the 810 or 810e chipset provide two DIMM sockets, with at least one socket populated with a single- or double-sided memory module.

Systems using the 820 chipset provide two RIMM sockets with the first socket populated with a RIMM and the remaining socket populated with a RIMM or a RIMM continuity module.

2.4.5 MASS STORAGE

All models include a 3.5 inch 1.44-MB diskette drive installed as drive A. All models also include two (one primary, one secondary) PCI bus-mastering Enhanced IDE (EIDE) controllers integrated into the chipset. Each controller provides UATA/66 support for two drives for a total of four IDE devices. A 32x CD-ROM is included on desktop CDS models and on all MT models.

2.4.6 SERIAL AND PARALLEL INTERFACES

All models include two serial ports and a parallel port accessible at the rear of the chassis. Each serial port is RS-232-C/16550-compatible and supports standard baud rates up to 115,200 as well as two high-speed baud rates of 230K and 460K, and utilize DB-9 connectors. The parallel interface is Enhanced Parallel Port (EPP1.9) and Enhanced Capability Port (ECP) compatible, and supports bi-directional data transfers through a DB-25 connector.

2.4.7 UNIVERSAL SERIAL BUS INTERFACE

All models feature two Universal Serial Bus (USB) ports that provide a 12Mb/s interface for peripherals. The USB provides hot plugging/unplugging (Plug 'n Play) functionality.

2.4.8 GRAPHICS SUBSYSTEM

The type of graphics subsystem employed is dependent on the chipset used. A comparison is provided in Table 2-5.

Table 2-5.
Graphics Subsystem Comparison

	810- or 810e-Based System	820-Based System
Graphics Controller	i740 AGP 2X Controller [1]	Matrox G400 AGP 4X Controller [2]
Graphics Memory	4 MB SDRAM	16 MB SDRAM
Maximum Resolution	1600 x 1200 @ 256 colors	1920 x 1080 @ 16.7M colors
Upgrade method	Disabling cntlr. and adding PCI card	Replacing AGP card [3]

NOTE:

[1] Graphics controller integrated into chipset's GMCH component.

[2] Separate AGP card in Deskpro EP and EN DT/MT systems.

Controller resident on system board in Deskpro EN SFF system.

Also, Workstation systems may be configured with ELSA or 3Dlabs AGP graphics card.

[3] On Deskpro EN SFF system, upgrade method is same as for 810/810e-based system.

2.4.9 AUDIO SUBSYSTEM

All models feature the Compaq Premier Sound system. The audio subsystem features an AC'97 specification-based design and uses the integrated AC97 audio controller of the chipset and an AC'97-compliant audio codec. Standard microphone and line inputs and headphone and line outputs are provided. Playback audio is processed through a five-level equalizer designed to compensate for chassis acoustics. A low-distortion 5-watt amplifier drives a long-excursion speaker for optimum sound.

2.5 SPECIFICATIONS

This section includes the environmental, electrical, and physical specifications for the Compaq Deskpro Series Personal Computers. Where provided, metric statistics are given in parenthesis. All specifications subject to change without notice.

Table 2-6.
Environmental Specifications

Parameter	Operating	Nonoperating
Air Temperature	50° to 95° F (10° to 35° C)	-24° to 140° F (-30° to 60° C)
Shock	N/A	60.0 g for 2 ms half-sine pulse
Vibration	0.000215g ² /hz, 10-300 Hz [1]	0.0005g ² /Hz, 10-500 Hz [1]
Humidity	90% RH @ 36° C (no hard drive)	95% RH @ 36° C
Maximum Altitude	10,000 ft (3048 m)	30,000 ft (9,144 m)

NOTE:

[1] 0.5 grms nominal

Table 2-7.
Electrical Specifications

Parameter	U.S.	International
Input Line Voltage:		
Nominal:	110 - 120 VAC	200 - 240 VAC
Maximum:	90 - 132 VAC	180 - 264 VAC
Input Line Frequency Range:		
Nominal:	50 - 60 Hz	50 - 60 Hz
Maximum:	47 - 63 Hz	47 - 63 Hz
Power Supply:		
Maximum Continuous Power		
EN SFF	120 watts	120 watts
EP, EN DT/MT, Workstations	200 watts	200 watts
Maximum Line Current Draw		
EN SFF	4.0 A	2.0 A
EP, EN DT/MT, Workstations	5.5 A	3.0 A

Table 2-8.
Physical Specifications

Parameter	EP [2] [3]	EN SFF	EN DT [4]	EN MT [4]
Height	6.60 in (16.76 cm)	3.25 in (8.25 cm)	5.88 in (14.93 cm)	20.25 in (51.44 cm)
Width	17.65 in (44.83 cm)	12.5 in (31.75 cm)	19.16 in (48.66 cm)	8.38 in (21.29 cm)
Depth	17.11 in (43.46 cm)	14.6 in (37.08 cm)	16.82 in (42.72 cm)	18.60 in (47.24 cm)
Weight (nom.) [1]	33 lb (14.95 kg)		32.0 lb (14.50 kg)	40.0 lb (18.20 kg)

NOTES:

[1] System weight may differ depending on installed drives/peripherals.

[2] Desktop configuration. For minitower configuration, swap Height and Width dimensions.

[3] or Workstation AP250

[4] or Workstation AP240

Table 2-9.
Diskette Drive Specifications
(Compaq SP# 179161-001)

Parameter	Measurement
Media Type	3.5 in 1.44 MB/720 KB diskette
Height	1/3 bay (1 in)
Bytes per Sector	512
Sectors per Track:	
High Density	18
Low Density	9
Tracks per Side:	
High Density	80
Low Density	80
Read/Write Heads	2
Average Access Time:	
Track-to-Track (high/low)	3 ms/6 ms
Average (high/low)	94 ms/173ms
Settling Time	15 ms
Latency Average	100 ms

Table 2-10.
32x CD-ROM Drive Specifications
(SP# 327659-001)

Parameter	Measurement
Interface Type	IDE
Transfer Rate:	
Max. Sustained	4800 KB/s
Burst	16.6 MB/s
Media Type	Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA
Capacity:	
Mode 1, 12 cm	550 MB
Mode 2, 12 cm	640 MB
8 cm	180 MB
Center Hole Diameter	15 mm
Disc Diameter	8/12 cm
Disc Thickness	1.2 mm
Track Pitch	1.6 μ m
Laser	
Beam Divergence	53.5 +/- 1.5 °
Output Power	53.6 0.14 mW
Type	GaAs
Wave Length	790 +/- 25 nm
Average Access Time:	
Random	<100 ms
Full Stroke	<150 ms
Audio Output Level	0.7 Vrms
Cache Buffer	128 KB

Table 2-11.
Hard Drive Specifications

Parameter	4.3 GB	6.4 GB	9.1 GB	13.5 GB	18.2 GB	20.0 GB
P/N	112254	112255	160062	118179	160063	157403
Interface	UATA	UATA	SCSI [1]	UATA	SCSI [1]	UATA
Drive Type	65	65	65	65	65	65
Drive Size	3.5/5.25 in	3.5/5.25 in	5.25 in	5.25	5.25	5.25
Transfer Rate (max)	66.6 MB/s	66.6 MB/s	160 MB/s	66.6 MB/s	160 MB/s	66.6 MB/s
Seek Time (w/settling)						
Single Track	2.0 ms	2.0 ms	.8 ms	1.7 ms	.8 ms	1.7 ms
Average	9.5 ms	<9.7 ms	6.9 ms	8.5 ms	6.9 ms	8.5 ms
Full Stroke	19.0 ms	20.0 ms	15.0 ms	15.0	15 ms	15 ms
Disk Format (logical):						
# of Cylinders	8419	13328	13816	15011	13816	16383
# of Data Heads	15	15	4	8	8	16
# of Sectors per Track	63	63	227-387	214-312	227-387	63
Rotation Speed	5400 RPM	5400 RPM	10K RPM	7200 RPM	10K RPM	7200 RPM
Drive Fault Prediction	SMART II	SMART II	SMART III	SMART III	SMART III	SMART III

NOTE:

[1] Wide Ultra3 SCSI I/F

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Chapter 3

PROCESSOR/ MEMORY SUBSYSTEM

3.1 INTRODUCTION

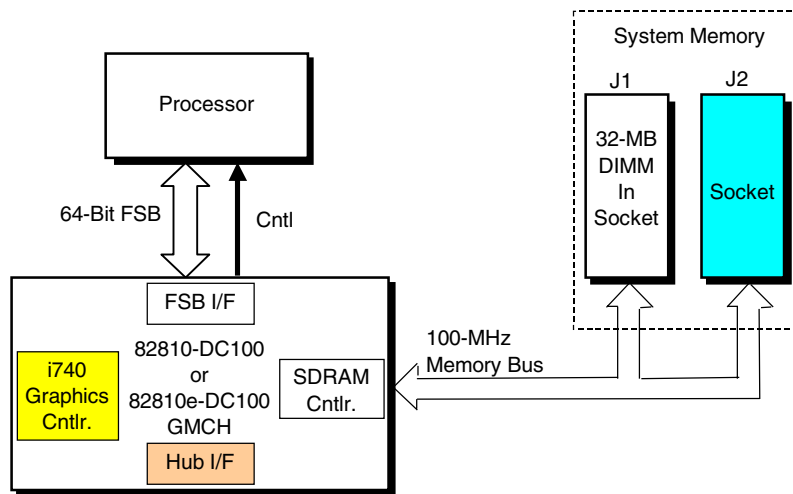
This chapter describes the processor/cache memory subsystem of Compaq Deskpro Personal Computers featuring Celeron and Pentium III processors and the 810, 810e, and 820 chipsets.

This chapter includes the following topics:

- ◆ 810/810e Chipset-based processor/memory subsystem [3.2] page 3-2
- ◆ 820 Chipset-based processor/memory subsystem [3.4] page 3-9

3.2 810/810e-BASED PROCESSOR/MEMORY SUBSYSTEM

Systems based on the 810 chipset feature an Intel Celeron processor (in a 370-pin PPGA package) working with the Intel 82810-DC100 Graphics/Memory Controller Hub (GMCH) (Figure 3-1). Systems based on the 810e chipset feature an Intel Pentium III processor working with an Intel 810e-DC100 GMCH. Both combinations each provide support for up to two SDRAM DIMMs and use an i740 3D graphics controller (covered in Chapter 6) integrated into the GMCH component. The key difference between the 810 and 810e chipsets is processor support, with the 82810-DC100 GMCH containing a 66-/100-MHz Front Side Bus (FSB) interface supporting the Celeron processor and the 82810e-DC100 GMCH containing a 100-/133-MHz FSB interface supporting the Pentium III processor.



	82810-DC100 GMCH	82810e-DC100 GMCH
Systems used on	EP, EN SFF/DT/MT	EP, EN SFF
Processor supported	Celeron	Pentium III
FSB speed	66/100 MHz	100/133 MHz

- May be populated with optional DIMM
- Covered in Chapter 6
- Covered in Chapter 4

Figure 3–1. 810/810e Chipset-Based Processor/Memory Subsystem Architecture

3.2.1 CELERON PROCESSOR

The 810-based system board includes a socket-7 type socket that accommodates the Celeron processor in a 370-pin PPGA package. The Celeron processor (Figure 3-2) uses a dual-ALU CPU with branch prediction and MMX support, floating point unit (FPU) for math coprocessing, a 32-KB primary (L1) cache, and a 128-KB secondary (L2) cache. All internal functions, except for the front side bus interface (FSB I/F), operate at processor speed.

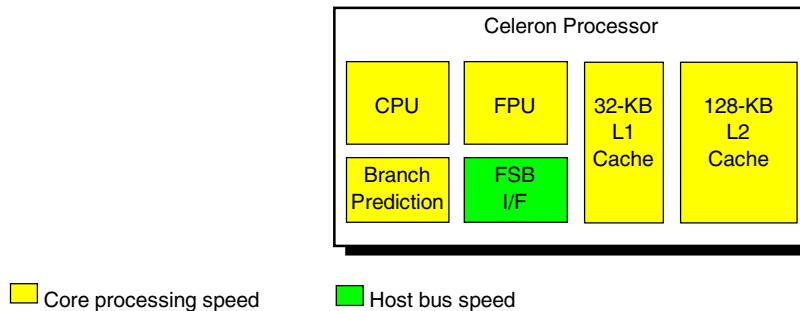


Figure 3-2. Celeron Processor Internal Architecture

The Celeron processor is software-compatible with earlier generation Pentium II, Pentium MMX, Pentium, and x86 processors. The MMX support provided by the Celeron consists of 57 special instructions for accelerating multimedia communications applications. Such applications often involve computing-intensive loops that can take up as much as 90 percent of the CPU's execution time. Using a parallel-processing technique called single-instruction multiple-data (SIMD), MMX logic processes data 64 bits at a time. Specific applications that can benefit from MMX technology include 2D/3D graphics, audio, speech recognition, video codecs, and data compression.

The Celeron processor is mounted in a PGA370 connector and easily replaced. The core and FSB frequencies are determined by a battery-backed register in the ICH, which reads frequency strapping signals from the processor, eliminating the use of a DIP switch. The 82810-DC100 GMCH supports the processors listed in the following table:

Table 3-1.
Celeron Processor Statistical Comparison

Processor	Core/L1/L2 Freq.	FSB Freq.	Core Voltage	Power Consumption
Celeron 300A	300 MHz	66 MHz	2.0 v	17.8 w
Celeron 333	333 MHz	66 MHz	2.0 v	19.7 w
Celeron 366	366 MHz	66 MHz	2.0 v	21.7 w
Celeron 400	400 MHz	66 MHz	2.0 v	23.7 w
Celeron 433	433 MHz	66 MHz	2.0 v	24.1 w
Celeron 466	466 MHz	66 MHz	2.0 v	25.6 w
Celeron 500	500 MHz	66 MHz	2.0 v	Na
Celeron 533	533 MHz	66 Mhz	2.0 v	Na

3.2.2 PENTIUM III PROCESSOR

The Intel Pentium III processor is packaged in a Single Edge Connector Cartridge (SECC2) that contains the microprocessor and a secondary (L2) cache. The processor's architecture (Figure 3-3) includes the same core functionality as described previously for the Celeron processor but includes a larger L2 cache and higher operating speeds.

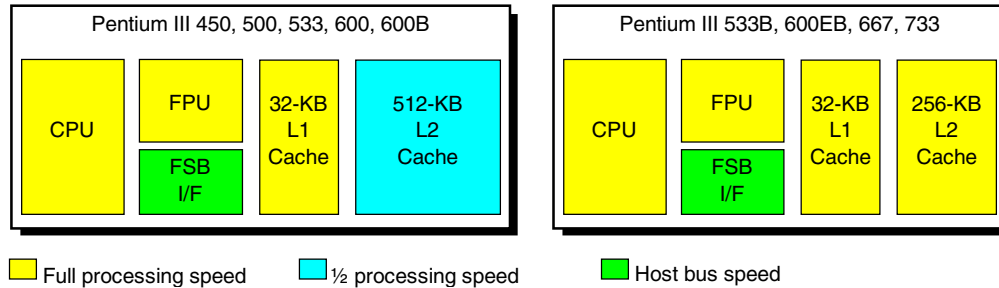


Figure 3-3. Pentium III Processor Internal Architecture

Table 3-2.
Pentium III Processor Statistical Comparison

Processor	CPU/L1 Speed	L2 Size / Speed	Core Voltage	FSB Speed
Pentium III 450	450 MHz	512 KB @ 225 MHz	2.00 VDC	100 MHz
Pentium III 500	500 MHz	512 KB @ 250 MHz	2.00 VDC	100 MHz
Pentium III 500E	500 MHz	256 KB @ 500 MHz	1.60 VDC	100 MHz
Pentium III 533	533 MHz	512 KB @ 266 MHz	2.00 VDC	100 MHz
Pentium III 533B	533 MHz	512 KB @ 266 MHz	2.05 VDC	133 MHz
Pentium III 533EB	533 MHz	256 KB @ 533 MHz	1.65 VDC	133 MHz
Pentium III 550	550 MHz	512 KB @ 275 MHz	2.00 VDC	100 MHz
Pentium III 550E	550 MHz	256 KB @ 550 MHz	1.60 VDC	100 MHz
Pentium III 600	600 MHz	512 KB @ 300 MHz	2.05 VDC	100 MHz
Pentium III 600B	600 MHz	512 KB @ 300 MHz	2.05 VDC	133 MHz
Pentium III 600E	600 MHz	256 KB @ 600 MHz	1.65 VDC	100 MHz
Pentium III 600EB	600 MHz	256 KB @ 600 MHz	1.65 VDC	133 MHz
Pentium III 667	667 MHz	256 KB @ 667 MHz	1.65 VDC	133 MHz
Pentium III 700	700 MHz	256 KB @ 700 MHz	1.65 VDC	100 MHz
Pentium III 733	733 MHz	256 KB @ 733 MHz	1.65 VDC	133 MHz

The Pentium III processor is software-compatible with Celeron, Pentium II, Pentium MMX, Pentium, and x86 processors. The Pentium III processor also features 70 FPU-based streaming SIMD extensions (SSE) that, when implemented by appropriate software, can enhance 3D transforming and speech processing operations. Operating system requirements for SSE support are as follows:

<u>Operating System</u>	<u>Level of SSE Support</u>
Windows 95	No SSE support
Windows 98, OSR0	SSE support though ISV and OpenGL 6.1 applications only
Windows 98, OSR1	SSE support though ISV, OpenGL, and DirectX applications
Windows 2000	SSE support with ISV, OpenGL, and DirectX applications
Windows NT 4.0	SSE support requires driver and Service Pack 4 (SP5 recommended)

3.2.3 SDRAM MEMORY

The 810-/810e-based system uses PC100 SDRAM for system memory. The memory interface consists of a 64-bit data bus operating at 100 MHz providing a maximum throughput rate of 800 MB/s. The system board provides two 168-pin SDRAM DIMM sockets that accommodate single- or double-sided DIMMs. **This system is designed for using non-ECC DIMMs only.**

If using memory modules from third party suppliers the following DIMM type is recommended: **100-MHz unbuffered RAM supporting CAS latency (CL) 2 or 3 with a data access time (clock-to-data out) of 9.0 ns or less @ CL=2 or CL=3.**

NOTE: The 82810/82810e GMCH performs memory accesses at 100 MHz regardless of the FSB frequency.

The RAM type and operating parameters are detected during POST by the system BIOS using the serial presence detect (SPD) method. This method employs an I²C bus to communicate with an EEPROM on each installed DIMM. The EEPROM holds the type and operating parameter data.

The supported format complies with the JEDEC specification for 128-byte EEPROMs. This system also provides support for 256-byte EEPROMs to include additional Compaq-added features such as part number and serial number. The SPD format as supported in this system is shown in Table 3-3.

The key SPD bytes that BIOS checks for compatibility are 2, 9, 10, 18, 23, and 24. **If BIOS detects EDO DIMMs a “memory incompatible” message will be displayed and the system will halt.** If ECC DIMMs are used, all DIMMs installed must be ECC for ECC benefits (error logging) to be realized.

Once BIOS determines the DIMM type the DRAM speed and CAS latency is checked based on the following criteria:

<u>Bus Speed</u>	<u>Cycle Time</u>	<u>Access from Clock</u>
100 MHz	10 ns	6 ns @ 50 pf loading

NOTE: Refer to chapter 8 for a description of the BIOS procedure of interrogating DIMMs.

Only CAS latencies of 2 or 3 are supported. If DIMMs with unequal CAS latencies are installed then operation will occur based on the DIMM with the greatest latency.

If an incompatible DIMM is detected the NUM LOCK will blink for a short period of time during POST and an error message may or may not be displayed before the system hangs.

The SPD address map is shown below.

Table 3-3.
SPD Address Map (SDRAM DIMM)

Byte	Description	Notes	Byte	Description	Notes
0	No. of Bytes Written Into EEPROM	[1]	27	Min. Row Prechge. Time	[7]
1	Total Bytes (#) In EEPROM	[2]	28	Min. Row Active to Delay	[7]
2	Memory Type		29	Min. RAS to CAS Delay	[7]
3	No. of Row Addresses On DIMM	[3]	30, 31	Reserved	
4	No. of Column Addresses On DIMM		32..61	Superset Data	[7]
5	No. of Module Banks On DIMM		62	SPD Revision	[7]
6, 7	Data Width of Module		63	Checksum Bytes 0-62	
8	Voltage Interface Standard of DIMM		64-71	JEP-106E ID Code	[8]
9	Cycletime @ Max CAS Latency (CL)	[4]	72	DIMM OEM Location	[8]
10	Access From Clock	[4]	73-90	OEM's Part Number	[8]
11	Config. Type (Parity, Nonparity, etc.)		91, 92	OEM's Rev. Code	[8]
12	Refresh Rate/Type	[4] [5]	93, 94	Manufacture Date	[8]
13	Width, Primary DRAM		95-98	OEM's Assembly S/N	[8]
14	Error Checking Data Width		99-125	OEM Specific Data	[8]
15	Min. Clock Delay	[6]	126, 127	Reserved	
16	Burst Lengths Supported		128-131	Compaq header "CPQ1"	[9]
17	No. of Banks For Each Mem. Device	[4]	132	Header checksum	[9]
18	CAS Latencies Supported	[4]	133-145	Unit serial number	[9] [10]
19	CS# Latency	[4]	146	DIMM ID	[9] [11]
20	Write Latency	[4]	147	Checksum	[9]
21	DIMM Attributes		148-255	Reserved	[9]
22	Memory Device Attributes				
23	Min. CLK Cycle Time at CL X-1	[7]			
24	Max. Acc. Time From CLK @ CL X-1	[7]			
25	Min. CLK Cycle Time at CL X-2	[7]			
26	Max. Acc. Time From CLK @ CL X-2	[7]			

NOTES:

- [1] Programmed as 128 bytes by the DIMM OEM
- [2] Must be programmed to 256 bytes.
- [3] High order bit defines redundant addressing: if set (1), highest order RAS# address must be re-sent as highest order CAS# address.
- [4] Refer to memory manufacturer's datasheet
- [5] MSb is Self Refresh flag. If set (1), assembly supports self refresh.
- [6] Back-to-back random column addresses.
- [7] Field format proposed to JEDEC but not defined as standard at publication time.
- [8] Field specified as optional by JEDEC but required by this system.
- [9] Compaq usage. This system requires that the DIMM EEPROM have this space available for reads/writes.
- [10] Serial # in ASCII format (MSB is 133). Intended as backup identifier in case vender data is invalid. Can also be used to indicate s/n mismatch and flag system administrator of possible system Tampering.
- [11] Contains the socket # of the module (first module is "1"). Intended as backup identifier (refer to note [10]).

Figure 3-4 shows the system memory map.

Host, PCI, AGP Area	FFFF FFFFh	High BIOS Area (2 MB)	4 GB
	FFE0 0000h FFDF FFFFh	PCI Memory (18 MB)	
	FEC1 0000h FEC0 FFFFh	APIC Config. Space (64 KB)	
	FEC0 0000h FEBF FFFFh	PCI Memory Expansion (2548 MB)	
	4000 0000h 3FFF FFFFh	Host/PCI Memory Expansion (1008 MB)	
Host, PCI, ISA Area	0100 0000h	Extended Memory (15 MB)	1 GB
	00FF FFFFh		
DOS Compatibility Area	0010 0000h	System BIOS Area (64 KB)	1 MB
	000F FFFFh		
	000F 0000h 000E FFFFh	Extended BIOS Area (64 KB)	640 KB
	000E 0000h 000D FFFFh	Option ROM (128 KB)	
	000C 0000h 000B FFFFh	Graphics/SMRAM RAM (128 KB)	512 KB
	000A 0000h 0009 FFFFh	Fixed Mem. Area (128 KB)	
	0008 0000h 0007 FFFFh	Base Memory (512 KB)	512 KB
	0000 0000h		

NOTE: All locations in memory are cacheable. Base memory is always mapped to DRAM. The next 128 KB fixed memory area can, through the north bridge, be mapped to DRAM or to PCI space. Graphics RAM area is mapped to PCI or AGP locations.

Figure 3-4. System Memory Map

3.2.4 SUBSYSTEM CONFIGURATION

The 82810-DC100 GMCH component provides the configuration function for the processor/memory subsystem. Table 3-3 lists the configuration registers used for setting and checking such parameters as memory control and PCI bus operation. These registers reside in the PCI Configuration Space and accessed using the methods described in Chapter 4, section 4.2.

Table 3-3.
Host/PCI Bridge Configuration Registers (GMCH, Function 0)

PCI Config. Addr.	Register	Reset Value	PCI Config. Addr.	Register	Reset Value
00, 01h	Vender ID	8086h	6A, 6Bh	DRAM Control Reg.	00h
02, 03h	Device ID	7190h	6C..6Fh	Memory Buffer Strength	55h
04, 05h	Command	0006h	70h	Multi-Transaction Timer	00h
06, 07h	Status	0210h	71h	CPU Latency Timer	10h
08h	Revision ID	--	72h	SMRAM Control	02h
09..0Bh	Class Code	--	90h	Error Command	00h
0Dh	Latency Timer	00h	91h	Error Status Register 0	00h
0Eh	Header Type	00h	92h	Error Status Register 1	00h
10..13h	Aperture Base Config.	8	93h	Reset Control	00h
50, 51h	PAC Config. Reg.	00h	A0..A3h	AGP Capability Identifier	N/A
53h	Data Buffer Control	83h	A4..A7h	AGP Status	N/A
55..56h	DRAM Row Type	00h	A8..ABh	AGP Command	00h
57h	DRAM Control	01h	B0..B3h	AGP Control	00h
58h	DRAM Timing	00h	B4h	Aperture Size	0000h
59..5Fh	PAM 0..6 Registers	00h	B8..BBh	Aperture Translation Table	0000h
60..67h	DRAM Row Boundary	01h	BCh	Aperture I/F Timer	00h
68h	Fixed DRAM Hole	00h	BDh	Low Priority Timer	00h

NOTES:

Refer to Intel Inc. documentation for detailed description of registers.
Assume unmarked locations/gaps as reserved.

3.3 820-BASED PROCESSOR/MEMORY SUBSYSTEM

The 820-based processor/memory subsystem features an Intel Pentium III processor (in a SECC2 package) working with the Intel 82820 Memory Controller Hub (MCH) (Figure 3-5). The 82820 MCH includes a 100-/133-MHz Front Side Bus interface (FSB I/F) and an AGP interface (described in Chapter 4) that supports AGP 4X transfers with a compliant AGP graphics card. The 820-based system features Direct Rambus technology, an architecture designed to keep pace with increasing processor power and speed.

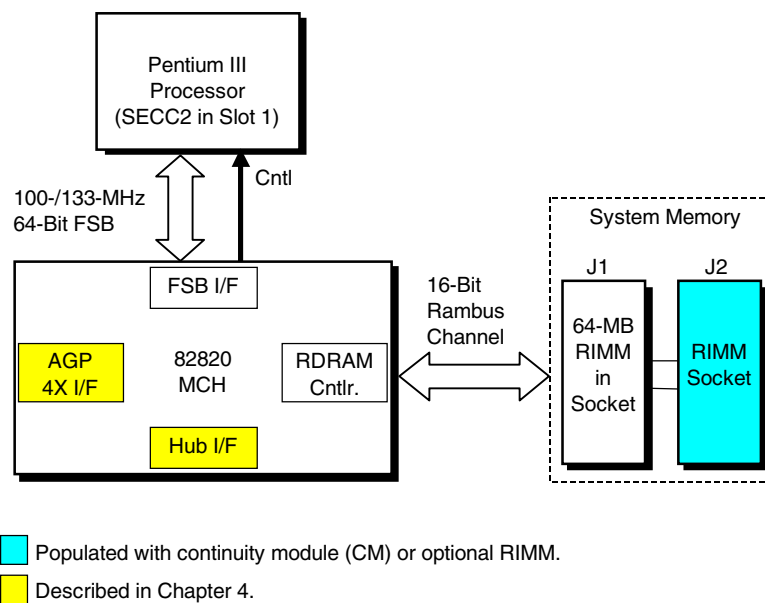


Figure 3-5. 820-Based Processor/Memory Subsystem Architecture

3.3.1 PENTIUM III PROCESSOR

The Intel Pentium III processor is packaged in a Single Edge Connector Cartridge (SECC2) that contains the microprocessor and secondary (L2) cache. The Pentium III processor is described in section 3.2.2.

3.3.2 RDRAM MEMORY

The 82820 MCH features Direct Rambus technology and in these systems supports up to two Rambus DRAM RIMMs. Direct Rambus technology provides a significant improvement in performance over DRAM/SDRAM memory designs and allows the system memory to keep pace with increasing processor performance. Rambus technology implements RDRAM devices accessed over a channel specifically designed for high speed operations.

As shown in Figure 3-6, the conventional DRAM-based memory interface with a set transfer rate of 66 or 100 MHz increases bandwidth by widening the data bus. With the current top speed of 100 MHz, a 64-bit SDRAM interface achieves a maximum throughput of 800 MB/s.

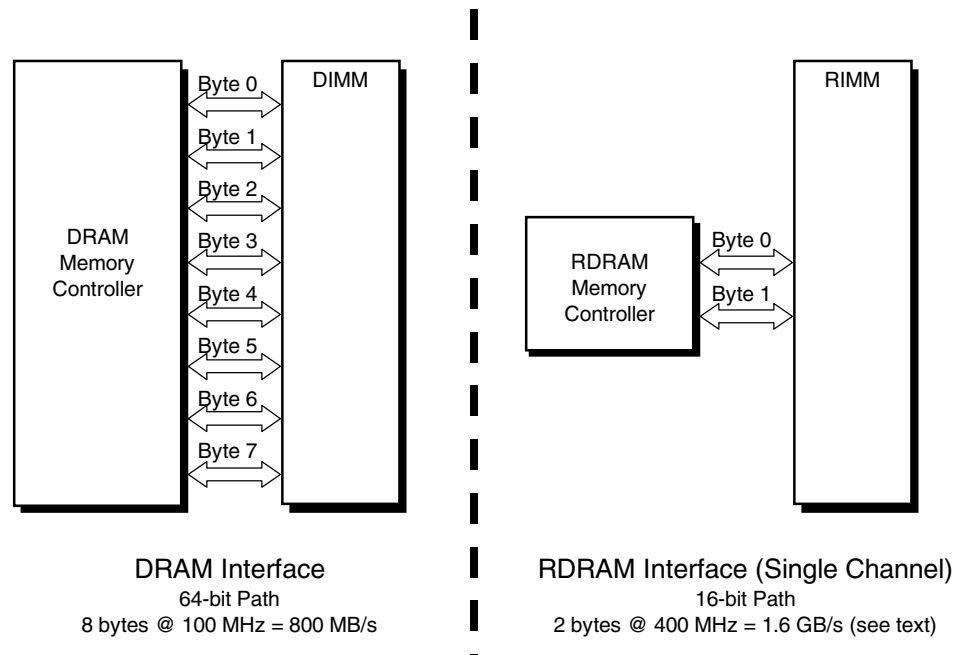


Figure 3-6. SDRAM/RDRAM Bandwidth Comparison

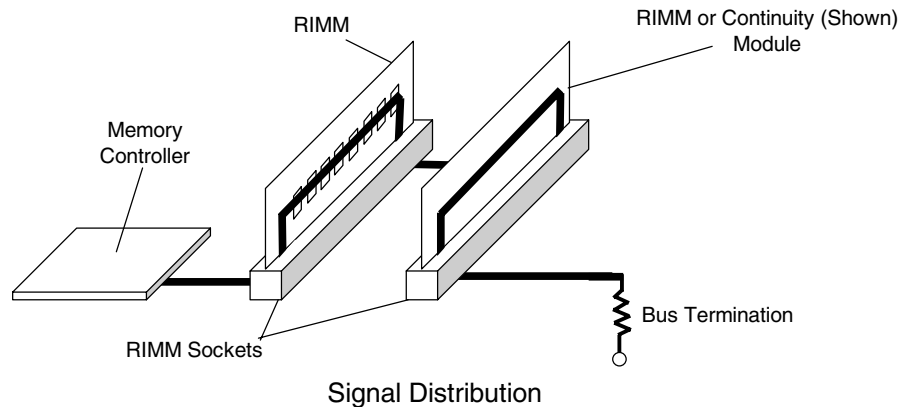
Although the Rambus channel handles only two bytes per transfer, data is clocked on both the rising and falling edges of the clock signal, allowing a 400-MHz clock to provide an effective speed of 800 MHz and resulting a throughput rate of 1.6 GB/s on the Rambus channel.

3.3.2.1 Rambus Attributes

To ensure signal quality during high-speed memory transfers, the Rambus interface design departs from previous memory interface designs in several key aspects (Figure 3-7). Unlike previous memory architectures, Rambus uses a daisy-chained signal distribution system that requires that all memory sockets be populated with either a RIMM or a continuity module in order to maintain constant load impedance. Rambus Signaling Levels (RSL) uses a 1.4-volt reference with a 0.8-volt swing between logic 0 at 1.8 V and logic 1 at 1.0 V.

Systems may employ PC600 (300 MHz), PC700 (350 MHz), or PC800 (400MHz) RIMMs. A mix of different-speed RIMMs on a channel is allowed but operation will be constrained to the speed of the slowest RIMM. A mix of ECC and non-ECC RIMMs may also be used, although all RIMMs must be ECC to realize ECC benefits.

The Rambus channel can handle a maximum load of 32 RDRAM devices (actual components or “chips”). Using 256-MB RIMMs employing 128-Mb technology with 16 RDRAM devices on each RIMM means that two RIMMs (for a total of 512 MB) will represent the maximum load capacity of the Rambus channel. Using two 512-MB RIMMs (when 256-Mb technology becomes available) will allow 1 gigabyte of memory to be installed.



Signal Name	No. of Lines	Input/Output [1]	Signal Level	Impedance	Function
ROW 2..0	3	O	RSL	28 ohms	Row address
COL 4..0	5	O	RSL	28 ohms	Column address
DQA 8..0	9	I/O	RSL	28 ohms	Data byte A (w/parity or ECC bit)
DQB 8..0	9	I/O	RSL	28 ohms	Data byte B (w/parity or ECC bit)
CFM, CFMN	2	O	RSL [2]	28 ohms	Clock-from-master for writes [3]
CTM, CTMN	2	I	RSL [2]	28 ohms	Clock-to-master for reads [3]
Vref	1	--	1.4 V	--	Reference voltage for RSL signals
SIO	1	I/O	CMOS	--	Serial I/F for initialization & pwr cntrl.
SCK	1	O	CMOS	56 ohms	SIO clock; 1 MHz for configuration, 100 MHz for power management.
CMD	1	I/O	CMOS	56 ohms	Serial I/F config. & power control
Vdd		--	2.5 V	--	Power for Rambus circuitry

NOTES:

[1] Relative to the memory controller.

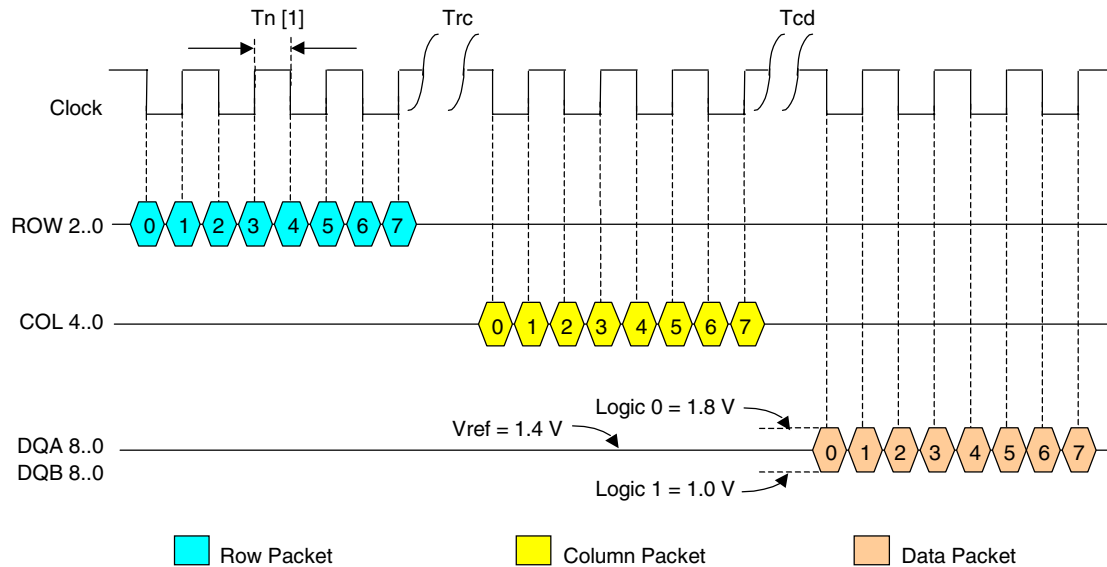
[2] Differential pair with E_p -p swing of 400 to 600 mV.

[3] 300 MHz clock for PC600 RIMM, 350 MHz clock for PC700 RIMM, 400 MHz clock for PC800 RIMM.

Figure 3–7. Key Rambus Channel Attributes

3.3.2.2 Rambus Channel Transactions

Transactions on the Rambus Channel involve packets of control (row or column) bits and packets of data bits. Each packet consists of eight segments, with even segments transferred on falling clock edges and odd segments transferred on rising clock edges. A typical operation consists of the memory controller sending out a 24-bit row packet followed by a 40-bit column packet and then the 144-bit (128-bit for non-ECC) data packet being either written to or read from RDRAM (Figure 3-8).



NOTE:

[1] $T_n = 1.25 \text{ ns @ 400 MHz (PC800)}$
 $= 1.42 \text{ ns @ 350 MHz (PC700)}$
 $= 1.66 \text{ ns @ 300 MHz (PC600)}$

Figure 3-8. Rambus Transactions

The clock signal is driven by the source device (i.e., by the memory controller during writes, by the RDRAM device during reads). The row (ROW) and column (COL) signal lines are driven only by the memory controller and assume the functions provided by the RAS/CAS signals of traditional memory buses. The ROW and COL signals are also used for power management and defining the type (read/write) of transaction. The data lines (DQAx/DQBx) are bi-directional, being driven by the controller during writes and by the RDRAM during reads. There is a specified delay period between related Row and Column packets (T_{rc} , typically 7 clock cycles) and related column and data packets (T_{cd} , typically 8 to 12 clock cycles).

Note that while Figure 3-8 illustrates a single Rambus transaction, actual operation can involve pipelined transactions where back-to-back column packets are sent followed by back-to-back data packets. A row packet may be omitted if the row to be accessed is already open. Another important characteristic is that the ROW, COL, and DQA/DQB signal lines act as independent buses and simultaneous transfers of row, column, and data information can take place.

3.3.2.3 RDRAM Power Management

The Rambus architecture provides for power management of each RDRAM device on a RIMM. RDRAM power management control is compatible with but may also work independently of ACPI. Power management of RDRAM is handled through control packets as well as the serial bus. Aside from complete “system off” state, an RDRAM may be placed in one of four basic power states:

- ◆ Active
- ◆ Standby
- ◆ Nap
- ◆ Powerdown

These states are characterized by parameters such as power consumed, refresh method, and the time required to resume full (Active state) operation. The following table defines the RDRAM power states.

State	Power Consumed [1]	Refresh Method	RDRAM CLK	Exit Latency [2]	RDRAM Functionality
Powerdown	1 mW	Self	Stopped	12 μ s	Lowest power state and condition entered after initialization. Can remain in this state indefinitely. Brought out of Powerdown only by command over the SIO serial bus.
Nap	10 mW	MCH	On	90 ns	Low power state. Can remain in this state for up to 10 μ s. Brought out of Nap only by command over the SIO serial bus.
Standby	250 mW	MCH	On	20 ns	Idle power state automatically entered after a transaction. Available to receive row packets. Transitions to Active or Nap state upon receipt of specific command on ROW bus.
Active	500 mW	MCH	On	--	Full power state. Available to receive control packets and transmit or receive data packets.

NOTES:

[1] Per RDRAM device

[2] Transition to Active state

3.3.2.4 RDRAM Configuration/Control

The Rambus architecture employs a CMOS-level serial bus (SIO, SCK, CMD) similar to that used on SDRAM-equipped systems. This bus is used for status and control of RDRAM configuration parameters as well as bringing RDRAM devices out of Powerdown and Nap states. The SIO signal is bi-directional and daisy-chained through all RDRAM devices, alternating from SIO0 to SIO1 between devices. The SCK and CMD signals are applied in parallel to all RDRAM devices. The SCK signal operates at 1 MHz during configuration and at 100 MHz when commands are issued to switch RDRAM devices from Powerdown or Nap states.

The 82820 MCH component provides the configuration function for the processor/memory subsystem. Table 3-5 lists the configuration registers used for setting and checking such parameters as memory control and PCI bus operation. These registers reside in the PCI Configuration Space and accessed using the methods described in Chapter 4, section 4.2.

Table 3-5.
Host/PCI Bridge Configuration Registers (MCH, Function 0)

PCI Config. Addr.	Register	Reset Value	PCI Config. Addr.	Register	Reset Value
00, 01h	Vender ID	8086h	90-91h	RAM/MTH Register Data	0000h
02, 03h	Device ID	2500h	94-96h	RAM Initialization Cntrl.	0's
04, 05h	Command	0066h	9Dh	SM RAMControl	02h
06, 07h	Status	--	9Eh	Ext. SMRAM Control	38h
08h	Revision ID	00h	9Fh	Power Management Cntrl.	00h
0Bh	Class Code	00h	A0, A1h	AGP Capability Identifier	0020h
0Dh	Latency Timer	00h	A2, A3h	" " "	0002h
0Eh	Header Type	00h	A4, A5h	AGP Status	1F00h
10-13h	Aperture Base Config.	8	A6, A7h	" "	0217h
40-47h	RAM Group Arch. Reg.	80h	A8-ABh	AGP Command	0's
50-52h	RAM Config. Reg.	80h	B4h	Aperture Size	00h
53h	RDRAM Pwr. Mngm.	00h	B8..BBh	Aperture Translation Table	0's
54-57h	Reserved	00h	BCh	AGP MTT Cntrl. Reg.	00h
58h	RAM Hole Cntrl.	00h	BDh	AGP Low Priority Timer Reg.	00h
59..5Fh	PAM 0..6 Registers	00h	BE, BFh	MCH Configuration	0's
60..6Fh	RAM Row Boundary		C4-CBh	Error Add./Sts/Cmd Reg.	0000h
80-87h	DRAM Throttle Control	0's	CC, CDh	SMI/SCI Error Command Reg.	0000h
88-8Ch	MCH Throttle Control	0's	DE-DFh	Scratch pad data	Xxxxh
--	--	--	E0-FFh	Reserved	0's

NOTES:

Refer to Intel Inc. documentation for detailed description of registers.
Assume unmarked locations/gaps as reserved.

The memory controller and RDRAM are configured by BIOS during POST. Refer to Chapter 8 for the configuration procedure performed by BIOS.

Chapter 4

SYSTEM SUPPORT

4.1 INTRODUCTION

This chapter covers subjects dealing with basic system architecture and covers the following topics:

- ◆ PCI bus overview (4.2) page 4-2
- ◆ AGP bus overview (4.3) page 4-10
- ◆ ISA bus overview (4.4) page 4-15
- ◆ System clock distribution (4.5) page 4-27
- ◆ Real-time clock and configuration memory (4.6) page 4-28
- ◆ System management (4.7) page 4-38
- ◆ Register map and miscellaneous functions (4.8) page 4-42

This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to Compaq Deskpro Personal Computers. For detailed information on specific components, refer to the applicable manufacturer's documentation.

4.2 PCI BUS OVERVIEW

NOTE: This section describes the PCI bus in general and highlights bus implementation in this particular system. For detailed information regarding PCI bus operation, refer to the *PCI Local Bus Specification Revision 2.2*.

This system implements a 32-bit Peripheral Component Interconnect (PCI) bus (spec. 2.2) operating at 33 MHz. The PCI bus handles address/data transfers through the identification of devices and functions on the bus. A device is typically defined as a component or slot that resides on the PCI bus (although some components such as the GMCH, MCH, and ICH are organized as multiple devices). A function is defined as the end source or target of the bus transaction. A device may contain one or more functions.

These systems use two PCI buses. The PCI bus #0 is internal to the 810/820 chipset, divided by the hub link bus, and is not physically accessible. The PCI bus #1 is used by additional interface functions and for any optional PCI expansion devices (Figure 4-1).

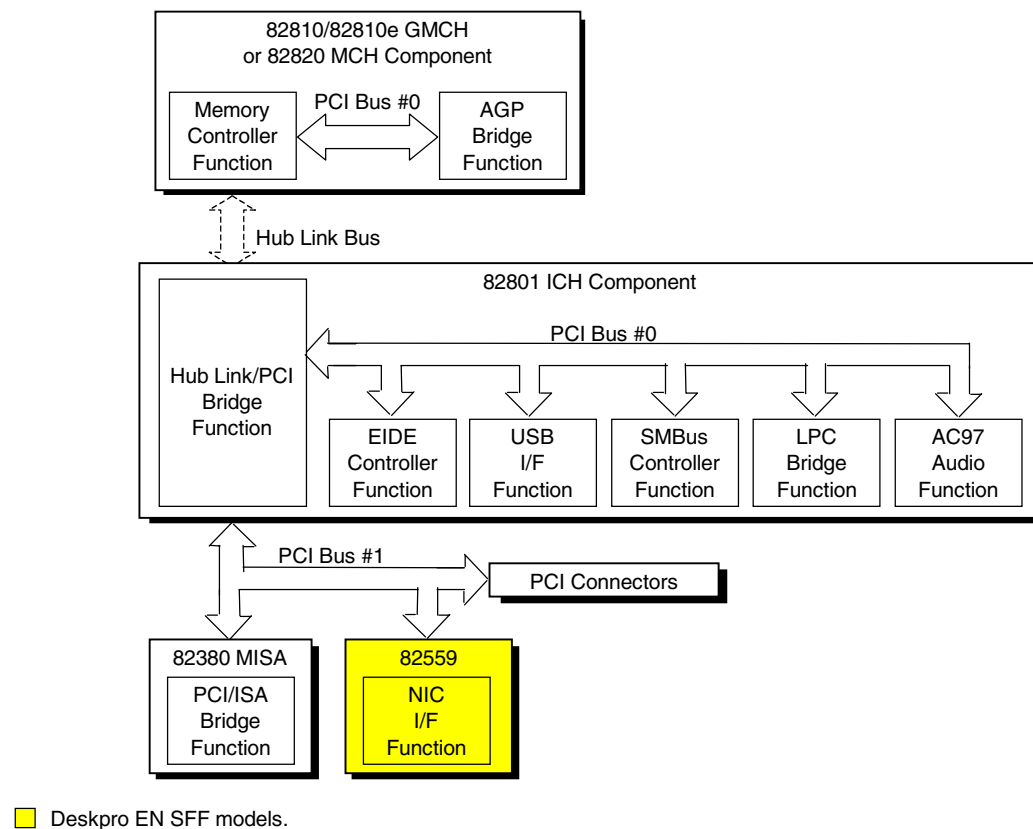


Figure 4-1. PCI Bus Devices and Functions

4.2.1 PCI BUS TRANSACTIONS

The PCI bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is realized during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing. Four types of address cycles can take place on the PCI bus; I/O, memory, configuration, and special. Address decoding is distributed (left up to each device on the PCI bus).

4.2.1.1 I/O and Memory Cycles

For I/O and memory cycles, a standard 32-bit address decode (AD31..0) for byte-level addressing is handled by the appropriate PCI device. For memory addressing, PCI devices decode the AD31..2 lines for dword-level addressing and check the AD1,0 lines for burst (linear-incrementing) mode. In burst mode, subsequent data phases are conducted a dword at a time with addressing assumed to increment accordingly (four bytes at a time).

4.2.1.2 Configuration Cycles

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.1) is employed. This method uses two 32-bit registers for initiating a configuration cycle for accessing the configuration space of a PCI device. The configuration address register (CONFIG_ADDRESS) at 0CF8h holds a value that specifies the PCI bus, PCI device, and specific register to be accessed. The configuration data register (CONFIG_DATA) at 0CFCh contains the configuration data.

PCI Configuration Address Register
I/O Port 0CF8h, R/W, (32-bit access only)

Bit	Function
31	Configuration Enable 0 = Disabled 1 = Enable
30..24	Reserved - read/write 0s
23..16	Bus Number. Selects PCI bus
15..11	PCI Device Number. Selects PCI device for access
10..8	Function Number. Selects function of selected PCI device.
7..2	Register Index. Specifies config. reg.
1,0	Configuration Cycle Type ID. 00 = Type 0 01 = Type 1

PCI Configuration Data Register
I/O Port 0CFCh, R/W, (8-, 16-, 32-bit access)

Bit	Function
31..0	Configuration Data.

Figure 4-2 shows how the loading of 0CF8h results in a Type 0 configuration cycle on the PCI bus. The Device Number (bits <15..11> determines which one of the AD31..11 lines is to be asserted high for the IDSEL signal, which acts as a “chip select” function for the PCI device to be configured. The function number (CF8h, bits <10..8>) is used to select a particular function within a PCI component.

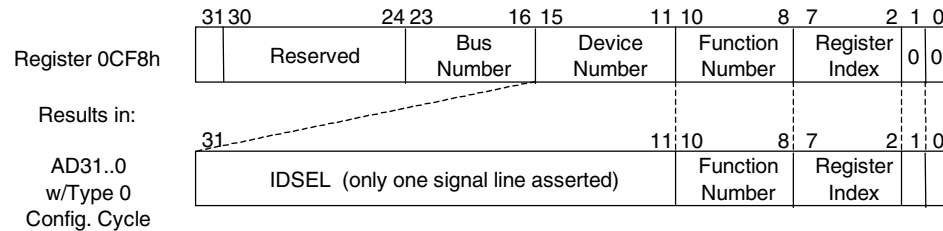


Figure 4-2. Type 0 Configuration Cycle

Type 0 configuration cycles are used for configuring devices on PCI bus # 0. Type 1 configuration cycles (reg. 0CF8h bits <1,0> = 01b) are passed on to PCI bus # 1. Table 4-1 shows the standard configuration of device numbers and IDSEL connections for components and slots residing on a PCI bus.

Table 4-1.
PCI Component Configuration Access

PCI Component	Note	Function #	Device #	PCI Bus #	IDSEL Wired to:
82810 GMCH, 82810e GMCH or 82820 MCH:					--
Memory Controller		0	0 (00h)	0	
AGP Bridge		0	1 (01h)	0	
AGP slot		0	0 (00h)	2	--
82801 ICH:					--
PCI Bridge		0	30 (1Eh)	0	
LPC Bridge		0	31 (1Fh)	0	
EIDE Controller		1	31 (1Fh)	0	
USB I/F		2	31 (1Fh)	0	
SMBus Controller		3	31 (1Fh)	0	
AC97 Audio Controller		5	31 (1Fh)	0	
AC97 Modem Controller		6	31 (1Fh)	0	
82559 Network I/F Controller	[1]	0	2 (02h)	1	AD18
82380AB ISA Bridge		0	6 (06h)	1	AD22
PCI Connector 1 (slot 1)		0	8 (08h)	1	AD24
PCI Connector 2 (slot 2)		0	9 (09h)	1	AD25
PCI Connector 3 (slot 3)	[2]	0	10 (0Ah)	1	AD26
PCI Connector 4 (slot 4)	[2]	0	11 (0Bh)	1	AD27
1394 I/F		0	12 (0Ch)	1	AD28
PCI Connector 5 (slot 5)	[2]	0	13 (0Dh)	1	AD29

NOTES:

[1] Deskpro EN SFF only.

[2] If present.

Not implemented.

The register index (CF8h, bits <7..2>) identifies the 32-bit location within the configuration space of the PCI device to be accessed. All PCI devices can contain up to 256 bytes of configuration data (Figure 4-3), of which the first 64 bytes comprise the configuration space header.

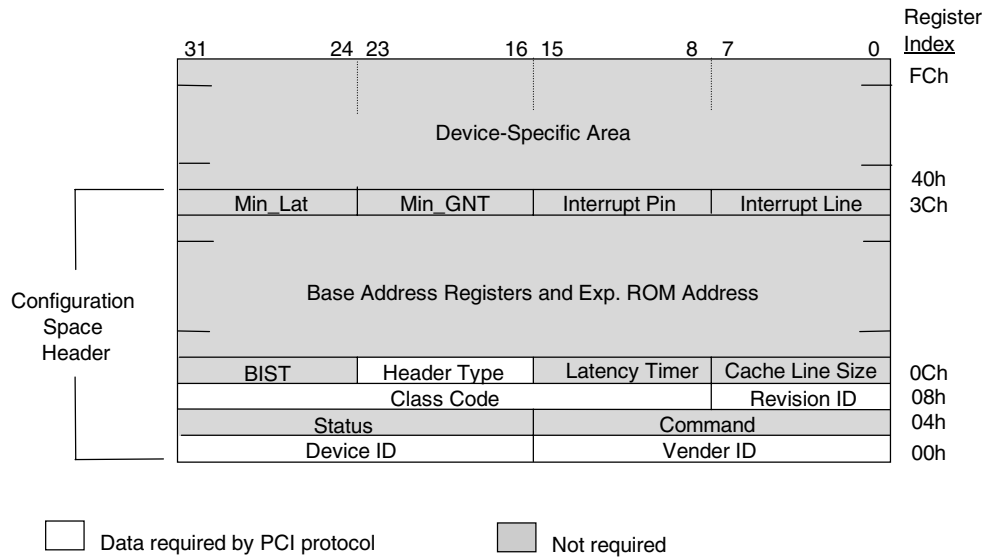


Figure 4-3. PCI Configuration Space Map

Each PCI device is identified with a vender ID (assigned to the vender by the PCI Special Interest Group) and a device ID (assigned by the vender). The device and vender IDs for the devices on the system board are listed in Table 4-2.

Table 4-2. System Board PCI Device Identification		
PCI Device	Vender ID	Device ID
8281082810e GMCH or 82820 MCH:		
Memory Controller	8086h	2500h
AGP Bridge	8086h	2501h
82801 ICH:		
PCI Bridge	8086h	2418h
LPC Bridge	8086h	2410h
EIDE Controller	8086h	2411h
USB I/F	8086h	2412h
SMBus Controller	8086h	2413h
AC97 Audio Controller	8086h	2415h
82559 Network I/F Controller	8086h	1229h
82380AB ISA Bridge	8086h	

4.2.2 PCI BUS MASTER ARBITRATION

The PCI bus supports a bus master/target arbitration scheme. A bus master is a device that has been granted control of the bus for the purpose of initiating a transaction. A target is a device that is the recipient of a transaction. The Request (REQ), Grant (GNT), and FRAME signals are used by PCI bus masters for gaining access to the PCI bus. When a PCI device needs access to the PCI bus (and does not already own it), the PCI device asserts its REQ n signal to the PCI bus arbiter (a function of the system controller component). If the bus is available, the arbiter asserts the GNT n signal to the requesting device, which then asserts FRAME and conducts the address phase of the transaction with a target. If the PCI device already owns the bus, a request is not needed and the device can simply assert FRAME and conduct the transaction. Table 4-3 shows the grant and request signals assignments for the devices on the PCI bus.

Table 4-3.
PCI Bus Mastering Devices

REQ/GNT Line	Device
REQA/GNTA	82360 or ITE 8889 ISA Bridge
REQ0/GNT0	PCI Connector Slot 1
REQ1/GNT1	PCI Connector Slot 2
REQ2/GNT2	82559 NIC [1] / PCI Connector Slot 3 [2]
REQ3/GNT3	PCI Connector Slot 4 [2]
REQ4/GNT4	PCI Connector Slot 5 [2]
GREQ/GGNT	AGP Slot [3]

NOTE:

[1] Deskpro EN SFF models only.

[2] If present.

[3] 820 chipset-based systems only.

PCI bus arbitration is based on a round-robin scheme that complies with the fairness algorithm specified by the PCI specification. The bus parking policy allows for the current PCI bus owner (excepting the PCI/ISA bridge) to maintain ownership of the bus as long as no request is asserted by another agent. Note that most CPU-to-DRAM and AGP-to-DRAM accesses can occur concurrently with PCI traffic, therefore reducing the need for the Host/PCI bridge to compete for PCI bus ownership.

4.2.3 OPTION ROM MAPPING

During POST, the PCI bus is scanned for devices that contain their own specific firmware in ROM. Such option ROM data, if detected, is loaded into system memory's DOS compatibility area (refer to the system memory map shown in chapter 3).

4.2.4 PCI INTERRUPT MAPPING

The PCI bus provides for four interrupt signals; INTA-, INTB-, INTC-, and INTD-. These signals may be generated by on-board PCI devices or by devices installed in the PCI slots. In order to minimize latency, INTx- signal routing from the interrupt controller of the ICH to PCI slots/devices is distributed evenly as shown below:

Intr. Cntlr.	PCI Slot 1	PCI Slot 2	PCI Slot 3	PCI Slot 4	PCI Slot 5	AGP Slot	1394 I/F	NIC I/F	USB I/F
INTA-	INTA-	INTB-	INTC-	INTD-	INTA-	--	--	--	--
INTB-	INTB-	INTC-	INTD-	INTA-	INTB-	--	INTB-	--	--
INTC-	INTC-	INTD-	INTA-	INTB-	INTC-	INTA-	--	INTA-	--
INTD-	INTD-	INTA-	INTB-	INTC-	INTD-	INTB-	--	--	INTA-

NOTES:

PCI Slots 3 and up may not be present depending on system.

Interrupts generated by PCI devices can be configured to share the standard AT (IRQn) interrupt lines.

Two devices that share a single PCI interrupt must also share the corresponding AT interrupt.

4.2.5 PCI POWER MANAGEMENT SUPPORT

This system complies with the PCI Power Management Interface Specification (rev 1.0). The PCI Power Management Enable (PME-) signal is supported by the 810 and 820 chipsets and allows compliant PCI and AGP peripherals to initiate the power management routine.

4.2.6 PCI SUB-BUSSES

The 810, 810e, and 820 chipsets implement two data busses that are supplementary in operation to the PCI bus:

- ◆ Hub Link Bus
- ◆ LPC Bus

4.2.6.1 Hub Link Bus

The 810, 810e, and 820 chipsets implement a Hub Link bus between the GMCH/MCH and the ICH. The Hub Link bus handles transactions at a 66-MHz rate using PCI-type protocol. This bus is transparent to software and not accessible for expansion purposes.

4.2.6.2 LPC Bus

The 82801 ICH implements a Low Pin Count (LPC) bus for handling transactions to and from the 47B347 Super I/O Controller as well as the 82802 FWH. The LPC bus transfers data a nibble (4 bits) at a time at a 33-MHz rate. Generally transparent in operation, the LPC bus becomes a factor primarily during the configuration of DMA channel modes (see section 4.4.3 “DMA”).

4.2.7 PCI CONFIGURATION

PCI bus operations, especially those that involve ISA bus interaction, require the configuration of certain parameters such as PCI IRQ routing, DMA channel configuration, RTC control, port decode ranges, and firmware hub (FWH) access control. These parameters are handled by the LPC I/F bridge function (PCI function #0, device 31) of the ICH component and configured through the PCI configuration space registers listed in Table 4-4. Configuration is provided by BIOS at power-up but re-configurable by software.

Table 4-4.
LPC Bridge Configuration Registers
(ICH, Function 0, Device 31)

PCI Config.			PCI Config.		
Addr.	Register	Reset Value	Addr.	Register	Reset Value
00, 01h	Vender ID	8086h	88h	Device 31 Error Config.	00h
02, 03h	Device ID	2410h	8Ah	Device 31 Error Status	00h
04, 05h	Command	000Fh	90, 91h	PCI DMA Configuration	0000h
06, 07h	Status	0280h	A0-CFh	Power Management	
08h	Revision ID	00h	D0-D3h	General Control	0's
09-0Bh	Class Code	00h	D4-D7h	General Status	F00h
0Eh	Header Type	01h	D8h	RTC Configuration	00h
40-43hh	ACPI Base Address	1	E1h	COM Port Decode Range	00h
44h	ACPI Control	00h	E2h	DD & LPT Port Dec. Range	00h
4E, 4Fh	BIOS Control	0000h	E3h	FWH Decode Enable	80h
54h	TCO Control	80h	E4, E5h	LPC I/F Decode Range 1	0000h
58-5Bh	GPIO Base Address	1	E6, E7h	LPC I/F Enables	0000h
5Ch	GPIO Control	00h	E8h	FWH Select	
60-63h	PCI IRQ Routing Cntrl.	80h	EC, EDh	LPC I/F Decode Range 2	0000h
64h	Serial IRQ Control	10h	F2, F3h	Functions Disable	00

NOTE: Assume unmarked locations/gaps as reserved.

4.2.8 PCI CONNECTOR

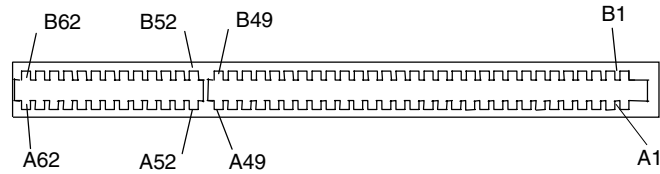


Figure 4-4. PCI Bus Connector (32-Bit Type)

Table 4-5.
PCI Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	-12 VDC	TRST-	32	AD17	AD16
02	TCK	+12 VDC	33	C/BE2-	+3.3 VDC
03	GND	TMS	34	GND	FRAME-
04	TDO	TDI	35	IRDY-	GND
05	+5 VDC	+5 VDC	36	+3.3 VDC	TRDY-
06	+5 VDC	INTA-	37	DEVSEL-	GND
07	INTB-	INTC-	38	GND	STOP-
08	INTD-	+5 VDC	39	LOCK-	+3.3 VDC
09	PRSENT1-	Reserved	40	PERR-	SDONE n
10	RSVD	+5 VDC	41	+3.3 VDC	SBO-
11	PRSENT2-	Reserved	42	SERR-	GND
12	GND	GND	43	+3.3 VDC	PAR
13	GND	GND	44	C/BE1-	AD15
14	RSVD	+3.3 AUX	45	AD14	+3.3 VDC
15	GND	RST-	46	GND	AD13
16	CLK	+5 VDC	47	AD12	AD11
17	GND	GNT-	48	AD10	GND
18	REQ-	GND	49	GND	AD09
19	+5 VDC	PME-	50	Key	Key
20	AD31	AD30	51	Key	Key
21	AD29	+3.3 VDC	52	AD08	C/BE0-
22	GND	AD28	53	AD07	+3.3 VDC
23	AD27	AD26	54	+3.3 VDC	AD06
24	AD25	GND	55	AD05	AD04
25	+3.3 VDC	AD24	56	AD03	GND
26	C/BE3-	IDSEL	57	GND	AD02
27	AD23	+3.3 VDC	58	AD01	AD00
28	GND	AD22	59	+5 VDC	+5 VDC
29	AD21	AD20	60	ACK64-	REQ64-
30	AD19	GND	61	+5 VDC	+5 VDC
31	+3.3 VDC	AD18	62	+5 VDC	+5 VDC
--	--	--	--	--	--

4.3 AGP BUS OVERVIEW

NOTE: Systems based on the 810 or 810e chipset feature an AGP 2X graphics adapter that is wholly integrated into the GMCH component making the AGP bus transparent (i.e., unaccessible). Systems based on the 820 chipset provide full AGP 4X support (with a compliant graphics controller) although the 820-based Deskpro EN SFF does not include an AGP slot. For a detailed description of AGP bus operations refer to the *AGP Interface Specification* available at the following AGP forum web site:
<http://www.agpforum.org/index.htm>

The Accelerated Graphics Port (AGP) bus is specifically designed as an economical yet high-performance interface for graphics adapters, especially those designed for 3D operations. The AGP interface is designed to give graphics adapters dedicated pipelined access to system memory for the purpose of off-loading texturing, z-buffering, and alpha blending used in 3D graphics operations. By off-loading a large portion of 3D data to system memory the AGP graphics adapter only requires enough memory for frame buffer (display image) refreshing.

4.3.1 BUS TRANSACTIONS

The operation of the AGP bus is based on the 66-MHz PCI specification but includes additional mechanisms to increase bandwidth. During the configuration phase the AGP bus acts in accordance with PCI protocol. Once graphics data handling operation is initiated, AGP-defined protocols take effect. The AGP graphics adapter acts generally as the AGP master, but can also behave as a “PCI” target during fast writes from the GMCH or MCH.

Key differences between the AGP interface and the PCI interface are as follows:

- ◆ Address phase and associated data transfer phase are disconnected transactions. Addressing and data transferring occur as contiguous actions on the PCI bus. On the AGP bus a request for data and the transfer of data may be separated by other operations.
- ◆ Commands on the AGP bus specify system memory accesses only. Unlike the PCI bus, commands involving I/O and configuration are not required or allowed. The system memory address space used in AGP operations is the same linear space used by PCI memory space commands, but is further specified by the graphics address re-mapping table (GART) of the north bridge component.
- ◆ Data transactions on the AGP bus involve eight bytes or multiples of eight bytes. The AGP memory addressing protocol uses 8-byte boundaries as opposed to PCI’s 4-byte boundaries. If a transfer of less than eight bytes is needed, the remaining bytes are filled with arbitrary data that is discarded by the target.
- ◆ Pipelined requests are defined by length or size on the AGP bus. The PCI bus defines transfer lengths with the FRAME- signal.

There are two basic types of transactions on the AGP bus: data requests (addressing) and data transfers. These actions are separate from each other.

4.3.1.1 Data Request

Requesting data is accomplished in one of two ways; either multiplexed addressing (using the AD lines for addressing/data) or demultiplexed (“sideband”) addressing (using the SBA lines for addressing only and the AD lines for data only). Even though there are only eight SBA lines (as opposed to the 32 AD lines) sideband addressing maximizes efficiency and throughput by allowing the AD lines to be exclusively used for data transfers. Sideband addressing occurs at the same rate (1X, 2X, or 4X) as data transfers. The differences in rates will be discussed in the next section describing data transfers. Note also that sideband addressing is limited to 48 bits (address bits 48-63 are assumed zero). The GMCH and MCH components support both SBA and AD addressing, but the method and rate is selected by the AGP graphics adapter.

4.3.1.2 Data Transfers

Data transfers use the AD lines and occur as the result of data requests described previously. Each transaction resulting from a request involves at least eight bytes, requiring the 32 AD lines to handle at least two transfers per request. The 82820 MCH supports three transfer rates: 1X, 2X, and 4X. Regardless of the rate used, the speed of the bus clock is constant at 66 MHz. The following subsections describe how the use of additional strobe signals makes possible higher transfer rates.

AGP 1X Transfers

During a AGP 1X transfer the 66-MHz CLK signal is used to qualify the control and data signals. Each 4-byte data transfer is synchronous with one CLK cycle so it takes two CLK cycles for a minimum 8-byte transfer (Figure 4-5 shows two 8-byte transfers). The GNT- and TRDY- signals retain their traditional PCI functions. The ST0..3 signals are used for priority encoding, with “000” for low priority and “001” indicating high priority. The signal level for AGP 1X transfers may be 3.3 or 1.5 VDC.

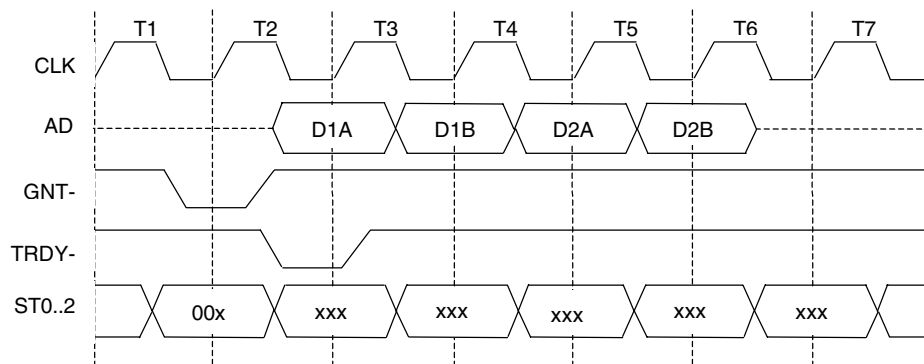


Figure 4-5. AGP 1X Data Transfer (Peak Transfer Rate: 266 MB/s)

AGP 2X Transfers

During AGP 2X transfers, clocking is basically the same as in 1X transfers except that the 66-MHz CLK signal is used to qualify only the control signals. The data bytes are latched by an additional strobe (AD_STBx) signal so that an 8-byte transfer occurs in one CLK cycle (Figure 4-6). The first four bytes (DnA) are latched by the receiving agent on the falling edge of AD_STBx and the second four bytes (DnB) are latched on the rising edge of AD_STBx. The signal level for AGP 2X transfers may be 3.3 or 1.5 VDC.

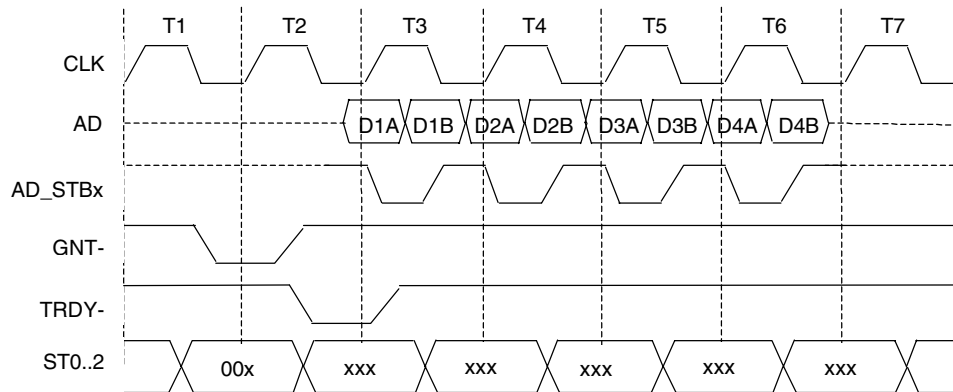


Figure 4-6. AGP 2X Data Transfer (Peak Transfer Rate: 532 MB/s)

AGP 4X Transfers

The AGP 4X transfer rate allows sixteen bytes of data to be transferred in one clock cycle. As in 2X transfers the 66-MHz CLK signal is used only for qualifying control signals while strobe signals are used to latch each 4-byte transfer on the AD lines. As shown in Figure 4-7, 4-byte block DnA is latched by the falling edge of AD_STBx while DnB is latched by the falling edge of AD_STBx-. The signal level for AGP 4X transfers is 1.5 VDC.

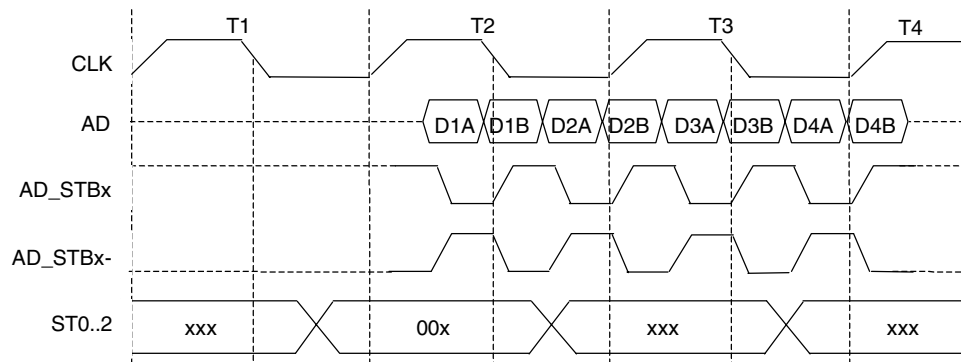


Figure 4-7. AGP 4X Data Transfer (Peak Transfer Rate: 1064 MB/s)

4.3.2 AGP CONFIGURATION

AGP bus operations require the configuration of certain parameters involving system memory access by the AGP graphics adapter. The AGP bus interface is configured as a PCI device integrated within the north bridge (MCH, device 1) component. The AGP function is, from the PCI bus perspective, treated essentially as a PCI/PCI bridge and configured through PCI configuration registers (Table 4-6). Configuration is accomplished by BIOS during POST.

NOTE: Configuration of the AGP bus interface involves functions 0 and 1 of the MCH. Function 0 registers (listed in Table 3-4) include functions that affect basic control (GART) of the AGP.

Table 4-6.
PCI/AGP Bridge Function Configuration Registers
(MCH, Function 1)

PCI Config. Addr.	Register	Reset Value	PCI Config. Addr.	Register	Reset Value
00, 01h	Vender ID	8086h	1Bh	Sec. Master Latency Timer	00h
02, 03h	Device ID	7191h	1Ch	I/O Base Address	F0h
04, 05h	Command	0000h	1Dh	I/O Limit Address	00h
06, 07h	Status	0220h	1E, 1Fh	Sec. PCI/PCI Status	02A0h
08h	Revision ID	00h	20, 21h	Memory Base Address	FFF0h
0A, 0Bh	Class Code	0406h	22, 23h	Memory Limit Address	0000h
0Eh	Header Type	01h	24, 25h	Prefetch Mem. Base Addr.	FFF0h
18h	Primary Bus Number	00h	26, 27h	Prefetch Mem. Limit Addr.	0000h
19h	Secondary Bus Number	00h	3Eh	PCI/PCI Bridge Control	80h
1Ah	Subordinate Bus Number	00h	3F-FFh	Reserved	00h

NOTE:

Assume unmarked locations/gaps as reserved. Refer to Intel documentation for detailed register descriptions.

The AGP graphics adapter (actually its resident controller) is configured as a standard PCI device.

4.3.3 AGP CONNECTOR

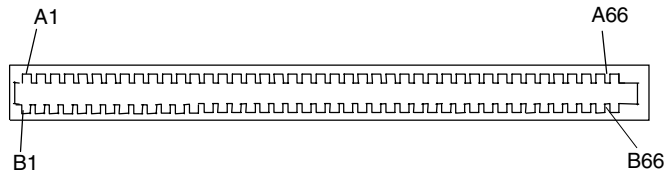


Figure 4-8. Universal AGP Bus Connector

Table 4-7.
AGP Bus Connector Pinout

Pin	A Signal	B Signal	Pin	A Signal	B Signal	Pin	A Signal	B Signal
01	+12 VDC	OVRcnt-	23	GND	GND	45	VDD3	VDD3
02	Type Det-	VDD	24	NC	VDD3 Aux	46	TRDY-	DEVSEL-
03	NC	VDD	25	VDD3	VDD3	47	STOP-	VDDQ
04	USBN	USBP	26	PAD30	PAD31	48	PME-	PERR-
05	GND	GND	27	PAD28	PAD29	49	GND	GND
06	INTA-	INTB-	28	VDD3	VDD3	50	PAR	SERR-
07	RESET	CLK	29	PAD26	PAD27	51	PAD15	CBE1-
08	GNT-	REQ-	30	PAD24	PAD25	52	VDDQ	VDDQ
09	VDD3	VDD3	31	GND	GND	53	PAD13	PAD14
10	ST1	ST0	32	AD_STB1-	AD_STB1	54	PAD11	PAD12
11	NC	ST2	33	CBE3-	PAD23	55	GND	GND
12	PIPE-	RBF-	34	VDDQ	VDDQ	56	PAD09	PAD10
13	GND	GND	35	PAD22	PAD21	57	CBE0-	PAD08
14	WBF-	NC	36	PAD20	PAD19	58	VDDQ	VDDQ
15	SBA1	SBA0	37	GND	GND	59	AD_STB0-	AD_STB0
16	VDD3	VDD3	38	PAD18	PAD17	60	PAD06	PAD07
17	SBA3	SBA2	39	PAD16	CBE2-	61	GND	GND
18	SB_STB-	SB_STB	40	VDDQ	VDDQ	62	PAD04	PAD05
19	GND	GND	41	FRAME-	IRDY-	63	PAD02	PAD03
20	SBA5	SBA4	42	NC	VDD3 Aux	64	VDDQ	VDDQ
21	SBA7	DBA6	43	GND	GND	65	PAD00	PAD01
22	NC	NC	44	NC	NC	66	VREFGC	VREFGC

NOTES;

NC = Not connected

VDDQ = 3.3 VDC when TYPE DET- is left open by AGP 1X/2X card.

VDDQ = 1.5 VDC when TYPE DET- is grounded by AGP 4X card.

4.4 ISA BUS OVERVIEW

NOTE: This section describes the ISA bus in general and highlights bus implementation in this particular system. For detailed information regarding ISA bus operation, refer to the *Compaq Extended Industry Standard Architecture (EISA) Technical Reference Guide*.

The industry standard architecture (ISA) bus provides an 8-/16-bit path for standard I/O peripherals as well as for optional devices that can be installed in the ISA expansion slots. Figure 4-8 shows the key functions and devices that reside on the ISA bus.

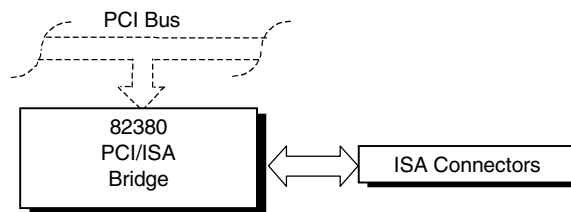


Figure 4-9. ISA Bus Block Diagram

4.4.1 ISA CONNECTOR

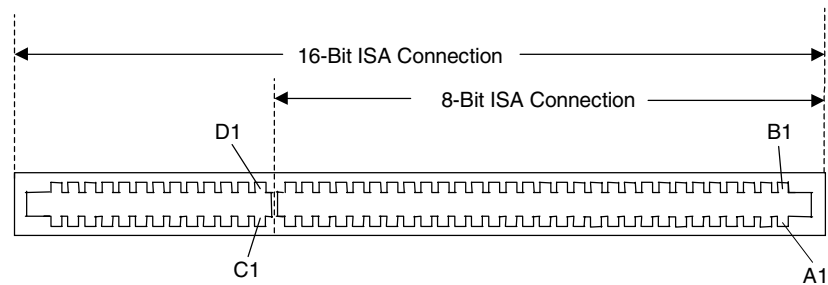


Figure 4-10. ISA Expansion Connector

Table 4-8.
ISA Expansion Connector Pinout

16-Bit ISA Interface			
8-Bit ISA Interface			
Pin	Signal	Pin	Signal
B01	GND	A01	I/O CHK-
B02	RESDRV	A02	SD7
B03	+5 VDC	A03	SD6
B04	IRQ9	A04	SD5
B05	-5 VDC	A05	SD4
B06	DRQ2	A06	SD3
B07	-12 VDC	A07	SD2
B08	NOWS-	A08	SD1
B09	+12 VDC	A09	SD0
B10	GND	A10	BUSRDY
B11	SMWTC-	A11	DMA
B12	SMRDC-	A12	SA19
B13	IOWC-	A13	SA18
B14	IORC-	A14	SA17
B15	DAK3-	A15	SA16
B16	DRQ3	A16	SA15
B17	DAK1	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH-	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DAK2-	A26	SA5
B27	T-C	A27	SA4
B28	BALE	A28	SA3
B29	+5 VDC	A29	SA2
B30	OSC	A30	SA1
B31	GND	A31	SA0
		D01	M16-
		D02	I/O16-
		D03	IRQ10
		D04	IRQ11
		D05	IRQ12
		D06	IRQ15
		D07	IRQ14
		D08	DAK0-
		D09	DRQ0
		D10	DAK5-
		D11	DRQ5
		D12	DAK6-
		D13	DRQ6
		D14	DAK7-
		D15	DRQ7
		D16	+5 VDC
		D17	GRAB-
		D18	GND
		C01	SBHE-
		C02	LA23
		C03	LA22
		C04	LA21
		C05	LA20
		C06	LA19
		C07	LA18
		C08	LA17
		C09	MRDC-
		C10	MWTC-
		C11	SD8
		C12	SD9
		C13	SD10
		C14	SD11
		C15	SD12
		C16	SD13
		C17	SD14
		C18	SD15

4.4.2 ISA BUS TRANSACTIONS

The ISA bus supports 8- and 16-bit transfers at an 8-MHz rate. Devices limited to 8-bit transfers use the lower byte portion (data lines 7..0) while 16-bit transfers use the full bandwidth (data lines 15..0). Addressing is handled by two classifications of address signals: latched and latching. Latched address signals (SA19..0) select the specific byte within the 1-MB section of memory defined by address lines LA23..17. Latching address lines (LA23..17) provide a longer setup time for pre-chip selection or for pre-address decoding for high-speed memory and allow access to up to 16 megabytes of physical memory on the ISA bus. The SA19..17 signals have the same values as the LA19..17 signals for all memory cycles. The I/O cycles use only the SA15..0 signals.

The key control signals are described as follows:

- ◆ MRDC- (Memory Read Cycle): MRDC- is active on all ISA memory reads accessing memory from 000000h to FFFFFFFh.
- ◆ SMEMR- (System Memory Read): SMEMR- is asserted by the PCI/ISA bridge to request an ISA memory device to drive data onto the data lines for accesses below one megabyte. SMEMR- is a delayed version of MRDC-.
- ◆ MWTC- (Memory Write Cycle): MWTC- is active on all ISA memory write cycles accessing memory from 000000h to FFFFFFFh.
- ◆ SMEMW- (System Memory Write): SMEMW- is asserted by the PCI/ISA bridge to request an ISA memory device to accept data from the data lines for access below one megabyte. SMEMW- is a delayed version of MWTC-.
- ◆ IORC- (Input/Output Read Cycle): IORC- commands an ISA I/O device to drive data onto the data lines.
- ◆ IOWC- (Input/Output Write Cycle): IOWC- commands an ISA I/O device to accept data from the data lines.
- ◆ SBHE- (System Byte High Enable): SBHE- indicates that a byte is being transferred on the upper half (D15..8) of the data lines.
- ◆ SA0- (System Address Bit <0>): This bit is the complement of SBHE- and indicates that a byte is being transferred on the lower half (D7..0) of the data lines.
- ◆ M16- (16-bit Memory Cycle): M16- is asserted by 16-bit ISA devices to indicate 16-bit memory cycle capability.
- ◆ IO16- (16-bit I/O Cycle): IO16- is asserted by 16-bit ISA devices to indicate 16-bit I/O cycle transfer capability.

If the address on the SA lines is above one megabyte, SMRDC- and SMWTC- will not be active. The MRDC- and MWTC- signals are active for memory accesses up to 16 megabytes and can be used by any device that uses the full 16-bit ISA bus. To request a 16-bit transfer, a device asserts either the M16- (memory) or IO16- (I/O) signal when the device is addressed.

When another device (such as a DMA device or another bus master) takes control of the ISA, the Bus Address Latch Enable (BALE) signal is held active for the duration of the operation. As a result, signals LA23..17 are always enabled and must be held stable for the duration of each bus cycle.

When the address changes, devices on the bus may decode the latchable address (LA23..17) lines and then latch them. This arrangement allows devices to decode chip selects and M16- before the next cycle actually begins.

The following guidelines apply to optional ISA devices installed in the system:

- ◆ On bus lines that can be driven by a controller board, the driver should be able to sink a minimum of 20 ma at 0.5 VDC and source 2 ma at 3.75 VDC.
- ◆ On bus lines that are driven in the low direction only (open collector), the driver should be able to sink 20 ma at 0.5 VDC.
- ◆ The load on any logic line from a single bus slot should not exceed 2.0 ma in the low state (at 0.5 VDC) or 0.1 ma in the high state (at 3.75 VDC).
- ◆ The logic-high voltage at the bus ranges from 3.75 VDC to 5.5 VDC. The logic low voltage ranges from 0 VDC to 0.8 VDC.

4.4.3 DIRECT MEMORY ACCESS

Direct Memory Access (DMA) is a method by which a device accesses system memory without involving the microprocessor. Although the DMA method is normally used to transfer blocks of data to or from an ISA I/O device, PCI devices may also use DMA operation as well. The DMA method reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

NOTE: This section describes DMA in general. For detailed information regarding DMA operation, refer to the data manual for the Intel 82801AA I/O Controller Hub.

The 82801 ICH component includes the equivalent of two 8237 DMA controllers cascaded together to provide eight DMA channels, each (excepting channel 4) configurable to a specific device. Table 4-9 lists the default configuration of the DMA channels.

Table 4-9.
Default DMA Channel Assignments

DMA Channel	Device ID
Controller 1 (byte transfers)	
0	Spare & ISA conn. pins D8, D9
1	Audio subsystem & ISA conn. pins B17, B18
2	Diskette drive & ISA conn. pins B6, B26
3	ECP LPT1 & ISA conn. pins B15, B16
Controller 2 (word transfers)	
4	Cascade for controller 1
5	Spare & ISA conn. pins D10, D11
6	Spare & ISA conn. pins D12, D13
7	Spare & ISA conn. pins. D14, D15

All channels in DMA controller 1 operate at a higher priority than those in controller 2. Note that channel 4 is not available for use other than its cascading function for controller 1. The DMA controller 2 can transfer words only on an even address boundary. The DMA controller and page register define a 24-bit address that allows data transfers within the address space of the CPU.

In addition to device configuration, each channel can be configured (through PCI Configuration Registers) for one of two modes of operation:

- ◆ LPC DMA
- ◆ PC/PCI DMA

The LPC DMA mode uses the LPC bus to communicate DMA channel control and is implemented for devices using DMA through the LPC47B347 I/O controller such as the diskette drive controller.

The PC/PCI DMA mode uses the REQ#/GNT# signals to communicate DMA channel control and should be set for any ISA expansion slot devices since they operate through the PCI/ISA bridge device, which requires PC/PCI DMA protocol.

The DMA logic is accessed through two types of I/O mapped registers; page registers and controller registers.

4.4.3.1 DMA Page Registers

The DMA page register contains the eight most significant bits of the 24-bit address and works in conjunction with the DMA controllers to define the complete (24-bit) address for the DMA channels. Table 4-10 lists the page register port addresses.

Table 4-10. DMA Page Register Addresses	
DMA Channel	Page Register I/O Port
Controller 1 (byte transfers)	
Ch 0	087h
Ch 1	083h
Ch 2	081h
Ch 3	082h
Controller 2 (word transfers)	
Ch 4	n/a
Ch 5	08Bh
Ch 6	089h
Ch 7	08Ah
Refresh	08Fh [see note]

NOTE:

The DMA memory page register for the refresh channel must be programmed with 00h for proper operation.

The memory address is derived as follows:

24-Bit Address - Controller 1 (Byte Transfers)

<u>8-Bit Page Register</u>	<u>8-Bit DMA Controller</u>
A23..A16	A15..A00

24-Bit Address - Controller 2 (Word Transfers)

<u>8-Bit Page Register</u>	<u>16-Bit DMA Controller</u>
A23..A17	A16..A01, (A00 = 0)

Note that address line A16 from the DMA memory page register is disabled when DMA controller 2 is selected. Address line A00 is not connected to DMA controller 2 and is always 0 when word-length transfers are selected.

By not connecting A00, the following applies:

- ◆ The size of the the block of data that can be moved or addressed is measured in 16-bits (words) rather than 8-bits (bytes).
- ◆ The words must always be addressed on an even boundary.

DMA controller 1 can move up to 64 Kbytes of data per DMA transfer. DMA controller 2 can move up to 64 Kwords (128 Kbytes) of data per DMA transfer. Word DMA operations are only possible between 16-bit memory and 16-bit peripherals.

The RAM refresh is designed to perform a memory read cycle on each of the 512 row addresses in the DRAM memory space. Refresh operations are used to refresh memory on the 32-bit memory bus and the ISA bus. The refresh address is provided on lines SA00 through SA08. Address lines LA23..17, SA18,19 are driven low.

The remaining address lines are in an undefined state during the refresh cycle. The refresh operations are driven by a 69.799-KHz clock generated by Interval Timer 1, Counter 1. The refresh rate is 128 refresh cycles in 2.038 ms.

4.4.3.2 DMA Controller Registers

Table 4-11 lists the DMA Controller Registers and their I/O port addresses. Note that there is a set of registers for each DMA controller.

Table 4-11.
DMA Controller Registers

Register	Controller 1	Controller 2	R/W
Status	008h	0D0h	R
Command	008h	0D0h	W
Mode	00Bh	0D6h	W
Write Single Mask Bit	00Ah	0D4h	W
Write All Mask Bits	00Fh	0DEh	W
Software DRQx Request	009h	0D2h	W
Base and Current Address - Ch 0	000h	0C0h	W
Current Address - Ch 0	000h	0C0h	R
Base and Current Word Count - Ch 0	001h	0C2h	W
Current Word Count - Ch 0	001h	0C2h	R
Base and Current Address - Ch 1	002h	0C4h	W
Current Address - Ch 1	002h	0C4h	R
Base and Current Word Count - Ch 1	003h	0C6h	W
Current Word Count - Ch 1	003h	0C6h	R
Base and Current Address - Ch 2	004h	0C8h	W
Current Address - Ch 2	004h	0C8h	R
Base and Current Word Count - Ch 2	005h	0CAh	W
Current Word Count - Ch 2	005h	0CAh	R
Base and Current Address - Ch 3	006h	0CCh	W
Current Address - Ch 3	006h	0CCh	R
Base and Current Word Count - Ch 3	007h	0CEh	W
Current Word Count - Ch 3	007h	0CEh	R
Temporary (Command)	00Dh	0DAh	R
Reset Pointer Flip-Flop (Command)	00Ch	0D8h	W
Master Reset (Command)	00Dh	0DAh	W
Reset Mask Register (Command)	00Eh	0DCh	W

4.4.4 INTERRUPTS

The microprocessor uses two types of interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor but may be inhibited by hardware or software means external to the microprocessor.

4.4.4.1 Maskable Interrupts

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Peripheral functions produce a unique INTA-D (PCI) or IRQ0-15 (ISA) signal that is routed to interrupt processing logic that asserts the interrupt (INTR-) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

Figure 4-11 shows the routing of PCI and ISA interrupts. Most IRQs are routed through the I/O controller, which contains a serializing function. A serialized interrupt stream is applied to the 82801 ICH.

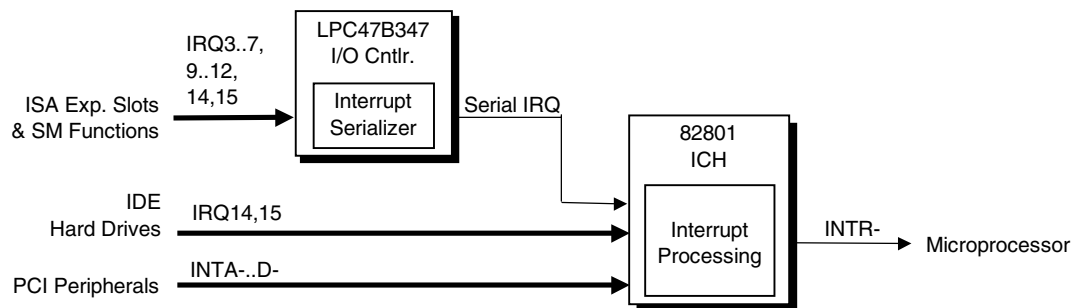


Figure 4-11. Maskable Interrupt Processing, Block Diagram

The 82801 ICH component, which includes the equivalent of two 8259 interrupt controllers cascaded together, handles the decoding of the serial interrupt stream (Serial IRQ signal) as well as interrupts IRQ14 and 15 from the IDE hard drives. The ICH also receives the PCI interrupt signals (INTA-..INTD-) from PCI devices. The PCI interrupts can be configured by PCI Configuration Registers 60h..63h to share the standard ISA interrupts (IRQn). The power-up default configuration has the PIRQn disabled. Table 4-13 lists the standard source configuration for maskable interrupts and their priorities. If more than one interrupt is pending, the highest priority (lowest number) is processed first.

The 82801 ICH is configured to handle interrupts in 8259-mode.

Table 4-12.
Maskable Interrupt Priorities and Assignments

Priority	Signal Label	Source (Typical)
1	IRQ0	Interval timer 1, counter 0
2	IRQ1	Keyboard
3	IRQ8-	Real-time clock
4	IRQ9	Spare and ISA connector pin B04
5	IRQ10	Spare and ISA connector pin D03
6	IRQ11	Spare and ISA connector pin D04
7	IRQ12	Mouse and ISA connector pin D05
8	IRQ13	Coprocessor (math)
9	IRQ14	IDE primary I/F and ISA connector pin D07
10	IRQ15	IDE secondary I/F and ISA connector pin D06
11	IRQ3	Serial port (COM2) and ISA connector pin B25
12	IRQ4	Serial port (COM1) and ISA connector pin B24
13	IRQ5	ISA connector pin B23
14	IRQ6	Diskette drive controller and ISA connector pin B22
15	IRQ7	Parallel port (LPT1)
--	IRQ2	NOT AVAILABLE (Cascade from interrupt controller 2)

Interrupts generated by PCI devices can be configured to share the standard AT (IRQ_n) interrupt lines. Also, PCI interrupts are hardwired for even distribution to minimize latency (see section 4.2.4 “PCI Interrupt Mapping”).

Maskable Interrupt processing is controlled and monitored through standard AT-type I/O-mapped registers. These registers are listed in Table 4-13.

Table 4-13.
Maskable Interrupt Control Registers

I/O Port	Register
020h	Base Address, Int. Cntrl. 1
021h	Initialization Command Word 2-4, Int. Cntrl. 1
0A0h	Base Address, Int. Cntrl. 2
0A1h	Initialization Command Word 2-4, Int. Cntrl. 2

The initialization and operation of the interrupt control registers follows standard AT-type protocol.

4.4.4.2 Non-Maskable Interrupts

Non-maskable interrupts cannot be masked (inhibited) within the microprocessor itself but may be maskable by software using logic external to the microprocessor. There are two non-maskable interrupt signals: the NMI- and the SMI-. These signals have service priority over all maskable interrupts, with the SMI- having top priority over all interrupts including the NMI-.

NMI- Generation

The Non-Maskable Interrupt (NMI-) signal can be generated by one of the following actions:


- ◆ Parity errors detected on the ISA bus (activating IOCHK-).
- ◆ Parity errors detected on a PCI bus (activating SERR- or PERR-).
- ◆ Microprocessor internal error (activating IERRA or IERRB)

The IOCHK-, SERR-, and PERR- signals are routed through the ICH component, which in turn activates the NMI to the microprocessor.

The NMI Status Register at I/O port 061h contains NMI source and status data as follows:

NMI Status Register 61h

Bit	Function
7	NMI Status: 0 = No NMI from system board parity error. 1 = NMI requested, read only
6	IOCHK- NMI: 0 = No NMI from IOCHK- 1 = IOCHK- is active (low), NMI requested, read only
5	Interval Timer 1, Counter 2 (Speaker) Status
4	Refresh Indicator (toggles with every refresh)
3	IOCHK- NMI Enable/Disable: 0 = NMI from IOCHK- enabled 1 = NMI from IOCHK- disabled and cleared (R/W)
2	System Board Parity Error (PERR/SERR) NMI Enable: 0 = Parity error NMI enabled 1 = Parity error NMI disabled and cleared (R/W)
1	Speaker Data (R/W)
0	Interval Timer 1, Counter 2 Gate Signal (R/W) 0 = Counter 2 disabled 1 = Counter 2 enabled

 Functions not related to NMI activity.

After the active NMI has been processed, status bits <7> or <6> are cleared by pulsing bits <2> or <3> respectively.

The NMI Enable Register (070h, <7>) is used to enable/disable the NMI signal. Writing 80h to this register masks generation of the NMI-. Note that the lower six bits of register at I/O port 70h affect RTC operation and should be considered when changing NMI- generation status.

SMI- Generation

The SMI- (System Management Interrupt) is typically used for power management functions. When power management is enabled, inactivity timers are monitored. When a timer times out, SMI- is asserted and invokes the microprocessor's SMI handler. The SMI- handler works with the APM BIOS to service the SMI- according to the cause of the timeout.

Although the SMI- is primarily used for power management the interrupt is also employed for the QuickLock/QuickBlank functions as well.

4.4.5 INTERVAL TIMER

The interval timer generates pulses at software (programmable) intervals. A 8254-compatible timer is integrated into the 82801 component. The timer function provides three counters, the functions of which are listed in Table 4-14.

Table 4-14.
Interval Timer Functions

Counter	Function	Gate	Clock In	Clock Out
0	System Clock	Always on	1.193 MHz	IRQ0
1	Refresh	Always on	1.193 MHz	Refresh Req.
2	Speaker Tone	Port 61, bit<0>	1.193 MHz	Speaker Input

The interval timer is controlled through the I/O mapped registers listed in Table 4-15.

Table 4-15.
Interval Timer Control Registers

I/O Port	Register
040h	Read or write value, counter 0
041h	Read or write value, counter 1
042h	Read or write value, counter 2
043h	Control Word

Interval timer operation follows standard AT-type protocol. For a detailed description of timer registers and operation, refer to the *Compaq Extended Industry Standard Architecture Expansion Bus Technical Reference Guide*.

4.4.6 ISA CONFIGURATION

The working relationship between the PCI and ISA buses requires that certain parameters such as DMA channels and interrupts be configured. The LPC bridge function of the 82801 ICH component includes PCI configuration registers for setting these and other related parameters. These parameters are programmed by BIOS during power-up, using registers listed previously in Table 4-6.

4.5 SYSTEM CLOCK DISTRIBUTION

These systems use a CK133 clock generator (for 820-based systems) or a CK Whitney or ICS92250-16 clock generator (for 810/810e-based systems). Table 4-16 lists the system board clock signals and how they are distributed.

Table 4-16.
Clock Generation and Distribution

Frequency/Signal	Source	Destination
300, 350, 400 MHz [1]	82820	RIMM sockets
66, 100, or 133 MHz (CPUCLK) [2]	CLK Gen.	Processor, GMCH/MCH
100 MHz	CK	DIMM sockets [3]
66 MHz	82820 MCH	AGP Slot
48 MHz	"	82801 ICH, 47B347 I/O Cntrlr.
33 MHz (PCICLK)	"	82801 ICH, PCI Slots, 82380 ISA Bridge
14.31818 MHz	Crystal	CK133
14.31818 MHz	CLK Gen	82801 ICH, ISA slots
8.33 MHz (BCLK)	82380	ISA slots

NOTES:

Clock generator SMBus device class address: 11010b

Clock generator SMBus device select address: 01b

[1] 820-based systems only.

[2] Depending on processor type (refer to Chapter 3, "Processor/Memory Subsystem").

[3] 810/810e-based systems only.

Certain clock outputs are turned off during reduced power modes to conserve energy. Clock output control is handled through the SMBus interface by BIOS.

4.6 REAL-TIME CLOCK AND CONFIGURATION MEMORY

The Real-time clock (RTC) and configuration memory (also referred to as “CMOS”) functions are provided by the 82801 ICH component and is MC146818-compatible. As shown in the following figure, the 82801 ICH component provides 256 bytes of battery-backed RAM divided into two 128-byte configuration memory areas. The RTC uses the first 14 bytes (00-0Dh) of the standard memory area. All locations of the standard memory area (00-7Fh) can be directly accessed using conventional OUT and IN assembly language instructions through I/O ports 70h/71h, although the suggested method is to use the INT15 AX=E823h BIOS call. Also note that CMOS locations above 3Fh are used for the control and status of features that should be handled through BIOS function INT15h, AX=E845h.

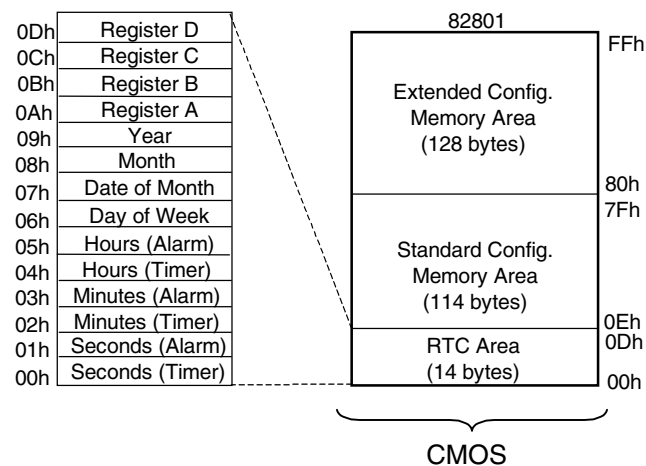


Figure 4-12. Configuration Memory Map

A lithium 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. During system operation a wire-ORed circuit allows the RTC and configuration memory to draw power from the power supply. The battery is located in a battery holder on the system board and has a life expectancy of four to eight years. When the battery has expired it is replaced with a Renata CR2032 or equivalent 3-VDC lithium battery.

NOTE: Early 810-based Deskpro systems include Compaq solutions to RTC defects present in early steps of the chipset and described as follows:

Incorrect reading of the RTC – To correct an RTC bug, a direct RTC access by software prompts an SMI that invokes a BIOS “double check” of the RTC for a correct read. The standard BIOS calls that read the RTC have also been modified to provide a “double check” for time/date reads.

Inaccurate Clock – An auxiliary oscillator circuit is included to correct deficiencies in the chipset’s time keeping.

Table 4-17 lists the mapping of the configuration memory.

Table 4-17.
Configuration Memory (CMOS) Map

Location	Function	Location	Function
00-0Dh	Real-time clock	24h	System board ID
0Eh	Diagnostic status	25h	System architecture data
0Fh	System reset code	26h	Auxiliary peripheral configuration
10h	Diskette drive type	27h	Speed control external drive
11h	Reserved	28h	Expanded/base mem. size, IRQ12
12h	Hard drive type	29h	Miscellaneous configuration
13h	Security functions	2Ah	Hard drive timeout
14h	Equipment installed	2Bh	System inactivity timeout
15h	Base memory size, low byte/KB	2Ch	Monitor timeout, Num Lock Cntrl
16h	Base memory size, high byte/KB	2Dh	Additional flags
17h	Extended memory, low byte/KB	2Eh-2Fh	Checksum of locations 10h-2Dh
18h	Extended memory, high byte/KB	30h-31h	Total extended memory tested
19h	Hard drive 1, primary controller	32h	Century
1Ah	Hard drive 2, primary controller	33h	Miscellaneous flags set by BIOS
1Bh	Hard drive 1, secondary controller	34h	International language
1Ch	Hard drive 2, secondary controller	35h	APM status flags
1Dh	Enhanced hard drive support	36h	ECC POST test single bit
1Eh	Reserved	37h-3Fh	Power-on password
1Fh	Power management functions	40-FFh	Feature Control/Status

NOTES:

Assume unmarked gaps are reserved.

Higher locations (>3Fh) contain information that should be accessed using the INT15, AX=E845h BIOS function (refer to Chapter 8 for BIOS function descriptions).

4.6.1 CLEARING CMOS

The contents of configuration memory (including the password) can be cleared by the following procedure:

1. Turn off unit.
2. Remove chassis hood (cover).
3. Press and hold CMOS clear button on system board for 5 seconds, then release.
4. Replace hood (cover).
5. Turn unit on.

Note that it is not necessary to unplug the unit from the AC socket to clear the configuration memory.

4.6.2 STANDARD CMOS LOCATIONS

The following paragraphs describe standard configuration memory locations 0Ah-3Fh. These locations are accessible through using OUT/IN assembly language instructions using port 70/71h or BIOS function INT15, AX=E823h.

RTC Control Register A, Byte 0Ah

Bit	Function
7	Update in Progress. Read only. 0 = Time update will not occur before 2444 us 1 = Time update will occur within 2444 us
6..4	Divider Chain Control. R/W. 00x = Oscillator disabled. 010 = Normal operation (time base frequency = 32.768 KHz). 11x = Divider chain reset.
3..0	Periodic Interrupt Control. R/W. Specifies the periodic interrupt interval. 0000 = none 1000 = 3.90625 ms 0001 = 3.90625 ms 1001 = 7.8125 ms 0010 = 7.8125 ms 1010 = 15.625 ms 0011 = 122.070 us 1011 = 31.25 ms 0100 = 244.141 us 1100 = 62.50 ms 0101 = 488.281 us 1101 = 125 ms 0110 = 976.562 us 1110 = 250 ms 0111 = 1.953125 ms 1111 = 500 ms

RTC Control Register B, Byte 0Bh

Bit	Function
7	Time Update Enable/disable 0 = Normal operation, 1 = Disable time updating for time set
6	Periodic Interrupt Enable/Disable. 0 = Disable, 1 = Enable interval specified by Register A
5	Alarm Interrupt Enable/disable 0 = Disabled, 1 = Enabled
4	End-of-Update Interrupt Enable/Disable 0 = Disabled, 1 = Enabled
3	Reserved (read 0)
2	Time/Date Format Select 0 = BCD format, 1 = Binary format
1	Time Mode 0 = 12-hour mode, 1 = 24-hour mode
0	Automatic Daylight Savings Time Enable/Disable 0 = Disable 1 = Enable (Advance 1 hour on 1 st Sunday in April, retreat 1 hour on last Sunday in October).

RTC Status Register C, Byte 0Ch

Bit	Function
7	If set, interrupt output signal active (read only)
6	If set, indicates periodic interrupt flag
5	If set, indicates alarm interrupt
4	If set, indicates end-of-update interrupt
3..0	Reserved

RTC Status Register D, Byte 0Dh

Bit	Function
7	RTC Power Status 0 = RTC has lost power 1 = RTC has not lost power
6..0	Reserved

Configuration Byte 0Eh, Diagnostic Status

Default Value = 00h

This byte contains diagnostic status data.

Configuration Byte 0Fh, System Reset Code

Default Value = 00h

This byte contains the system reset code.

Configuration Byte 10h, Diskette Drive Type

Bit	Function
7..4	Primary (Drive A) Diskette Drive Type
3..0	Secondary (Drive B) Diskette Drive Type

Valid values for bits <7..4> and bits <3..0>:

0000 = Not installed
 0001 = 360-KB drive
 0010 = 1.2-MB drive
 0011 = 720-KB drive
 0100 = 1.44-MB/1.25-MB drive
 0110 = 2.88-MB drive
 (all other values reserved)

Configuration Byte 12h, Hard Drive Type

Bit	Function
7..4	Primary Controller 1, Hard Drive 1 Type: 0000 = none 1000 = Type 8 0001 = Type 1 1001 = Type 9 0010 = Type 2 1010 = Type 10 0011 = Type 3 1011 = Type 11 0100 = Type 4 1100 = Type 12 0101 = Type 5 1101 = Type 13 0110 = Type 6 1110 = Type 14 0111 = Type 7 1111 = other (use bytes 19h)
3..0	Primary Controller 1, Hard Drive 2 Type: 0000 = none 1000 = Type 8 0001 = Type 1 1001 = Type 9 0010 = Type 2 1010 = Type 10 0011 = Type 3 1011 = Type 11 0100 = Type 4 1100 = Type 12 0101 = Type 5 1101 = Type 13 0110 = Type 6 1110 = Type 14 0111 = Type 7 1111 = other (use bytes 1Ah)

Configuration Byte 13h, Security Functions

Default Value = 00h

Bit	Function
7	Reserved
6	QuickBlank Enable After Standby: 0 = Disable 1 = Enable
5	Administrator Password: 0 = Not present 1 = Present
4	Reserved
3	Diskette Boot Enable: 0 = Enable 1 = Disable
2	QuickLock Enable: 0 = Disable 1 = Enable
1	Network Server Mode/Security Lock Override: 0 = Disable 1 = Enable
0	Password State (Set by BIOS at Power-up) 0 = Not set 1 = Set

Configuration Byte 14h, Equipment Installed

Default Value (standard configuration) = 03h

Bit	Function
7,6	No. of Diskette Drives Installed: 00 = 1 drive 10 = 3 drives 01 = 2 drives 11 = 4 drives
5..2	Reserved
1	Coprocessor Present 0 = Coprocessor not installed 1 = Coprocessor installed
0	Diskette Drives Present 0 = No diskette drives installed 1 = Diskette drive(s) installed

Configuration Bytes 15h and 16h, Base Memory Size

Default Value = 280h

Bytes 15h and 16h hold a 16-bit value that specifies the base memory size in 1-KB (1024) increments. Valid base memory sizes are 512 and 640 kilobytes .

Configuration Bytes 17h and 18h, Extended Memory Size

Bytes 17h and 18h hold a 16-bit value that specifies the extended memory size in 1-KB increments.

Configuration Bytes 19h-1Ch, Hard Drive Types

Byte 19h contains the hard drive type for drive 1 of the primary controller if byte 12h bits <7..4> hold 1111b. Byte 1Ah contains the hard drive type for drive 2 of the primary controller if byte 12h bits <3..0> hold 1111b. Bytes 1Bh and 1Ch contain the hard drive types for hard drives 1 and 2 of the secondary controller.

Configuration Byte 1Dh, Enhanced IDE Hard Drive Support

Default Value = F0h

Bit	Function
7	EIDE - Drive C (83h)
6	EIDE - Drive D (82h)
5	EIDE - Drive E (81h)
4	EIDE - Drive F (80h)
3..0	Reserved

Values for bits <7..4> :

0 = Disable

1 = Enable for auto-configure

Configuration Byte 1Fh, Power Management Functions

Default Value = 00h

Bit	Function
7..4	Reserved
3	Slow Processor Clock for Low Power Mode 0 = Processor runs at full speed 1 = Processor runs at slow speed
2	Reserved
1	Monitor Off Mode 0 = Turn monitor power off after 45 minutes in standby 1 = Leave monitor power on
0	Energy Saver Mode Indicator (Blinking LED) 0 = Disable 1 = Enable

Configuration Byte 24h, System Board Identification

Default Value = 7Eh

Configuration memory location 24h holds the system board ID.

Configuration Byte 25h, System Architecture Data

Default Value = 0Bh

Bit	Function
7..4	Reserved
3	Unmapping of ROM: 0 = Allowed 1 = Not allowed
2	Reserved
1,0	Diagnostic Status Byte Address 00 = Memory locations 80C00000h-80C00004h 01 = I/O ports 878h-87Ch 11 = neither place

Configuration Byte 26h, Auxiliary Peripheral Configuration

Default Value = 00h

Bit	Function
7,6	I/O Delay Select 00 = 420 ns (default) 01 = 300 ns 10 = 2600 ns 11 = 540 ns
5	Alternative A20 Switching 0 = Disable port 92 mode 1 = Enable port 92 mode
4	Bi-directional Print Port Mode 0 = Disabled 1 = Enabled
3	Graphics Type 0 = Color 1 = Monochrome
2	Hard Drive Primary/Secondary Address Select: 0 = Primary 1 = Secondary
1	Diskette I/O Port 0 = Primary 1 = Secondary
0	Diskette I/O Port Enable 0 = Primary 1 = Secondary

Configuration Byte 27h, Speed Control/External Drive

Default Value = 00h

Bit	Function
7	Boot Speed 0 = Max MHz 1 = Fast speed
6..0	Reserved

Configuration Byte 28h, Expanded and Base Memory, IRQ12 Select

Default Value = 00h

Bit	Function
7	IRQ12 Select 0 = Mouse 1 = Expansion bus
6,5	Base Memory Size: 00 = 640 KB 01 = 512 KB 10 = 256 KB 11 = Invalid
4..0	Internal Compaq Memory: 00000 = None 00001 = 512 KB 00010 = 1 MB 00011 = 1.5 MB . . 11111 = 15.5 MB

Configuration Byte 29h, Miscellaneous Configuration Data

Default Value = 00h

Bit	Function
7..5	Reserved
4	Primary Hard Drive Enable (Non-PCI IDE Controllers) 0 = Disable 1 = Enable
3..0	Reserved

Configuration Byte 2Ah, Hard Drive Timeout

Default Value = 02h

Bit	Function
7..5	Reserved
4..0	Hard Drive Timeout (index to SIT timeout record)

Configuration Byte 2Bh, System Inactivity Timeout

Default Value = 23h

Bit	Function
7	Reserved
6,5	Power Conservation Boot 00 = Reserved 01 = PC on 10 = PC off 11 = Reserved
4..0	System Inactive Timeout. (Index to SIT system timeout record) 00000 = Disabled

Configuration Byte 2Ch, ScreenSave and NUMLOCK Control

Default Value = 00h

Bit	Function
7	Reserved
6	Numlock Control 0 = Numlock off at power on 1 = Numlock on at power on
5	Screen Blank Control: 0 = No screen blank 1 = Screen blank w/QuickLock
4..0	ScreenSave Timeout. (Index to SIT monitor timeout record) 000000 = Disabled

Configuration Byte 2Dh, Additional Flags

Default Value = 00h

Bit	Function
7..5	Reserved
4	Memory Test 0 = Test memory on power up only 1 = Test memory on warm boot
3	POST Error Handling (BIOS Defined) 0 = Display "Press F1 to Continue" on error 1 = Skip F1 message
2..0	Reserved

Configuration Byte 2Eh, 2Fh, Checksum

These bytes hold the checksum of bytes 10h to 2Dh.

Configuration Byte 30h, 31h, Total Extended Memory Tested

This location holds the amount of system memory that checked good during the POST.

Configuration Byte 32h, Century

This location holds the Century value in a binary coded decimal (BCD) format.

Configuration Byte 33h, Miscellaneous Flags

Default Value = 80h

Bit	Function
7	Memory Above 640 KB 0 = No, 1 = Yes
6	Reserved
5	Weitek Numeric Coprocessor Present: 0 = Not installed, 1 = Installed
4	Standard Numeric Coprocessor Present: 0 = Not installed, 1 = Installed
3..0	Reserved

Configuration Byte 34h, International Language Support

Default Value = 00h

Configuration Byte 35h, APM Status Flags

Default Value = 11h

Bit	Function
7..6	Power Conservation State: 00 = Ready 01 = Standby 10 = Suspend 11 = Off
5,4	Reserved
3	32-bit Connection: 0 = Disconnected, 1 = Connected
2	16-bit Connection 0 = Disconnected, 1 = Connected
1	Real Mode Connection 0 = Disconnected, 1 = Connected
0	Power Management Enable: 0 = Disabled 1 = Enabled

Configuration Byte 36h, ECC POST Test Single Bit Errors

Default Value = 01h

Bit	Function
7	Row 7 Error Detect
6	Row 6 Error Detect
5	Row 5 Error Detect
4	Row 4 Error Detect
3	Row 3 Error Detect
2	Row 2 Error Detect
1	Row 1 Error Detect
0	Row 0 Error Detect

0 = No single bit error detected.

1 = Single bit error detected.

Configuration Byte 37h-3Fh, Power-On Password

These eight locations hold the power-on password.

4.6.3 CMOS FEATURE BITS

Configuration memory above location 3Fh is used for storing special features that are accessed using BIOS function INT15, AX=E845h. Refer to Chapter 8 for more information on accessing the feature bits with BIOS.

4.7 SYSTEM MANAGEMENT

This section describes functions having to do with security, power management, temperature, and overall status. These functions are handled by hardware and firmware (BIOS) and generally configured through the Setup utility.

4.7.1 SECURITY FUNCTIONS

These systems include various features that provide different levels of security. Note that this subsection describes **only the hardware functionality** (including that supported by Setup) and does not describe security features that may be provided by the operating system and application software.

4.7.1.1 Power-On Password

These systems include a power-on password, which may be enabled or disabled through a jumper on header E49 on the system board. The jumper controls a GPIO input to the 82801 ICH that is checked during POST. The password is stored in configuration memory (CMOS) and if enabled and then forgotten by the user will require that CMOS be cleared (refer to section 4.6). Units are typically shipped with the jumper in place (password enabled).

4.7.1.2 Setup Password

The Setup utility may be configured to be always changeable or changeable only by entering a password. The password is held on CMOS and, if forgotten, will require that CMOS be cleared (refer to section 4.6).

4.7.1.3 Cable Lock Provision

These systems include a chassis cutout for the attachment of a cable lock mechanism.

4.7.1.4 I/O Interface Security

The serial, parallel, USB, and diskette interfaces may be disabled individually through the Setup utility to guard against unauthorized access to a system. In addition, the ability to write to or boot from a removable media drive (such as the diskette drive) may be enabled through the Setup utility. The disabling of the serial, parallel, and diskette interfaces are a function of the LPC47B34z I/O controller. The USB ports are controlled through the 82801 ICH.

4.7.1.5 Chassis Security

The Deskpro EN SFF/DT/MT systems and Deskpro Workstation feature Smart Cover (hood) Sensor and Smart Cover (hood) Lock mechanisms to inhibit unauthorized tampering of the system unit.

Smart Cover (Hood) Sensor

Deskpro EN SFF/DT/MT and Deskpro Workstation units include a plunger switch (mounted on the backplane board) that, when the hood is removed, closes and grounds the input of GPIO port 10 of the 82801 ICH. The battery-backed register for GPIO 10 will record this event with a set bit. This bit will remain set (even if the cover is replaced) until the system is powered up and the user completes the boot sequence successfully, at which time the bit will be cleared. Through Setup, the user can set this function to be used by Alert-On-LAN and/or one of three levels of support for a "hood removed" condition:

Level 0 - Hood removal indication is essentially disabled at this level. During POST, status bit is cleared and no other action is taken by BIOS.

Level 1 - During POST the message "The computer's cover has been removed since the last system start up" is displayed and time stamps in CMOS and SIT are updated.

Level 2 - During POST the "The computer's cover has been removed since the last system start up" message is displayed, time stamps in CMOS and SIT are updated, and the user is prompted for the administrator password.

Smart Cover (Hood) Lock

Deskpro EN SFF/DT/MT and Deskpro Workstation units include a solenoid-operated locking bar that, when activated, prevents the hood from being removed. The GPIO ports 44 and 45 of the LPC47B34x I/O controller provide the lock and unlock signals to the solenoid. A locked hood may be bypassed by unscrewing the locking mechanism with the Compaq Smart Cover Lock Failsafe Key (Compaq p/n xxxxxx).

4.7.2 POWER MANAGEMENT

This system provides baseline hardware support of ACPI- and APM-compliant firmware and software. Key power-consuming components (processor, chipset, I/O controller, and fan) can be placed into a reduced power mode either automatically or by user control. The system can then be brought back up ("wake-up") by events defined by the ACPI specification. The ACPI wake-up events supported by this system are listed as follows:

ACPI Wake-Up Event	System Wakes From
Power Button	Suspend or soft-off
RTC Alarm	Suspend or soft-off
Wake On LAN (w/NIC)	Suspend or soft-off
PME	Suspend or soft-off
Serial Port Ring	Suspend or soft-off
USB	Suspend only
Keyboard	Suspend only
Mouse	Suspend only

4.7.3 SYSTEM STATUS

These systems provide the user a visual indication of system boot and ROM flash status through the keyboard LEDs and operational status using bi-colored power and hard drive activity LEDs as indicated in Tables 4-18 and 4-19 respectively.

NOTE: The LED indications listed in Table 4-18 are valid only for PS/2-type keyboards. A USB keyboard will not provide LED status for the listed events, although the audible (beep) indications will occur.

Table 4-18.
System Boot/ROM Flash Status LED Indications

Event	NUM Lock LED	CAPs Lock LED	Scroll Lock LED
System memory failure [1]	Blinking	Off	Off
Graphics controller failure [2]	Off	Blinking	Off
System failure prior to graphics cntlr. initialization [3]	Off	Off	Blinking
ROMPAQ diskette not present, faulty, or drive prob.	On	Off	Off
Password prompt	Off	On	Off
ROM flash failed	Blinking [4]	Blinking [4]	Blinking [4]
Keyboard locked in network mode	Blinking [5]	Blinking [5]	Blinking [5]
Successful boot block ROM flash	On	On	On

NOTES:

[1] Accompanied by 1 short, 2 long audio beeps

[2] Accompanied by 1 long, 2 short audio beeps

[3] Accompanied by 2 long, 1 short audio beeps

[4] All LEDs will blink in sync twice, accompanied by 1 long and three short audio beeps

[5] LEDs will blink in sequence (NUM Lock, then CAPs Lock, then Scroll Lock)

Table 4-19.
System Operational Status LED Indications

System Status	Power LED	Hard Drive LED
S0: System on (normal operation)	Steady green	Green w/HD activity
S1: Suspend	Blinks green @ 1 Hz	Off
S3: Suspend to RAM	Blinks green @ 1 Hz	Off
S4: Suspend to disk	Blinks green @ 0.5 Hz	Off
S5: Soft off	Blinks green @ 0.5 Hz	Off
Backplane board not seated	Steady red	Steady red
Processor not seated	Steady red	Off
Thermal condition	Blinks red @ 4 Hz	Off
ROM error	Blinks red @ 1 Hz	Off
Power supply crowbar activated	Blinks red @ 0.5 Hz	Off
System off	Off	Off

4.7.4 THERMAL SENSING AND COOLING

All systems feature a variable-speed fan (mounted as a part of the power supply assembly) controlled by thermal sensing logic (Figure 4-13). An ASIC called the Temperature-sensing And Fan control Integrated circuit (TAFI) monitors a thermal diode internal to the processor and drives the fan accordingly; faster fan speeds at higher temperatures and lower fan speeds (or off) at lower temperatures. High and low thermal parameters are programmed into TAFI by BIOS during POST. The Fan CMD signal generated by the TAFI varies from 0 to 2.5 volts and is applied to control logic for conversion to the Fan SPD signal, which provides the voltage swing required for fan control. If the high thermal parameter is reached then the Therm- signal is asserted, which results in the fan being turned on full speed and can result in an AOL message being transmitted over a network.

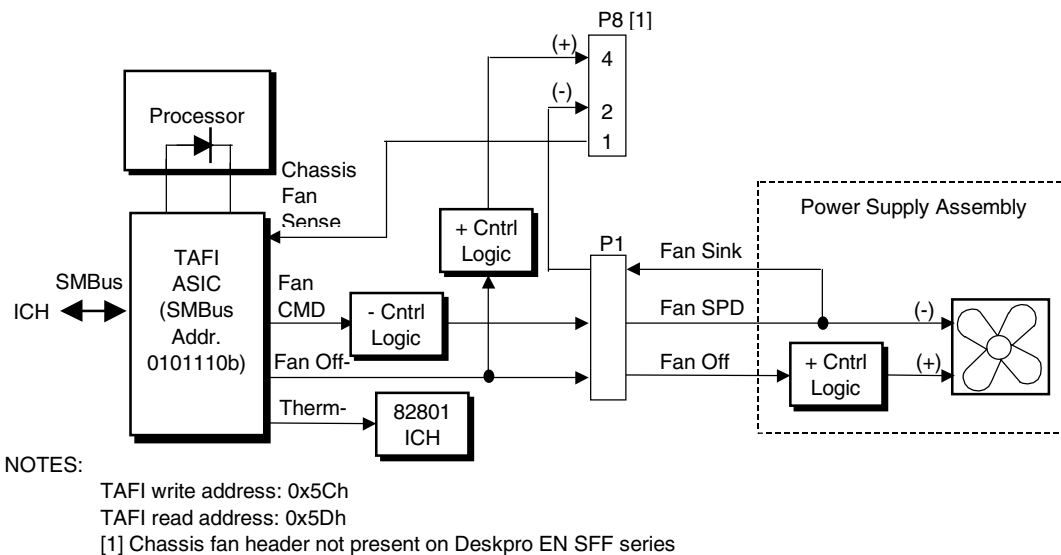


Figure 4-13. Fan Control Block Diagram

The TTL-level Fan Off - signal is used to turn off +12 VDC to the fan (such as during low power states), while the Fan SPD signal varies the negative voltage to the fan. The power supply assembly also includes a thermal sensor that can override a “Fan off” or “Fan slow” condition set by the TAFI ASIC and place the power supply fan in a full on state.

Deskpro EP, Workstation, and EN desktop and minitower systems support a chassis fan in addition to the power supply fan. The chassis fan (if present) is controlled solely by the TAFI ASIC and will not be overridden by a thermal condition dictated by the power supply.

NOTE: These systems do not support thermister-based fans used on earlier products.

All systems include a header for connection to a fan that may be included in some processor upgrade kits (known as “boxed processors”).

4.8 REGISTER MAP AND MISCELLANEOUS FUNCTIONS

This section contains the system I/O map and information on general-purpose functions of the ICH and I/O controller.

4.8.1 SYSTEM I/O MAP

Table 4-20 lists the fixed addresses of the input/output (I/O) ports.

Table 4-20.
System I/O Map

I/O Port	Function
0000..000Fh	DMA Controller 1
0020..0021h	Interrupt Controller 1
002Eh	Index Port to LPC47B34x I/O Controller
002Fh	Data Port for LPC47B34x I/O Controller (accessible in configuration mode only)
0040..0043h	Timer 1
0060h	Keyboard Controller Data Byte
0061h	NMI, Speaker Control
0064h	Keyboard Controller Command/Status Byte
0070h	NMI Enable, RTC/Lower CMOS Index
0071h	RTC Data
0080..008Fh	DMA Page Registers
0092h	Port A, Fast A20/Reset
00A0..00A1h	Interrupt Controller 2
00B2h, 00B3h	APM Control/Status Ports
00C0..00DFh	DMA Controller 2
00F0h	Math Coprocessor Busy Clear
015C, 015Dh	LPC47B34x I/O Controller Configuration Registers (Index, Data)
0170..0177h	Hard Drive (IDE) Controller 2
01F0..01FFh	Hard Drive (IDE) Controller 1
0201..024Fh	Audio subsystem control (primary & secondary addresses)
0278..027Bh	Parallel Port (LPT2)
02F8..02FFh	Serial Port (COM2)
0371.. 0375h	Diskette Drive Controller Alternate Addresses
0376h	IDE Controller Alternate Address
0377h	IDE Controller Alternate Address, Diskette Drive Controller Alternate Address
0378..037Fh	Parallel Port (LPT1)
0388..038Bh	FM synthesizer (alias addresses)
03B0..03DFh	Graphics Controller
03E8..03EFh	Serial Port (COM3)
03F0..03F5h	Diskette Drive Controller Primary Addresses
03F6, 03F7h	Diskette Drive Controller Primary Addresses, Hard Drive Controller Primary Addresses
03F8..03FFh	Serial Port (COM1)
04D0, 04D1h	Master, Slave Edge/Level INTR Control Register
0C00, 0C01h	PCI IRQ Mapping Index, Data
0C06, 0C07h	Reserved - Compaq proprietary use only
0C50, 0C51h	System Management Configuration Registers (Index, Data)
0C52h	General Purpose Port
0C7Ch	Machine ID
0CF8h	PCI Configuration Address (dword access)
0CF9h	Reset Control Register
0CFCh	PCI Configuration Data (byte, word, or dword access)
FF00..FF07h	IDE Bus Master Register

NOTE: Assume unmarked gaps are reserved/unused.

4.8.2 82801 ICH GENERAL PURPOSE FUNCTIONS

The 82801 ICH component includes a number of single and multi-purpose pins available as general-purpose input/output (GPIO) ports. The GPIO ports are configured (enabled/disabled) during POST by BIOS through the PCI configuration registers of the ICH's LPC I/F Bridge (82801, function 0). The GPIO ports are controlled through 64 bytes of I/O space that is mapped during POST. Table 4-20 lists the utilization of the ICH's GPIO ports in these systems. Table 4-21 lists the GPIO registers for the LPC47B34x.

Table 4-21.
82801 ICH GPIO Register Utilization

GPIO Port #	Function	Direction
0	MISA REQA	
1	REQ5	
5	Pwr LED Det	I
6	HD LED Det	I
7	PERR	I
8	Password Disable	I
10	Hood Sense (intruder)	I
11	SMB Alert	I
12	TAFI Interrupt	I
13	SIO SMI	I
16	MISA GNTA	
17	LAN EN	
21	MISA NoGo	O
22	GPIO Spread	O
24	SLF S3	
25	Xxx Pwr En	
26	SUS Clk	O
27	Alert Clock	I/O
28	Alert Data	I/O

NOTE:

4.8.3 LPC47B34x I/O CONTROLLER FUNCTIONS

The LPC47B34x I/O controller contains various functions such as the keyboard/mouse interfaces, diskette interface, serial interfaces, and parallel interface. While the control of these interfaces uses standard AT-type I/O addressing (as described in chapter 5) the configuration of these functions uses indexed ports unique to the LPC47B34x. In these systems, hardware strapping selects I/O addresses 02Eh and 02Fh at reset as the Index/Data ports for accessing the logical devices within the LPC47B34x.

Table 4-22 lists the PnP standard control registers for the LPC47B34x.

Table 4-22. LPC47B34x I/O Controller Control Registers		
Index	Function	Reset Value
02h	Configuration Control	00h
03h	Reserved	
07h	Logical Device (Interface) Select: 00h = Diskette Drive I/F 01h = Reserved 02h = Reserved 03h = Parallel I/F 04h = Serial I/F (UART 1/Port A) 05h = Serial I/F (UART 2/Port B) 06h = Reserved 07h = Keyboard I/F 08h = Reserved 09h = Reserved 0Ah = Runtime Registers (GPIO Config.) 0Bh = Reserved	00h
20h	Super I/O ID Register (SID)	56h
21h	Revision	--
22h	Logical Device Power Control	00h
23h	Logical Device Power Management	00h
24h	PLL / Oscillator Control	04h
25h	Reserved	
26h	Configuration Address (Low Byte)	
27h	Configuration Address (High Byte)	
28-2Fh	Reserved	

NOTE:

For a detailed description of registers refer to appropriate SMC documentation.

The configuration registers are accessed through I/O registers 2Eh (index) and 2Fh (data) after the configuration phase has been activated by writing 55h to I/O port 2Eh. The desired interface (logical device) is initiated by firmware selecting logical device number of the 47B347 using the following sequence:

1. Write 07h to I/O register 2Eh.
2. Write value of logical device to I/O register 2Fh.
3. Write 30h to I/O register 2Eh.
4. Write 01h to I/O register 2Fh (this activates the interface).

Writing AAh to 2Eh deactivates the configuration phase.

4.8.3.1 LPC47B34x GPIO Utilization

The LPC47B34x I/O Controller provides 62 general-purpose pins that can be individually configured for specific purposes. These pins are configured through the Runtime registers (logical device 0Ah) during the system's configuration phase of the boot sequence by the BIOS.

Table 4-23 lists the GPIO registers for the LPC47B34x. Note that not all ports are listed as this table defines only the custom implementation of GPIO ports. Refer to SMC documentation for standard usage of unlisted GPIO ports.

Table 4-23.
LPC47B34x GPIO Port Utilization

GPIO Port #	Function	Direction
13	PME-	I
14	WOL	I
17	LED Test	O
20	Pri. IDE 80-pin Cable Detect	I
21	Sec. IDE 80-pin Cable Detect	I
22	Chassis ID bit 0	I
23	Chassis ID bit 1	I
24	AOL BIOS Fail	O
25	Hood Sense [1]	I
26	Processor Present	I
30	PS LED Color	O
31	PS LED Blink	O
32	Thermal Trip	I
33	2 MB Media ID	I
34	FWH Write Protect	O
35	FWH Reset	O
36	Diskette Motor A	O
37	Diskette Select A	O
42	ICH SCI	O
43	AOL OS Fail	O
44	Hood Lock [1]	I
45	Hood Unlock [1]	I
46	ICH SMI-	O
60	PCI Slot Reset	
62	PWR Button In	I
63	SLP S3	
64	SLP S5	
65	CPU Slow	O
66	PWR Button Out	O
67	PS On	O
83	PWR Good	I
84	AUX PWR Good	I
85	Coil Connected [1]	I
86	S3 On	O

NOTE:

[1] Not implemented on Deskpro EP series.

4.8.3.2 I/O Controller Miscellaneous Functions

The systems covered in this guide utilize the following specialized functions built into the LPC 47B34x I/O Controller:

- ◆ Power/Hard drive LED control – The I/O controller provides color and blink control for the front panel LEDs used for indicating system events as listed below:

System Status	Power LED	HD LED
S0: System on (normal operation)	Steady green	Green w/HD activity
S1: Suspend	Blinks green @ 1 Hz	Off
S3: Suspend to RAM	Blinks green @ 1 Hz	Off
S4: Suspend to disk	Blinks green @ 0.5 Hz	Off
S5: Soft off	Blinks green @ 0.5 Hz	Off
Backplane board not seated	Steady red	Steady red
Processor not seated	Steady red	Off
Thermal condition	Blinks red @ 4 Hz	Off
ROM error	Blinks red @ 1 Hz	Off
Power supply crowbar activated	Blinks red @ 0.5 Hz	Off
System off	Off	Off

- ◆ Intruder sensing – Used on Deskpro EN and Workstation models, battery-backed D-latch logic internal to the LPC47B34x is connected to the hood sensor switch to record hood (cover) removal.
- ◆ Hood lock/unlock – Used on Deskpro EN and Workstation models, logic internal to the LPC47B34x controls the lock bar mechanism.
- ◆ I/O security – The parallel, serial, and diskette interfaces may be disabled individually by software and the LPC47B34x's disabling register locked. If the disabling register is locked, a system reset through a cold boot is required to gain access to the disabling (Device Disable) register.
- ◆ Processor present/speed detection – One of the battery-back general-purpose inputs (GPI26) of the LPC47B34x detects if the processor has been removed. The occurrence of this event is passed to the ICH that will, during the next boot sequence, initiate the speed selection routine for the processor. The speed selection function replaces the manual DIP switch configuration procedure required on previous systems.
- ◆ Legacy/ACPI power button mode control – The LPC47B34x receives the pulse signal from the system's power button and produces the PS On signal according to the mode (legacy or ACPI) selected. Refer to chapter 7 for more information regarding power management.

Chapter 5

INPUT/OUTPUT INTERFACES

5.1 INTRODUCTION

This chapter describes the standard (i.e., system board) interfaces that provide input and output (I/O) porting of data and specifically discusses interfaces that are controlled through I/O-mapped registers. The following I/O interfaces are covered in this chapter:

- ◆ Enhanced IDE interface (5.2) page 5-1
- ◆ Diskette drive interface (5.3) page 5-5
- ◆ Serial interfaces (5.4) page 5-9
- ◆ Parallel interface (5.5) page 5-12
- ◆ Keyboard/pointing device interface (5.6) page 5-19
- ◆ Universal serial bus interface (5.7) page 5-26
- ◆ Audio subsystem (5.8) page 5-28
- ◆ Network support (5.9) page 5-35

5.2 ENHANCED IDE INTERFACE

The enhanced IDE (EIDE) interface consists of primary and secondary controllers integrated into the 82801 ICH component of the chipset. The IDE connectors on the system board are associated with the EIDE interface: two 40-pin IDE data connectors (one primary, one secondary), and, on the EN SFF system, a CD-ROM connector also associated with the secondary EIDE controller. Each controller can support two devices and can be configured independently for the following modes of operation:

- ◆ Programmed I/O (PIO) mode – CPU controls drive transactions through standard I/O mapped registers of the IDE drive.
- ◆ 8237 DMA mode – CPU offloads drive transactions using DMA protocol with transfer rates up to 16 MB/s.
- ◆ Ultra ATA/33 and /66 modes – Preferred bus mastering source-synchronous protocol providing transfer rates of 33 and 66 MB/s respectively.

NOTE: Although the EIDE interface can electrically handle four EIDE devices, the form factor of the unit chassis may impose a limit on the number of devices that can be mounted. Refer to chapter 2 for drive bay accommodations.

5.2.1 IDE PROGRAMMING

The IDE interface is configured as a PCI device during POST and controlled through I/O-mapped registers at runtime.

Hard drives types not found in the ROM's parameter table are automatically configured as to (soft)type by DOS as follows:

Primary controller: drive 0, type 65; drive 1, type 66
 Secondary controller: drive 0, type 68; drive 1, type 15

Non-DOS (non-Windows) operating systems may require using Setup (F10) for drive configuration.

5.2.1.1 IDE Configuration Registers

The IDE controller is configured as a PCI device with bus mastering capability. The PCI configuration registers for the IDE controller function (PCI device #31, function #1) are listed in Table 5-1.

Table 5-1. EIDE PCI Configuration Registers (82801, Device 31/Function 1)					
PCI Conf. Addr.	Register	Value on Reset	PCI Conf. Addr.	Register	Value on Reset
00-01h	Vender ID	8086h	24-2Bh	Reserved	0's
02-03h	Device ID	2411h	2C, 2Dh	Subsystem Vender ID	8086h
04-05h	PCI Command	0000h	2E, 2Fh	Subsystem ID	2411h
06-07h	PCI Status	0280h	30-3Fh	Reserved	0's
08h	Revision ID	00h	40-43h	Primary IDE Timing	0000h
09h	Programming	80h	44h	Secondary IDE Timing	00h
0Ah	Sub-Class	01h	48h	Sync. DMA Control	00h
0Bh	Base Class Code	01h	4A-4Bh	Sync. DMA Timing	0000h
0Dh	Master Latency Timer	0000h	54h	EIDE I/O Config.Register	00h
0Eh	Header Type	80h	F8-FBh	Manufacturer's ID	
0F-1Fh	Reserved	00h	FC-FFh	Reserved	
20-23h	BMIDE Base Address	1h	--	--	--

NOTE:

Assume unmarked gaps are reserved and/or not used.

5.2.1.2 IDE Bus Master Control Registers

The IDE interface can perform PCI bus master operations using the registers listed in Table 5-2. These registers occupy 16 bytes of variable I/O space set by software and indicated by PCI configuration register 20h in the previous table.

Table 5-2. IDE Bus Master Control Registers			
I/O Addr. Offset	Size (Bytes)	Register	Default Value
00h	1	Bus Master IDE Command (Primary)	00h
02h	1	Bus Master IDE Status (Primary)	00h
04h	4	Bus Master IDE Descriptor Pointer (Pri.)	0000 0000h
08h	1	Bus Master IDE Command (Secondary)	00h
0Ah	2	Bus Master IDE Status (Secondary)	00h
0Ch	4	Bus Master IDE Descriptor Pointer (Sec.)	0000 0000h

NOTE:

Unspecified gaps are reserved, will return indeterminate data, and should not be written to.

5.2.2 IDE CONNECTOR

This system uses a standard 40-pin connector for IDE devices. Note that some signals are re-defined for UATA/33 and UATA/66 modes, which require a special 80-conductor cable (supplied) designed to reduce cross-talk. Device power is supplied through a separate connector.

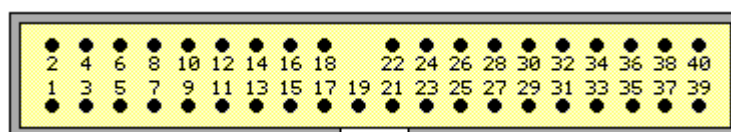


Figure 5-1. 40-Pin IDE Connector.

Table 5-5.
40-Pin IDE Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RESET-	Reset	21	DRQ	DMA Request
2	GND	Ground	22	GND	Ground
3	DD7	Data Bit <7>	23	IOW-	I/O Write [1]
4	DD8	Data Bit <8>	24	GND	Ground
5	DD6	Data Bit <6>	25	IOR-	I/O Read [2]
6	DD9	Data Bit <9>	26	GND	Ground
7	DD5	Data Bit <5>	27	IORDY	I/O Channel Ready [3]
8	DD10	Data Bit <10>	28	CSEL	Cable Select
9	DD4	Data Bit <4>	29	DAK-	DMA Acknowledge
10	DD11	Data Bit <11>	30	GND	Ground
11	DD3	Data Bit <3>	31	IRQn	Interrupt Request [4]
12	DD12	Data Bit <12>	32	IO16-	16-bit I/O
13	DD2	Data Bit <2>	33	DA1	Address 1
14	DD13	Data Bit <13>	34	DSKPDIAG	Pass Diagnostics
15	DD1	Data Bit <1>	35	DA0	Address 0
16	DD14	Data Bit <14>	36	DA2	Address 2
17	DD0	Data Bit <0>	37	CS0-	Chip Select
18	DD15	Data Bit <15>	38	CS1-	Chip Select
19	GND	Ground	39	HDACTIVE-	Drive Active (front panel LED) [5]
20	--	Key	40	GND	Ground

NOTES:

- [1] On UATA/33 and /66 modes, re-defined as STOP.
- [2] On UATA/33 and /66 mode reads, re-defined as DMARDY-.
On UATA/33 and /66 mode writes, re-defined as STROBE.
- [3] On UATA/33 and /66 mode reads, re-defined as STROBE-.
On UATA/33 and /66 mode writes, re-defined as DMARDY-.
- [4] Primary connector wired to IRQ14, secondary connector wired to IRQ15.
- [5] Pin 39 is used for spindle sync and drive activity (becomes SPSYNC/DACT-) when synchronous drives are connected.

Compaq Deskpro EN SFF models include a 50-pin connector for a CD-ROM drive that operates as a slave on the secondary IDE interface. This interface includes power and audio signals. The 50-pin connector is illustrated below followed by the pinout.

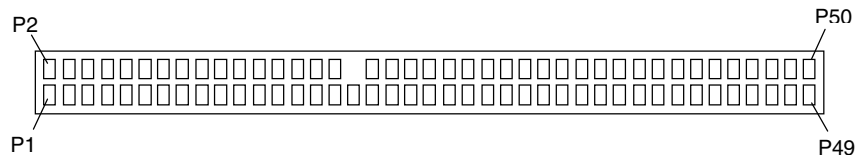


Figure 5-2. 50-Pin IDE CD-ROM Connector.

Table 5-4.
50-Pin IDE CD-ROM Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RESDRV-	Reset	26	GND	Ground
2	GND	Ground	27	CHRDY	I/O Channel Ready
3	SHD07	Data Bit <7>	28	ALE	Cable Select [1]
4	SHD08	Data Bit <8>	29	DAK-	DMA Acknowledge
5	SHD06	Data Bit <6>	30	GND	Ground
6	SHD09	Data Bit <9>	31	IRQ	Interrupt Request [1]
7	SHD05	Data Bit <5>	32	IO16-	16-bit I/O
8	SHD10	Data Bit <10>	33	A1	Address 1
9	SHD04	Data Bit <4>	34	PDIAG-	Pass Diagnostics
10	SHD11	Data Bit <11>	35	A0	Address 0
11	SHD03	Data Bit <3>	36	A2	Address 2
12	SHD12	Data Bit <12>	37	CS1FX-	Chip Select
13	SHD02	Data Bit <2>	38	CS3FX-	Chip Select
14	SHD13	Data Bit <13>	39	DASF-	Drive Active
15	SHD01	Data Bit <1>	40	GND	Ground
16	SHD14	Data Bit <14>	41	AUD L	Left Channel Audio
17	SHD00	Data Bit <0>	42	AUD R	Right Channel Audio
18	SHD15	Data Bit <15>	43	AUD R RTN	Right Channel Audio Return
19	GND	Ground	44	AUD L RTN	Left Channel Audio Return
20	--	(Key Space)	45	+5 VDC	Motor Power
21	DRQ	DMA Request	46	+5 VDC	Motor Power
22	GND	Ground	47	+5 VDC	Motor Power
23	IOW-	I/O Write	48	+5 VDC	Motor Power
24	GND	Ground	49	+5 VDC	Log Power
25	IOR-	I/O Read	50	+5 VDC	Log Power

NOTES:

[1] Pin is left floating to make CD-ROM always slave (see note below).

NOTE: The Deskpro EN SFF system board includes a header connector (E23). On CDS models this header ships with a jumper installed. If an LS-120 (Power Drive) drive is installed (in addition to the CD-ROM) and connected to the secondary 40-pin IDE connector then this jumper should be removed.

5.3 DISKETTE DRIVE INTERFACE

The diskette drive interface supports up to two diskette drives, each of which use a common cable connected to a standard 34-pin diskette drive connector. All models come standard with a 3.5-inch 1.44-MB diskette drive installed as drive A. The drive designation is determined by which connector is used on the diskette drive cable. The drive attached to the end connector is drive A while the drive attached to the second (next to the end) connector is drive B.

On all models, the diskette drive interface function is integrated into the LPC47B347 super I/O component. The internal logic of the I/O controller is software-compatible with standard 82077-type logic. The diskette drive controller has three operational phases in the following order:

- ◆ Command phase - The controller receives the command from the system.
- ◆ Execution phase - The controller carries out the command.
- ◆ Results phase - Status and results data is read back from the controller to the system.

The Command phase consists of several bytes written in series from the CPU to the data register (3F5h/375h). The first byte identifies the command and the remaining bytes define the parameters of the command. The Main Status register (3F4h/374h) provides data flow control for the diskette drive controller and must be polled between each byte transfer during the Command phase.

The Execution phase starts as soon as the last byte of the Command phase is received. An Execution phase may involve the transfer of data to and from the diskette drive, a mechanical control function of the drive, or an operation that remains internal to the diskette drive controller. Data transfers (writes or reads) with the diskette drive controller are by DMA, using the DRQ2 and DACK2- signals for control.

The Results phase consists of the CPU reading a series of status bytes (from the data register (3F5h/375h)) that indicate the results of the command. Note that some commands do not have a Result phase, in which case the Execution phase can be followed by a Command phase.

During periods of inactivity, the diskette drive controller is in a non-operation mode known as the Idle phase.

5.3.1 DISKETTE DRIVE PROGRAMMING

Programming the diskette drive interface consists of configuration, which occurs typically during POST, and control, which occurs at runtime.

5.3.1.1 Diskette Drive Interface Configuration

The diskette drive controller must be configured for a specific address and also must be enabled before it can be used. Address selection and enabling of the diskette drive interface are affected by firmware through the PnP configuration registers of the 47B347 I/O controller during POST.

The configuration registers are accessed through I/O registers 2Eh (index) and 2Fh (data) after the configuration phase has been activated by writing 55h to I/O port 2Eh. The diskette drive I/F is initiated by firmware selecting logical device 0 of the 47B347 using the following sequence:

1. Write 07h to I/O register 2Eh.
2. Write 00h to I/O register 2Fh (this selects the diskette drive I/F).
3. Write 30h to I/O register 2Eh.
4. Write 01h to I/O register 2Fh (this activates the interface).

Writing AAh to 2Eh deactivates the configuration phase. The diskette drive I/F configuration registers are listed in the following table:

Table 5-5. Diskette Drive Interface Configuration Registers			
Index Address	Function	R/W	Reset Value
30h	Activate	R/W	01h
60-61h	Base Address	R/W	03F0h
70h	Interrupt Select	R/W	06h
74h	DMA Channel Select	R/W	02h
F0h	DD Mode	R/W	02h
F1h	DD Option	R/W	00h
F2h	DD Type	R/W	FFh
F4h	DD 0	R/W	00h
F5h	DD 1	R/W	00h

For detailed configuration register information refer to the SMSC data sheet for the LPC47B347 I/O component.

5.3.1.2 Diskette Drive Interface Control

The BIOS function INT 13 provides basic control of the diskette drive interface. The diskette drive interface can be controlled by software through the LPC47B347's I/O-mapped registers listed in Table 5-6. The diskette drive controller of the LPC47B347 operates in the PC/AT mode in these systems.

Table 5-6.
Diskette Drive Interface Control Registers

Pri. Addr.	Sec. Addr.	Register	R/W
3F0h	370h	Status Register A: <7> Interrupt pending <6> Reserved (always 1) <5> STEP pin status (active high) <4> TRK 0 status (active high) <3> HDSEL status (0 = side 0, 1 = side 1) <2> INDEX status (active high) <1> WR PRTK status (0 = disk is write protected) <0> Direction (0 = outward, 1 = inward)	R
3F1h	371h	Status Register B: <7,6> Reserved (always 1's) <5> DOR bit 0 status <4> Write data toggle <3> Read data toggle <2> WGATE status (active high) <1,0> MTR 2, 1 ON- status (active high)	R
3F2h	372h	Digital Output Register (DOR): <7,6> Reserved <5,4> Motor 1, 0 enable (active high) <3> DMA enable (active high) <2> Reset (active low) <1,0> Drive select (00 = Drive 1, 01 = Drive 2, 10 = Reserved, 11 = Tape drive)	R/W
3F3h	373h	Tape Drive Register (available for compatibility)	R/W
3F4h	374h	Main Status Register (MSR): <7> Request for master (host can transfer data) (active high) <6> Transfer direction (0 = write, 1 = read) <5> non-DMA execution (active high) <4> Command busy (active high) <3,2> Reserved <1,0> Drive 1, 2 busy (active high)	R
		Data Rate Select Register (DRSR): <7> Software reset (active high) <6> Low power mode enable (active high) <5> Reserved (0) <4..2> Precompensation select (default = 000) <1,0> Data rate select (00 = 500 Kb/s, 01 = 300 Kb/s, 10 = 250 Kb/s, 11 = 2/1 Mb/s)	W
3F5h	375h	Data Register: <7..0> Data	R/W
3F6h	376h	Reserved	--
3F7h	377h	Digital Input Register (DIR): <7> DSK CHG status (records opposite value of pin) <6..0> Reserved (0's)	R
		Configuration Control Register (CCR): <7..2> Reserved <1,0> Data rate select (00 = 500 Kb/s, 01 = 300 Kb/s, 10 = 250 Kb/s, 11 = 2/1 Mb/s)	W

NOTE: The most recently written data rate value to either DRSR or CCR will be in effect.

5.3.2 DISKETTE DRIVE CONNECTOR

This system uses a standard 34-pin connector (refer to Figure 5-3 and Table 5-7 for the pinout) for diskette drives. Drive power is supplied through a separate connector.

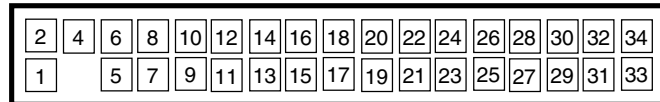


Figure 5-3. 34-Pin Diskette Drive Connector.

Table 5-7.
34-Pin Diskette Drive Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	18	DIR-	Drive head direction control
2	LOW DEN-	Low density select	19	GND	Ground
3	---	(KEY)	20	STEP-	Drive head track step control
4	MEDIA ID-	Media identification	21	GND	Ground
5	GND	Ground	22	WR DATA-	Write data
6	DRV 4 SEL-	Drive 4 select	23	GND	Ground
7	GND	Ground	24	WR ENABLE-	Enable for WR DATA-
8	INDEX-	Media index is detected	25	GND	Ground
9	GND	Ground	26	TRK 00-	Heads at track 00 indicator
10	MTR 1 ON-	Activates drive motor	27	GND	Ground
11	GND	Ground	28	WR PRTK-	Media write protect status
12	DRV 2 SEL-	Drive 2 select	29	GND	Ground
13	GND	Ground	30	RD DATA-	Data and clock read off disk
14	DRV 1 SEL-	Drive 1 select	31	GND	Ground
15	GND	Ground	32	SIDE SEL-	Head select (side 0 or 1)
16	MTR 2 ON-	Activates drive motor	33	GND	Ground
17	GND	Ground	34	DSK CHG-	Drive door opened indicator

5.4 SERIAL INTERFACES

The serial interfaces transmit and receive asynchronous serial data with external devices. The serial interface function is provided by the LPC47B347 I/O controller component, which includes a pair of NS16C550-compatible UARTs. The UARTS support the following baud rates:

Baud Rate	Baud Rate
50	3600
75	4800
110	7200
134.5	9600
150	19200
300	38400
600	57600
1200	115200
1800	230400 (see text)
2000	460800 (see text)
2400	

The baud rate of the UART is typically set to match the capability of the connected device. While most baud rates may be set at runtime, **baud rates 230400 and 460800 must be set during the configuration phase.**

5.4.1 RS-232 INTERFACE

Each UART is associated with a DB-9 connector that complies with EIA standard RS-232-C. The DB-9 connector is shown in the following figure and the pinout of the connector is listed in Table 5-8.

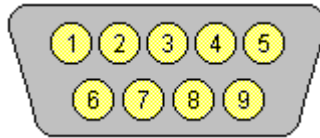


Figure 5-4. Serial Interface Connector (Male DB-9 as viewed from rear of chassis)

Table 5-8.
DB-9 Serial Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	CD	Carrier Detect	6	DSR	Data Set Ready
2	RX Data	Receive Data	7	RTS	Request To Send
3	TX Data	Transmit Data	8	CTS	Clear To Send
4	DTR	Data Terminal Ready	9	RI	Ring Indicator
5	GND	Ground	--	--	--

The standard RS-232-C limitation of 50 feet (of less) of cable between the DTE (computer) and DCE (modem) should be followed to minimize transmission errors. Higher baud rates may require shorter cables.

5.4.2 SERIAL INTERFACE PROGRAMMING

Programming the serial interfaces consists of configuration, which occurs during POST, and control, which occurs during runtime.

5.4.2.1 Serial Interface Configuration

The serial interfaces must be configured for a specific address range (COM1, COM2, etc.) and also must be activated before it can be used. Address selection and activation of the serial interface are affected through the PnP configuration registers of the LPC47B347 I/O controller.

The PnP configuration registers are accessed through I/O registers 02Eh (index) and 02Fh (data). Each serial interface is initiated by firmware selecting logical device 4 or 5 of the LPC47B347. After entering the configuration phase by writing 55h to I/O port 02Eh, activating each logical device is achieved with the following sequence:

1. Write 07h to I/O register 02Eh.
2. Write 04h or 05h to I/O register 02Fh (for selecting UART1 or UART2).
3. Write 30h to I/O register 02Eh.
4. Write 01h to I/O register 02Fh (this activates the interface).

Deactivating the configuration phase is accomplished by writing AAh to port 02Eh.

The serial interface configuration registers are listed in the following table:

Table 5-9.		
Serial Interface Configuration Registers		
Index		
Address	Function	R/W
30h	Activate	R/W
60h	Base Address MSB	R/W
61h	Base Address LSB	R/W
70h	Interrupt Select	R/W
F0h	Mode Register	R/W

NOTE:

Refer to LPC47B347 data sheet for detailed register information.

5.4.2.2 Serial Interface Control

The BIOS function INT 14 provides basic control of the serial interface. The serial interface can be directly controlled by software through the I/O-mapped registers listed in Table 5-9.

Table 5-10.
Serial Interface Control Registers

COM1 Addr.	COM2 Addr.	Register	R/W
3F8h	2F8h	Receive Data Buffer	R
		Transmit Data Buffer	W
		Baud Rate Divisor Register 0 (when bit 7 of Line Control Reg. Is set)	W
3F9h	2F9h	Baud Rate Divisor Register 1 (when bit 7 of Line Control Reg. Is set)	W
		Interrupt Enable Register:	R/W
		<7..4> Reserved (always 0's)	
		<3> Modem status interrupt enable (active high) (CTS, DSR, RI, CD)	
		<2> Rx line status interrupt enable (active high) (Overrun, parity, framing error)	
3FAh	2FAh	<1> Tx holding register empty interrupt enable (active high)	
		<0> Baud rate divisor interrupt enable (active high)	
		Interrupt ID Register:	R
		<7,6> FIFO Enable/Disable: 0 = disable, 1 = enable	
		<5,4> Reserved	
		<3..1> Interrupt Source:	
		000 = Modem status 100,101 = Reserved	
		001 = TX holding reg. Empty 110 = Character time-out	
		010 = RX data available 111 = Reserved	
		011 = RX line status	
3FBh	2FBh	<0> Interrupt pending (if cleared)	
		FIFO Control Register:	W
		<7,6> RX Trigger Level: 00 = 1 byte, 01 = 4 bytes, 10 = 8 bytes, 11 = 14 bytes	
		<5..3> Reserved	
		<2> TX FIFO reset (active high)	
		<1> RX FIFO reset (active high)	
3FCh	2FCh	<0> FIFO Enable/Disable: 0 = Disable TX/RX FIFO's, 1 = Enable TX/RX FIFO's	
		Line Control Register:	R/W
		<7> Register access control:	
		0 = RX buffer, TX holding, divisor rate registers are accessible.	
		1 = Divisor rate register is accessible	
		<6> Break control (forces SOUT single low if set)	
		<5> Stick parity (if set, even parity bit is 0, odd parity bit is 1)	
		<4> Parity type: 0 = odd, 1 = even	
		<3> Parity enable: 0 = disabled, 1 = enabled	
		<2> Stop bit: 0 = 1 stop bit, 1 = 2 stop bits	
3FDh	2FDh	<1,0> Word size: 00 = 5 bits, 01 = 6 bits, 10 = 7 bits, 11 = 8 bits	
		Modem Control Register:	R/W
		<7..5> Reserved	
		<4> Internal loopback enabled (if set)	
		<3> Serial I/F interrupts enabled (if set)	
		<2> Reserved	
3FEh	2FEh	<1> RTS signal active (if set)	
		<0> DTR signal active (if set)	
		Line Status Register:	R
		<7> Parity error, framing error, or Break condition (if set)	
		<6> TX holding and TX shift registers are empty (if set)	
		<5> TX holding register is empty (if set)	
3FEh	2FEh	<4> Break interrupt has occurred (if set)	
		<3> Framing error has occurred (if set)	
		<2> Parity error has occurred (if set)	
		<1> Overrun error has occurred (if set)	
		<0> Data register ready to be read (if set)	
		Modem Status:	R
		<7..4> DCD-, RI-, DSR, CTS (respectively) active (if set)	
		<3..0> DCD-, RI-, DSR, CTS (respectively) changed state since last read (if set)	

5.5 PARALLEL INTERFACE

The parallel interface provides connection to a peripheral device that has a compatible interface, the most common being a printer. The parallel interface function is integrated into the 87307 I/O controller component and provides bi-directional 8-bit parallel data transfers with a peripheral device. The parallel interface supports three main modes of operation:

- ◆ Standard Parallel Port (SPP) mode
- ◆ Enhanced Parallel Port (EPP) mode
- ◆ Extended Capabilities Port (ECP) mode

These three modes (and their submodes) provide complete support as specified for an IEEE 1284 parallel port.

5.5.1 STANDARD PARALLEL PORT MODE

The Standard Parallel Port (SPP) mode uses software-based protocol and includes two sub-modes of operation, compatible and extended, both of which can provide data transfers up to 150 KB/s. In the compatible mode, CPU write data is simply presented on the eight data lines. A CPU read of the parallel port yields the last data byte that was written.

The following steps define the standard procedure for communicating with a printing device:

1. The system checks the Printer Status register. If the Busy, Paper Out, or Printer Fault signals are indicated as being active, the system either waits for a status change or generates an error message.
2. The system sends a byte of data to the Printer Data register, then pulses the printer STROBE signal (through the Printer Control register) for at least 500 ns.
3. The system then monitors the Printer Status register for acknowledgment of the data byte before sending the next byte.

In extended mode, a direction control bit (CTR 37Ah, bit <5>) controls the latching of output data while allowing a CPU read to fetch data present on the data lines, thereby providing bi-directional parallel transfers to occur.

The SPP mode uses three registers for operation: the Data register (DTR), the Status register (STR) and the Control register (CTR). Address decoding in SPP mode includes address lines A0 and A1.

5.5.2 ENHANCED PARALLEL PORT MODE

In Enhanced Parallel Port (EPP) mode, increased data transfers are possible (up to 2 MB/s) due to a hardware protocol that provides automatic address and strobe generation. EPP revisions 1.7 and 1.9 are both supported. For the parallel interface to be initialized for EPP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with EPP mode. If compatible, then EPP mode can be used. In EPP mode, system timing is closely coupled to EPP timing. A watchdog timer is used to prevent system lockup.

Five additional registers are available in EPP mode to handle 16- and 32-bit CPU accesses with the parallel interface. Address decoding includes address lines A0, A1, and A2.

5.5.3 EXTENDED CAPABILITIES PORT MODE

The Extended Capabilities Port (ECP) mode, like EPP, also uses a hardware protocol-based design that supports transfers up to 2 MB/s. Automatic generation of addresses and strobes as well as Run Length Encoding (RLE) decompression is supported by ECP mode. The ECP mode includes a bi-directional FIFO buffer that can be accessed by the CPU using DMA or programmed I/O. For the parallel interface to be initialized for ECP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with ECP mode. If compatible, then ECP mode can be used.

Ten control registers are available in ECP mode to handle transfer operations. In accessing the control registers, the base address is determined by address lines A2-A9, with lines A0, A1, and A10 defining the offset address of the control register. Registers used for FIFO operations are accessed at their base address + 400h (i.e., if configured for LPT1, then 378h + 400h = 778h).

The ECP mode includes several sub-modes as determined by the Extended Control register. Two submodes of ECP allow the parallel port to be controlled by software. In these modes, the FIFO is cleared and not used, and DMA and RLE are inhibited.

5.5.4 PARALLEL INTERFACE PROGRAMMING

Programming the parallel interface consists of configuration, which typically occurs during POST, and control, which occurs during runtime.

5.5.4.1 Parallel Interface Configuration

The parallel interface must be configured for a specific address range (LPT1, LPT2, etc.) and also must be enabled before it can be used. When configured for EPP or ECP mode, additional considerations must be taken into account. Address selection, enabling, and EPP/ECP mode parameters of the parallel interface are affected through the PnP configuration registers of the LPC47B347 I/O controller. Address selection and enabling are automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The PnP configuration registers are accessed through I/O registers 15Ch (index) and 15Dh (data). The parallel interface is initiated by firmware selecting logical device 3 of the LPC47B347. This is accomplished by the following sequence:

1. Write 07h to I/O register 02Eh.
2. Write 03h to I/O register 02Fh (for selecting the parallel interface).
3. Write 30h to I/O register 02Eh.
4. Write 01h to I/O register 02Fh (this activates the interface).

The parallel interface configuration registers are listed in the following table:

Table 5-11.
Parallel Interface Configuration Registers

Index Address	Function	R/W	Reset Value
30h	Activate	R/W	00h
60h	Base Address MSB	R/W	00h
61h	Base Address LSB	R/W	00h
70h	Interrupt Select	R/W	00h
74h	DMA Channel Select	R/W	04h
F0h	Mode Register	R/W	00h
F1h	Mode Register 2	R/W	00h

5.5.4.2 Parallel Interface Control

The BIOS function INT 17 provides simplified control of the parallel interface. Basic functions such as initialization, character printing, and printer status are provided by subfunctions of INT 17. The parallel interface is controllable by software through a set of I/O mapped registers. The number and type of registers available depends on the mode used (SPP, EPP, or ECP). Table 5-12 lists the parallel registers and associated functions based on mode.

Table 5-12.
Parallel Interface Control Registers

I/O Address	Register	SPP Mode Ports	EPP Mode Ports	ECP Mode Ports
Base	Data	LPT1,2,3	LPT1,2	LPT1,2,3
Base + 1h	Printer Status	LPT1,2,3	LPT1,2	LPT1,2,3
Base + 2h	Control	LPT1,2,3	LPT1,2	LPT1,2,3
Base + 3h	Address	--	LPT1,2	--
Base + 4h	Data Port 0	--	LPT1,2	--
Base + 5h	Data Port 1	--	LPT1,2	--
Base + 6h	Data Port 2	--	LPT1,2	--
Base + 7h	Data Port 3	--	LPT1,2	--
Base + 400h	Parallel Data FIFO	--	--	LPT1,2,3
Base + 400h	ECP Data FIFO	--	--	LPT1,2,3
Base + 400h	Test FIFO	--	--	LPT1,2,3
Base + 400h	Configuration Register A	--	--	LPT1,2,3
Base + 401h	Configuration Register B	--	--	LPT1,2,3
Base + 402h	Extended Control Register	--	--	LPT1,2,3

Base Address:

LPT1 = 378h
LPT2 = 278h
LPT3 = 3BCh

The following paragraphs describe the individual registers. Note that only the LPT1-based addresses are given in these descriptions.

Data Register, I/O Port 378h

Data written to this register is presented to the data lines D0-D7. A read of this register when in SPP-compatible mode yields the last byte written. A read while in SPP-extended or ECP mode yields the status of data lines D0-D7 (i.e., receive data).

In ECP mode in the forward (output) direction, a write to this location places a tagged command byte into the FIFO and reads have no effect.

Status Register, I/O Port 379h, Read Only

This register contains the current printer status. Reading this register clears the interrupt condition of the parallel port.

Bit	Function
7	Printer Busy (if 0)
6	Printer Acknowledgment Of Data Byte (if 0)
5	Printer Out Of Paper (if 1)
4	Printer Selected/Online (if 1)
3	Printer Error (if 0)
2	Reserved
1	EPP Interrupt Occurred (if set while in EPP mode)
0	EPP Timeout Occurred (if set while in EPP mode)

Control Register, I/O Port 37Ah

This register provides the printer control functions.

Bit	Function
7,6	Reserved
5	Direction Control for PS/2 and ECP Modes: 0 = Forward. Drivers enabled. Port writes to peripheral (default) 1 = Backward. Tristates drivers and data is read from peripheral
4	Acknowledge Interrupt Enable 0 = Disable ACK interrupt 1 = Enable interrupt on rising edge of ACK
3	Printer Select (if 0)
2	Printer Initialize (if 1)
1	Printer Auto Line Feed (if 0)
0	Printer Strobe (if 0)

Address Register, I/O Port 37Bh (EPP Mode Only)

This register is used for selecting the EPP register to be accessed.

Data Port Registers 0-3, I/O Ports 37C-Fh (EPP Mode Only)

These registers are used for reading/writing data. Port 0 is used for all transfers. Ports 1-3 are used for transferring the additional bytes of 16- or 32-bit transfers through port 0.

FIFO Register, I/O Port 7F8h (ECP Mode Only)

While in ECP/forward mode, this location is used for filling the 16-byte FIFO with data bytes. Reads have no effect (except when used in Test mode). While in ECP/backward mode, reads yield data bytes from the FIFO.

Configuration Register A, I/O Port 7F8h (ECP Mode Only)

A read of this location yields 10h, while writes have no effect.

Configuration Register B, I/O Port 7F9h (ECP Mode, Read Only)

A read of this location yields the status defined as follows:

Bit	Function
7	Reserved (always 0)
6	Status of Selected IRQn.
5,4	Selected IRQ Indicator: 00 = IRQ7 11 = IRQ5 All other values invalid.
3	Reserved (always 1)
2..0	Reserved (always 000)

Extended Control Register B, I/O Port 7FAh (ECP ModeOnly)

This register defines the ECP mode functions.

Bit	Function
7..5	ECP Submode Select: 000 = Standard forward mode (37Ah <5> forced to 0). Writes are controlled by software and FIFO is reset. 001 = PS/2 mode. Reads and writes are software controlled and FIFO is reset. 010 = Parallel Port FIFO forward mode (37Ah <5> forced to 0). Writes are hardware controlled. 011 = ECP FIFO mode. Direction determined by 37Ah, <5>. Reads and writes are hardware controlled.
4	ECP Interrupt Mask: 0 = Interrupt is generated on ERR- assertion. 1 = Interrupt is inhibited.
3	ECP DMA Enable/Disable. 0 = Disabled 1 = Enabled
2	ECP Interrupt Generation with DMA 0 = Enabled 1 = Disabled
1	FIFO Full Status (Read Only) 0 = Not full (at least 1 empty byte) 1 = Full
0	FIFO Empty Status (Read Only) 0 = Not empty (contains at least 1 byte) 1 = Empty

5.5.5 PARALLEL INTERFACE CONNECTOR

Figure 5-5 and Table 5-13 show the connector and pinout of the parallel interface connector. Note that some signals are redefined depending on the port's operational mode.

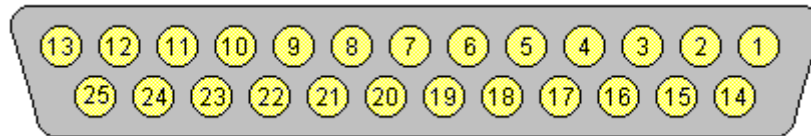


Figure 5-5. Parallel Interface Connector (Female DB-25 as viewed from rear of chassis)

Table 5-13.
DB-25 Parallel Connector Pinout

Pin	Signal	Function	Pin	Signal	Function
1	STB-	Strobe / Write [1]	14	LF-	Line Feed [2]
2	D0	Data 0	15	ERR-	Error [3]
3	D1	Data 1	16	INIT-	Initialize Paper [4]
4	D2	Data 2	17	SLCTIN-	Select In / Address. Strobe [1]
5	D3	Data 3	18	GND	Ground
6	D4	Data 4	19	GND	Ground
7	D5	Data 5	20	GND	Ground
8	D6	Data 6	21	GND	Ground
9	D7	Data 7	22	GND	Ground
10	ACK-	Acknowledge / Interrupt [1]	23	GND	Ground
11	BSY	Busy / Wait [1]	24	GND	Ground
12	PE	Paper End / User defined [1]	25	GND	Ground
13	SLCT	Select / User defined [1]	--	--	--

NOTES:

[1] Standard and ECP mode function / EPP mode function

[2] EPP mode function: Data Strobe

ECP modes: Auto Feed or Host Acknowledge

[3] EPP mode: user defined

ECP modes: Fault or Peripheral Req.

[4] EPP mode: Reset

ECP modes: Initialize or Reverse Req.

5.6 KEYBOARD/POINTING DEVICE INTERFACE

The keyboard/pointing device interface provides the connection of an enhanced keyboard and a mouse using PS/2-type connections. The keyboard/pointing device interface function is provided by the LPC47B347 I/O controller component, which integrates 8042-compatible keyboard controller logic (hereafter referred to as simply the “8042”) to communicate with the keyboard and pointing device using bi-directional serial data transfers. The 8042 handles scan code translation and password lock protection for the keyboard as well as communications with the pointing device. This section describes the interface itself. The keyboard is discussed in the Appendix C.

5.6.1 KEYBOARD INTERFACE OPERATION

The data/clock link between the 8042 and the keyboard is uni-directional for Keyboard Mode 1 and bi-directional for Keyboard Modes 2 and 3. (These modes are discussed in detail in Appendix C). This section describes Mode 2 (the default) mode of operation.

Communication between the keyboard and the 8042 consists of commands (originated by either the keyboard or the 8042) and scan codes from the keyboard. A command can request an action or indicate status. The keyboard interface uses IRQ1 to get the attention of the CPU.

The 8042 can send a command to the keyboard at any time. When the 8042 wants to send a command, the 8042 clamps the clock signal from the keyboard for a minimum of 60 μ s. If the keyboard is transmitting data at that time, the transmission is allowed to finish. When the 8042 is ready to transmit to the keyboard, the 8042 pulls the data line low, causing the keyboard to respond by pulling the clock line low as well, allowing the start bit to be clocked out of the 8042. The data is then transferred serially, LSb first, to the keyboard (Figure 5-6). An odd parity bit is sent following the eighth data bit. After the parity bit is received, the keyboard pulls the data line low and clocks this condition to the 8042. When the keyboard receives the stop bit, the clock line is pulled low to inhibit the keyboard and allow it to process the data.

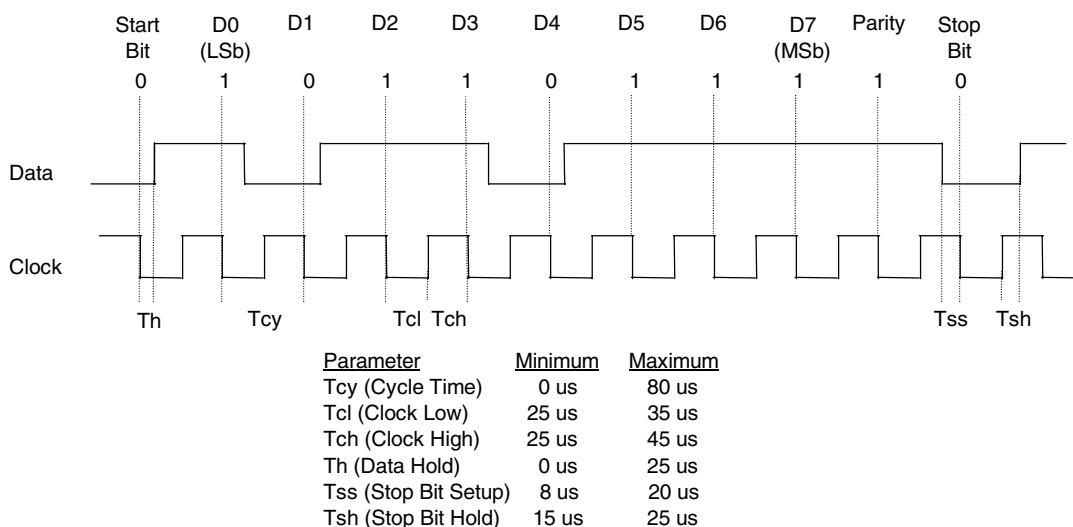


Figure 5-6. 8042-To-Keyboard Transmission of Code EDh, Timing Diagram

Control of the data and clock signals is shared by the 8042 and the keyboard depending on the originator of the transferred data. Note that the clock signal is always generated by the keyboard. After the keyboard receives a command from the 8042, the keyboard returns an ACK code. If a parity error or timeout occurs, a Resend command is sent to the 8042.

Table 5-14 lists and describes commands that can be issued by the 8042 to the keyboard.

Table 5-14.
8042-To-Keyboard Commands

Command	Value	Description
Set/Reset Status Indicators	EDh	Enables LED indicators. Value EDh is followed by an option byte that specifies the indicator as follows: Bits <7..3> not used Bit <2>, Caps Lock (0 = off, 1 = on) Bit <1>, NUM Lock (0 = off, 1 = on) Bit <0>, Scroll Lock (0 = off, 1 = on)
Echo	EEh	Keyboard returns EEh when previously enabled.
Invalid Command	EFh/F1h	These commands are not acknowledged.
Select Alternate Scan Codes	F0h	Instructs the keyboard to select another set of scan codes and sends an option byte after ACK is received: 01h = Mode 1 02h = Mode 2 03h = Mode 3
Read ID	F2h	Instructs the keyboard to stop scanning and return two keyboard ID bytes.
Set Typematic Rate/Display	F3h	Instructs the keyboard to change typematic rate and delay to specified values: Bit <7>, Reserved - 0 Bits <6,5>, Delay Time 00 = 250 ms 01 = 500 ms 10 = 750 ms 11 = 1000 ms Bits <4..0>, Transmission Rate: 00000 = 30.0 ms 00001 = 26.6 ms 00010 = 24.0 ms 00011 = 21.8 ms : 11111 = 2.0 ms
Enable	F4h	Instructs keyboard to clear output buffer and last typematic key and begin key scanning.
Default Disable	F5h	Resets keyboard to power-on default state and halts scanning pending next 8042 command.
Set Default	F6h	Resets keyboard to power-on default state and enable scanning.
Set Keys - Typematic	F7h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make/Brake	F8h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make	F9h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Typematic/Make/Brake	FAh	Clears keyboard buffer and sets default scan code set. [1]
Set Type Key - Typematic	FBh	Clears keyboard buffer and prepares to receive key ID. [1]
Set Type Key - Make/Brake	FCh	Clears keyboard buffer and prepares to receive key ID. [1]
Set Type Key - Make	FDh	Clears keyboard buffer and prepares to receive key ID. [1]
Resend	FEh	8042 detected error in keyboard transmission.
Reset	FFh	Resets program, runs keyboard BAT, defaults to Mode 2.

Note:

[1] Used in Mode 3 only.

5.6.2 POINTING DEVICE INTERFACE OPERATION

The pointing device (typically a mouse) connects to a 6-pin DIN-type connector that is identical to the keyboard connector both physically and electrically. The operation of the interface (clock and data signal control) is the same as for the keyboard. The pointing device interface uses the IRQ12 interrupt.

5.6.3 KEYBOARD/POINTING DEVICE INTERFACE PROGRAMMING

Programming the keyboard interface consists of configuration, which occurs during POST, and control, which occurs during runtime.

5.6.3.1 8042 Configuration

The keyboard/pointing device interface must be enabled and configured for a particular speed before it can be used. Enabling and speed parameters of the 8042 logic are affected through the PnP configuration registers of the LPC47B347 I/O controller. Enabling and speed control are automatically set by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The PnP configuration registers are accessed through I/O registers 02Eh (index) and 02Fh (data). The keyboard and mouse interfaces are initiated by firmware selecting logical device 7 of the LPC47B347. This is accomplished by the following sequence:

1. Write 07h to I/O register 02Eh.
2. Write 07h to I/O register 02Fh (for selecting the keyboard interface).
3. Write 30h to I/O register 02Eh.
4. Write 01h to I/O register 02Fh (this activates the interface).

The keyboard interface configuration registers are listed in the following table:

Table 5-15.		
Keyboard Interface Configuration Registers		
Index		
Address	Function	R/W
30h	Activate	R/W
70h	Primary Interrupt Select	R/W
72h	Secondary Interrupt Select	R/W
F0h	Reset and A20 Select	R/W

5.6.3.2 8042 Control

The BIOS function INT 16 is typically used for controlling interaction with the keyboard. Sub-functions of INT 16 conduct the basic routines of handling keyboard data (i.e., translating the keyboard's scan codes into ASCII codes). The keyboard/pointing device interface is accessed by the CPU through I/O mapped ports 60h and 64h, which provide the following functions:

- ◆ Output buffer reads
- ◆ Input buffer writes
- ◆ Status reads
- ◆ Command writes

Ports 60h and 64h can be accessed using the IN instruction for a read and the OUT instruction for a write. Prior to reading data from port 60h, the "Output Buffer Full" status bit (64h, bit <0>) should be checked to ensure data is available. Likewise, before writing a command or data, the "Input Buffer Empty" status bit (64h, bit <1>) should also be checked to ensure space is available.

I/O Port 60h

I/O port 60h is used for accessing the input and output buffers. This register is used to send and receive data from the keyboard and the pointing device. This register is also used to send the second byte of multi-byte commands to the 8042 and to receive responses from the 8042 for commands that require a response.

A read of 60h by the CPU yields the byte held in the output buffer. The output buffer holds data that has been received from the keyboard and is to be transferred to the system.

A CPU write to 60h places a data byte in the input byte buffer and sets the CMD/ DATA bit of the Status register to DATA. The input buffer is used for transferring data from the system to the keyboard. All data written to this port by the CPU will be transferred to the keyboard **except** bytes that follow a multibyte command that was written to 64h

I/O Port 64h

I/O port 64h is used for reading the status register and for writing commands. A read of 64h by the CPU will yield the status byte defined as follows:

Bit	Function
7..4	General Purpose Flags.
3	CMD/DATA Flag (reflects the state of A2 during a CPU write). 0 = Data 1 = Command
2	General Purpose Flag.
1	Input Buffer Full. Set (to 1) upon a CPU write. Cleared by IN A, DBB instruction.
0	Output Buffer Full (if set). Cleared by a CPU read of the buffer.

A CPU write to I/O port 64h places a command value into the input buffer and sets the CMD/DATA bit of the status register (bit <3>) to CMD.

Table 5-16 lists the commands that can be sent to the 8042 by the CPU. The 8042 uses IRQ1 for gaining the attention of the CPU.

Table 5-16.
CPU Commands To The 8042

Value	Command Description
20h	Put current command byte in port 60h.
60h	Load new command byte. This is a two-byte operation described as follows: <ol style="list-style-type: none"> Write 60h to port 64h. Write the command byte to port 60h as follows: <ul style="list-style-type: none"> Bit <7> Reserved <6> Keyboard Code Conversion <ul style="list-style-type: none"> 0 = Do not convert codes 1 = Convert codes to 9-bit 8088/8086-compatible format Bit <5> Pointing Device Enable <ul style="list-style-type: none"> 0 = Enable pointing device 1 = Disable pointing device Bit <4> Keyboard Enable <ul style="list-style-type: none"> 0 = Enable keyboard 1 = Disable keyboard Bit <3> Reserved Bit <2> System Flag <ul style="list-style-type: none"> 0 = Cold boot 1 = CPU reset (exit from protected mode) Bit <1> Pointing Device Interrupt Enable <ul style="list-style-type: none"> 0 = Disable interrupt 1 = Enable interrupt Bit <0> Keyboard Interrupt Enable <ul style="list-style-type: none"> 0 = Disable interrupt 1 = Enable interrupt
A4h	Test password installed. Tests whether or not a password is installed in the 8042: If FAh is returned, password is installed. If F1h is returned, no password is installed.
A5h	Load password. This multi-byte operation places a password in the 8042 using the following manner: <ol style="list-style-type: none"> Write A5h to port 64h. Write each character of the password in 9-bit scan code (translated) format to port 60h. Write 00h to port 60h.
A6h	Enable security. This command places the 8042 in password lock mode following the A5h command. The correct password must then be entered before further communication with the 8042 is allowed.
A7h	Disable pointing device. This command sets bit <5> of the 8042 command byte, pulling the clock line of the pointing device interface low.
A8h	Enable pointing device. This command clears bit <5> of the 8042 command byte, activating the clock line of the pointing device interface.
A9h	Test the clock and data lines of the pointing device interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
AAh	Initialization. This command causes the 8042 to inhibit the keyboard and pointing device and places 55h into the output buffer.
ABh	Test the clock and data lines of the keyboard interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
ADh	Disable keyboard command (sets bit <4> of the 8042 command byte).
AEnh	Enable keyboard command (clears bit <4> of the 8042 command byte).

Continued

Table 5-16. CPU Commands To The 8042 (*Continued*)

Value	Command Description
C0h	Read input port of the 8042. This command directs the 8042 to transfer the contents of the input port to the output buffer so that they can be read at port 60h. The contents are as follows: Bit <7> Password Enable: 0 = Disabled 1 = Enabled Bit <6> External Boot Enable: 0 = Enabled 1 = Disabled Bit <5> Setup Enable: 0 = Enabled 1 = Disabled Bit <4> VGA Enable: 0 = Enabled 1 = Disabled Bit <3> Diskette Writes: 0 = Disabled 1 = Enabled Bit <2> Reserved Bit <1> Pointing Device Data Input Line Bit <0> Keyboard Data Input Line
C2h	Poll Input Port High. This command directs the 8042 to place bits <7..4> of the input port into the upper half of the status byte on a continuous basis until another command is received.
C3h	Poll Input Port Low. This command directs the 8042 to place bits <3..0> of the input port into the lower half of the status byte on a continuous basis until another command is received.
D0h	Read output port. This command directs the 8042 to transfer the contents of the output port to the output buffer so that they can be read at port 60h. The contents are as follows: Bit <7> Keyboard data stream Bit <6> Keyboard clock Bit <5> IRQ12 (pointing device interrupt) Bit <4> IRQ1 (keyboard interrupt) Bit <3> Pointing device clock Bit <2> Pointing device data Bit <1> A20 Control: 0 = Hold A20 low 1 = Enable A20 Bit <0> Reset Line Status; 0 = Inactive 1 = Active
D1h	Write output port. This command directs the 8042 to place the next byte written to port 60h into the output port (only bit <1> can be changed).
D2h	Echo keyboard data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the keyboard. No 11-to-9 bit translation takes place but an interrupt (IRQ1) is generated if enabled.
D3h	Echo pointing device data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the pointing device. An interrupt (IRQ12) is generated if enabled.
D4h	Write to pointing device. Directs the 8042 to send the next byte written to 60h to the pointing device.
E0h	Read test inputs. Directs the 8042 to transfer the test bits 1 and 0 into bits <1,0> of the output buffer.
F0h-FFh	Pulse output port. Controls the pulsing of bits <3..0> of the output port (0 = pulse, 1 = don't pulse). Note that pulsing bit <0> will reset the system.

5.6.4 KEYBOARD/POINTING DEVICE INTERFACE CONNECTOR

There are separate connectors for the keyboard and pointing device. Both connectors are identical both physically and electrically. Figure 5-7 and Table 5-17 show the connector and pinout of the keyboard/pointing device interface connectors.

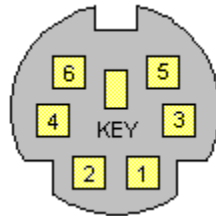


Figure 5-7. Keyboard or Pointing Device Interface Connector
(as viewed from rear of chassis)

Table 5-17.
Keyboard/Pointing Device Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	DATA	Data	4	+ 5 VDC	Power
2	NC	Not Connected	5	CLK	Clock
3	GND	Ground	6	NC	Not Connected

5.7 UNIVERSAL SERIAL BUS INTERFACE

The Universal Serial Bus (USB) interface provides up to 12 Mb/s data transfers between the host system and peripherals designed with a compatible USB interface. This high speed interface supports hot-plugging of compatible devices, making possible system configuration changes without powering down or even rebooting systems. The USB interface supports both isochronous and asynchronous communications, and integrates a 5-VDC power bus that can eliminate the need for external powering of small remote peripherals. The USB interface function is provided by the 82801 ICH component of the chipset.

5.7.1 USB KEYBOARD CONSIDERATIONS

The BIOS ROM checks the USB port, during POST, for the presence of a USB keyboard. This allows a system with only a USB keyboard to be used during ROM-based setup and also on a system with an OS that does not include a USB driver.

On such a system a keystroke will generate an SMI and the SMI handler will retrieve the data from the device and convert it to PS/2 data. The data will be passed to the keyboard controller and processed as in the PS/2 interface. Changing the delay and/or typematic rate of a USB keyboard though BIOS function INT 16 is not supported.

The system does not support hot-plugging of a USB keyboard, nor is a keyboard attached to a USB hub supported. A PS/2 keyboard and a USB keyboard can, however, be connected and used simultaneously.

5.7.2 USB CONFIGURATION

The USB interface functions as a PCI device (31) within the 82801 component (function 2) and is configured using PCI Configuration Registers as listed in Table 5-18.

Table 5-18.
USB Interface Configuration Registers

PCI Config. Addr.	Register	Reset Value	PCI Config. Addr.	Register	Reset Value
00, 01h	Vendor ID	8086h	0Dh	Latency Timer	00h
02, 03h	Device ID	2412h	0Eh	Header Type	00h
04, 05h	PCI Command	0000h	20-23h	I/O Space Base Address	1h
06, 07h	PCI Status	0280h	3Ch	Interrupt Line	00h
08h	Revision ID	00h	3Dh	Interrupt Pin	04h
09h	Programming I/F	00h	60h	Miscellaneous Control 1	10h
0Ah	Sub Class Code	03h	C0, C1h	Miscellaneous Control 2	2000h
0Bh	Base Class Code	0Ch	C4h	USB Resume Enable	00h

NOTES:

Assume unmarked locations/gaps as reserved.

Refer to applicable Intel documentation for detailed descriptions of registers.

5.7.3 USB CONTROL

The USB is controlled through I/O registers as listed in table 5-19.

Table 5-19.
USB Control Registers

I/O Addr.	Register	Default Value
00, 01h	Command	0000h
02, 03h	Status	0000h
04, 05h	Interrupt Enable	0000h
06, 07	Frame Number	0000h
08, 0B	Frame List Base Address	0000h
0Ch	Start of Frame Modify	40h
10, 11h	Port 1 Status/Control	0080h
12, 13h	Port 2 Status/Control	0080h
18h	Test Data	00h

5.7.4 USB CONNECTOR

The USB interface provides two identical connectors (ports A and B).

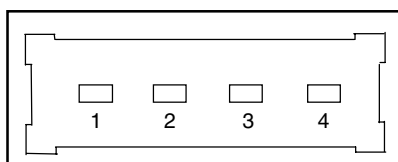


Figure 5-8. Universal Serial Bus Connector (one of two as viewed from rear of chassis)

Table 5-20.
USB Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	Vcc	+5 VDC	3	USB+	Data (plus)
2	USB-	Data (minus)	4	GND	Ground

5.8 AUDIO SUBSYSTEM

A PCI audio subsystem is integrated onto the system board of all Compaq Deskpros covered in this guide. Implementing AC'97 design guidelines, the audio subsystem features Compaq Premier Sound components designed to provide optimum sound. Key features of the audio subsystem include:

- ◆ AC'97 ver. 2.1 compliance
- ◆ Multiple audio channel streaming
- ◆ Soft CD, DVD/AC-3 processing
- ◆ Wavetable synthesis utilizing system memory
- ◆ Acoustic echo cancellation
- ◆ 16-bit stereo PCM input and output w/ up to 48 KHz sampling
- ◆ Compaq Premier Sound components

5.8.1 FUNCTIONAL ANALYSIS

A block diagram of the audio subsystem is shown in Figure 5-9. The architecture uses the AC'97 Audio Controller of the 82801 ICH component to access and control an Analog Devices AD1881 Audio Codec, which provides the analog-to-digital (ADC) and digital-to-analog (DAC) conversions as well as the mixing functions.

All control functions such as volume, audio source selection, and sampling rate are controlled through software over the PCI bus through the AC97 Audio Controller of the 82801 ICH. Control data and digital audio streams (record and playback) are transferred between the Audio Controller and the Audio Codec over the AC97 Link Bus. Playback audio from the Audio Codec is processed through an equalizer designed to compensate for chassis acoustics. A 5-watt low-distortion amplifier (TDA7056A) drives a long-excursion large-magnet speaker for optimum sound.

The analog interfaces allowing connection to external audio devices are discussed in the following paragraphs.

Mic In - This input uses a three-conductor (stereo) mini-jack that is specifically designed for connection of a condenser microphone with an impedance of 10-K ohms. This is the default recording input after a system reset.

Line In - This input uses a three-conductor (stereo) mini-jack that is specifically designed for connection of a high-impedance (10k-ohm) audio source such as a tape deck.

Headphones Out - This input uses a three-conductor (stereo) mini-jack that is specifically designed for connecting a set of 16-ohm (nom.) stereo headphones. Plugging into the Headphones jack mutes the signal to the internal speaker and the Line Out jack.

Line Out - This output uses a three-conductor (stereo) mini-jack for connecting left and right channel line-level signals (20-K ohm impedance). A typical connection would be to a tape recorder's Line In (Record In) jacks, an amplifier's Line In jacks, or to "powered" speakers that contain amplifiers. Plugging into the Line Out mutes the internal speaker.

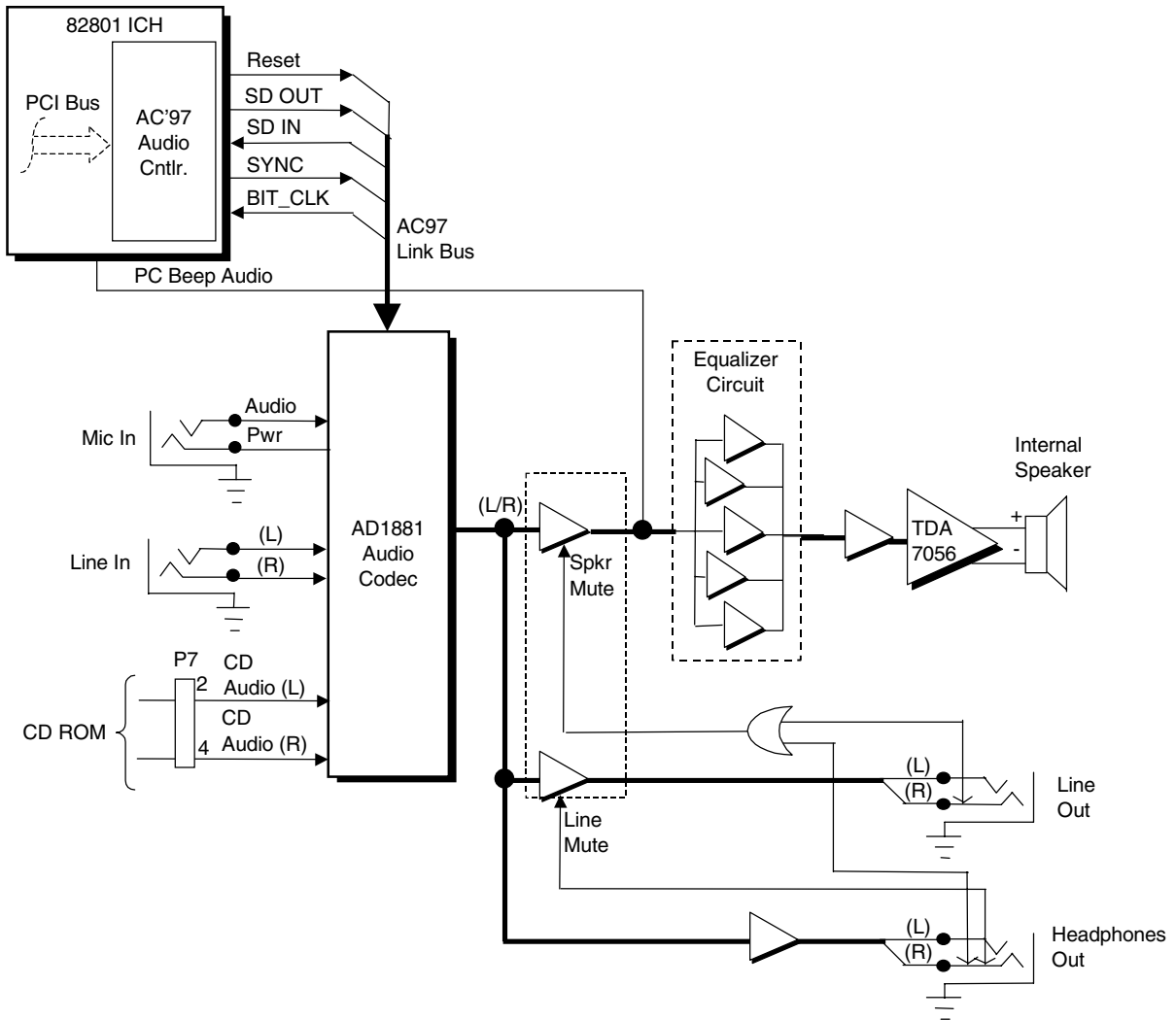


Figure 5-9. Audio Subsystem Block Diagram

Legacy beep audio originates from the 82801 ICH and is applied to the equalizer circuit, bypassing the audio codec so that basic support of beep codes produced during POST is maintained.

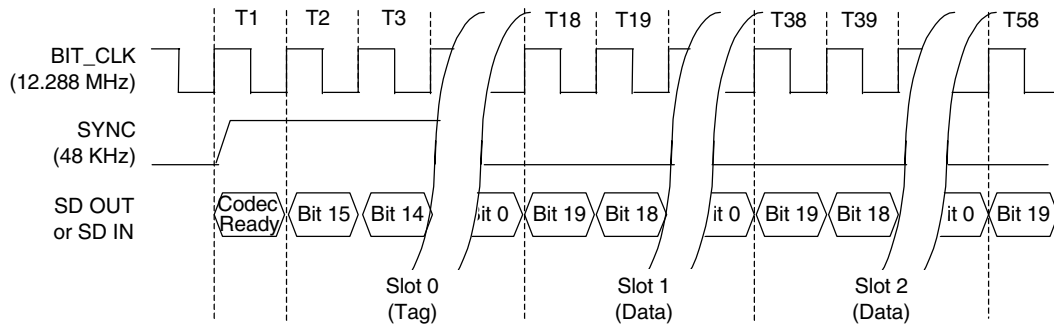
5.8.2 AC97 AUDIO CONTROLLER

The AC97 Audio Controller is a PCI device (device 31/function 5) that is integrated into the 82801 ICH component and supports the following functions:

- ◆ Read/write access to audio codec registers
- ◆ 16-bit stereo PCM output @ up to 48 KHz sampling
- ◆ 16-bit stereo PCM input @ up to 48 KHz sampling
- ◆ Acoustic echo correction for microphone
- ◆ AC'97 Link Bus
- ◆ ACPI power management

5.8.3 AC97 LINK BUS

The audio controller and the audio codec communicate over a five-signal AC97 Link Bus (Figure 5-10). The AC97 Link Bus includes two serial data lines (SD OUT/SD IN) that transfer control and PCM audio data serially to and from the audio codec using a time-division multiplexed (TDM) protocol. The data lines are qualified by a 12.288 MHz BIT_CLK signal driven by the audio codec. Data is transferred in frames synchronized by the 48-KHz SYNC signal, which is derived from the clock signal and driven by the audio controller. The SYNC signal is high during the frame's tag phase then falls during T17 and remains low during the data phase. A frame consists of one 16-bit tag slot followed by twelve 20-bit data slots. When asserted (typically during a power cycle), the RESET- signal (not shown) will reset all audio registers to their default values.



Slot	Description
0	Bit 15: Frame valid bit Bits 14-3: Slots 1-12 valid bits Bits 2-0: Codec ID
1	Command address: Bit 19, R/W; Bits 18..12, reg. Index; Bits 11..0, reserved.
2	Command data
3	Bits 19-4: PCM audio data, left channel (SD OUT, playback; SD IN, record) Bits 3-0 all zeros
4	Bits 19-4: PCM audio data, right channel (SD OUT, playback; SD IN, record) Bits 3-0 all zeros
5	Modem codec data (not used in this system)
6-11	Reserved
12	I/O control

Figure 5-10. AC'97 Link Bus Protocol

5.8.4 AUDIO CODEC

The audio codec provides pulse code modulation (PCM) coding and decoding of audio information as well as the selection and/or mixing of analog channels. As shown in Figure 5-11, analog audio from a microphone, tape, or CD can be selected and, if to be recorded (saved) onto a disk drive, routed through an analog-to-digital converter (ADC). The resulting left and right PCM record data are muxed into a time-division-multiplexed (TDM) data stream (SD IN signal) that is routed to the audio controller. Playback (PB) audio takes the reverse path from the audio controller to the audio codec as SD OUT data and is decoded and processed by the digital-to-analog converter (DAC). The codec supports simultaneous record and playback of stereo (left and right) audio. The Sample Rate Generator may be set for sampling frequencies up to 48 KHz.

Analog audio may then be routed through 3D stereo enhancement processor or bypassed to the output selector (SEL). The integrated analog mixer provides the computer control-console functionality handling multiple audio inputs.

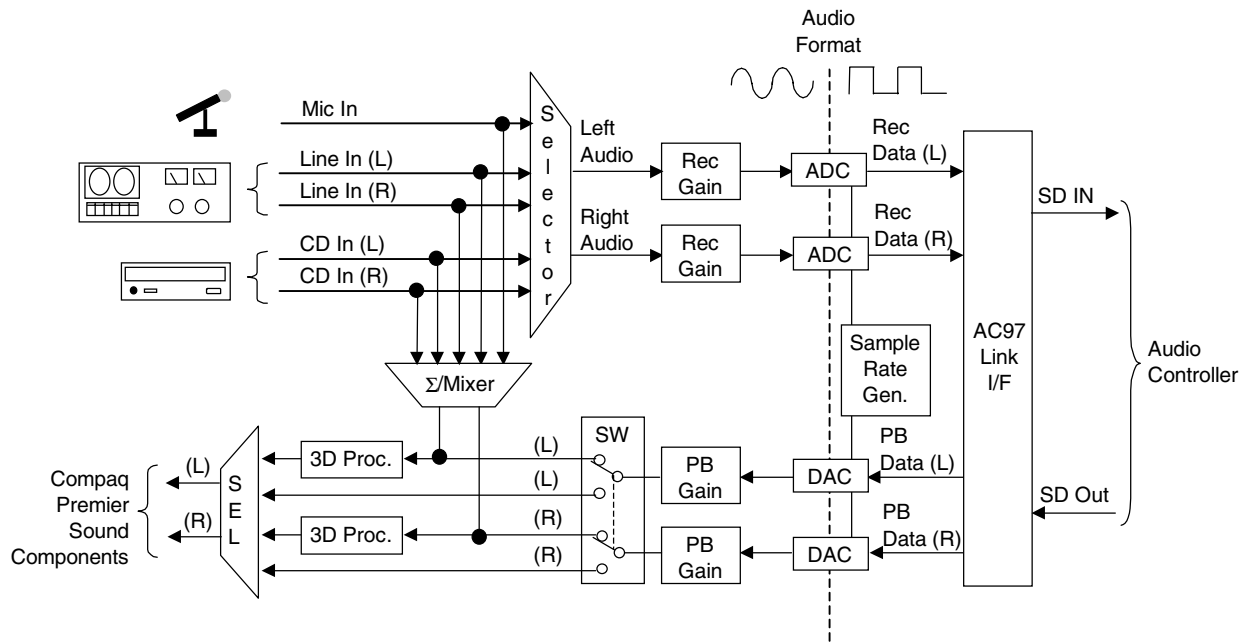


Figure 5-11. AD1881 Audio Codec Functional Block Diagram

All inputs and outputs are two-channel stereo except for the microphone input, which is inputted as a single-channel but mixed internally onto both left and right channels. The microphone input is the default active input. All block functions are controlled through index-addressed registers of the codec.

5.8.5 COMPAQ PREMIER SOUND COMPONENTS

The left and right channel outputs of the audio codec are distributed to Line Out amplifiers, Headphone amplifiers, and Compaq Premier Sound Components. Compaq Premier Sound components include the following:

- ◆ Equalization circuitry
- ◆ Power amplifier
- ◆ High performance speaker

The equalization circuitry includes five band-pass amplifiers that adjust the frequency response to the acoustics of the chassis. The equalizer output is applied to a low-distortion amplifier that provides up to 5 watts of audio into an 8-ohm load. The power amplifier drives a high performance speaker (Figure 5-12) featuring a large magnet and long-throw cone to provide rich, full audio. The speaker is mounted with vibration isolators to reduce the chance of vibration-induced rattling interfering with audio playback.

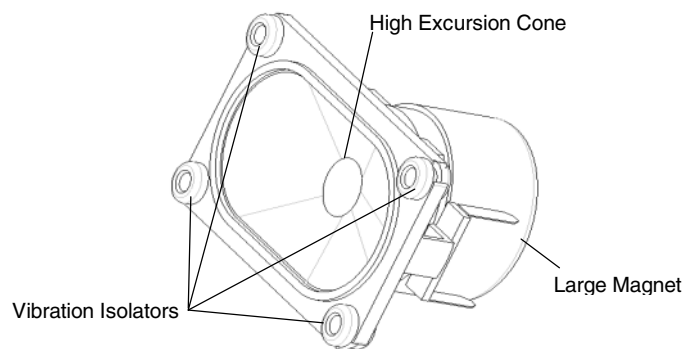


Figure 5-12. Compaq Premier Sound Speaker

5.8.6 AUDIO PROGRAMMING

Audio subsystem programming consists configuration, typically accomplished during POST, and control, which occurs during runtime. The register maps are described in the following subsections.

5.8.6.1 Audio Configuration

The audio subsystem is configured according to PCI protocol through the AC'97 audio controller function of the 82801 ICH. Table 5-21 lists the PCI configuration registers of the audio subsystem.

Table 5-21.
AC'97 Audio Controller
PCI Configuration Registers (82801 Device 31/Function 5)

PCI Conf. Addr.	Register	Value on Reset	PCI Conf. Addr.	Register	Value on Reset
00-01h	Vendor ID	8086h	14-17h	Native Audio Bus Mstr. Addr.	1h
02-03h	Device ID	2415h	18-1Bh	Reserved	1h
04-05h	PCI Command	0000h	1C-2Bh	Reserved	1h
06-07h	PCI Status	0280h	2C-2Dh	Subsystem Vendor ID	0000h
08h	Revision ID	xxh	2E-2Fh	Subsystem ID	0000h
09h	Programming	01h	30-3Bh	Reserved	0's
0Ah	Sub-Class	01h	3Ch	Interrupt Line	00h
0Bh	Base Class Code	04h	3Dh	Interrupt Pin	03h
0Eh	Header Type	00h	3E-FFh	Reserved	0's
10-13h	Native Audio Mixer Base Addr.	1h	--	--	--

NOTE:

Assume unmarked gaps are reserved and/or not used.

5.8.6.2 Audio Control

The audio subsystem is controlled through a set of indexed registers that physically reside in the audio codec. The register addresses are decoded by the audio controller and forwarded to the audio codec over the AC97 Link Bus previously described. The audio codec's control registers (Table 5-22) are mapped into 64 kilobytes of variable I/O space, the exact location determined by configuration software during POST.

Table 5-22.
AC'97 Audio Codec Control Registers

Offset Addr. / Register	Value On Reset	Offset Addr. / Register	Value On Reset	Offset Addr. / Register	Value On Reset
00h Reset	0100h	14h Video Vol.	8808h	28h Ext. Audio ID.	0001h
02h Master Vol.	8000h	16h Aux Vol.	8808h	2Ah Ext. Audio Ctrl/Sts	0000h
04h Reserved	X	18h PCM Out Vol.	8808h	2Ch PCM DAC SRate	BB80h
06h Mono Mstr. Vol.	8000h	1Ah Record Sel.	0000h	32h PCM ADC SRate	BB80h
08h Reserved	X	1Ch Record Gain	8000h	34h Reserved	X
0Ah PC Beep Vol.	8000h	1Eh Reserved	X	72h Reserved	X
0Ch Phone In Vol.	8008h	20h Gen. Purpose	0000h	74h Serial Config.	7x0xh
0Eh Mic Vol.	8008h	22h 3D Control	0000h	76h Misc. Control Bits	0404h
10h Line In Vol.	8808h	24h Reserved	X	7Ch Vendor ID1	4144h
12h CD Vol.	8808h	26h Pwr Mgmt.	000xh	7Eh Vendor ID2	5340h

NOTE:

Assume unmarked gaps are reserved and/or not used.

5.8.7 AUDIO SPECIFICATIONS

The specifications of the audio subsystem are listed in Table 5-23.

Table 5-23. Audio Subsystem Specifications	
Parameter	Measurement
Sampling Rate	5.51 KHz to 44 KHz
Resolution	16 bit
Nominal Input Voltage:	
Mic In (w/+20 db gain)	.283 Vp-p
Line In	2.83 Vp-p
Impedance:	
Mic In	1 K ohms (nom)
Line In	10 K ohms (min)
Line Out	800 ohms
Signal-to-Noise Ratio (input to Line Out)	90 db (nom)
Max. Power Output:	
Into 16-ohm load	3 watts
Into 8-ohm load (shipped configuration)	5.2 watts
Total Harmonic Distortion (THD) (to int. spkr):	
@ 0.5 watts	1 %
@ max. power output	10 %
Headphone Output Power (into 32 ohms)	60 mW
Input Gain Attenuation Range	46.5 db
Master Volume Range	-94.5 db
Frequency Response:	
Codec	20-20 KHz
Speaker	450 - 4000 Hz

5.9 NETWORK SUPPORT

All Compaq Deskpro systems covered in this guide include specific features to support communications over a network. In addition, some models, including those of the Deskpro EN Small Form Factor Series, include a network interface controller (NIC) as standard.

5.9.1 PCI VER.2.2 SUPPORT

These systems support the PME- (power management event) signal and provide 3.3 VDC auxiliary power on all PCI slots. Network interface cards compliant with PCI ver. 2.2 may be installed to provide “system off” network support without additional cable connections. In a powered down state the compliant network card receives 3.3 volts of auxiliary DC power on pin A14 of the PCI connector and uses PCI pin A19 for the PME- signal that is routed to general purpose input # 13 of the LPC47B34x I/O controller. Network activity causing the NIC card to assert the PME- signal can be used to restart or “wake” the system from a suspend state.

NOTE: For auxiliary power to be available in a system-off condition the unit must be plugged into an active AC outlet. Controlling unit power through an AC outlet strip will, with the strip turned off, disable PME functionality.

5.9.2 WAKE-ON-LAN SUPPORT

These systems provide Wake-On-LAN (WOL) support, which allows a compatible network interface card to be powered up and respond to special packets while the system is in a low-power (suspend) state. The compatible network interface card receives 5 VDC auxiliary power through a cable connection with the WOL header connector. The WOL connection also carries the WOL signal generated from the NIC card to general purpose input #14 of the LPC47B34x I/O controller. When relevant packets are received, the NIC card asserts the WOL signal, which is used to initiate the power-up (“wake up”) sequence.

NOTE: For auxiliary power to be available in a system-off condition the unit must be plugged into an active AC outlet. **A system plugged into an AC outlet strip that is turned off will disable WOL functionality.** Some NIC cards may require the WOL cable connection for power even if WOL functionality is not used.

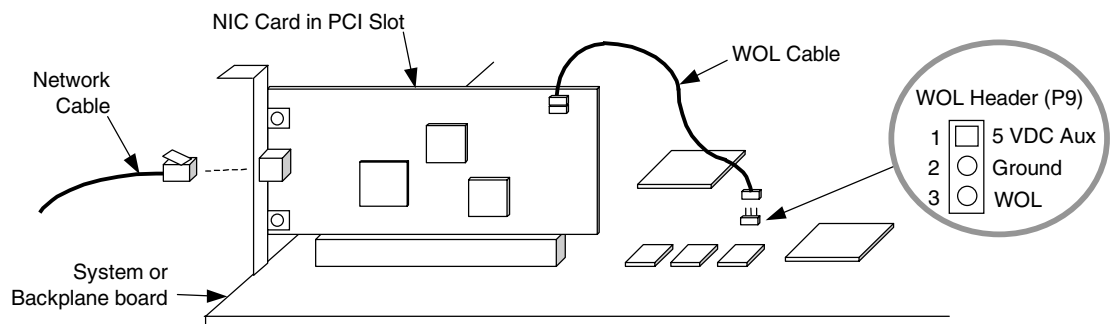


Figure 5-13. WOL Interface Connection (Generic Representation)

5.9.3 NETWORK ALERT FUNCTIONS

These systems provide the capability of alerting a network management console of specific events occurring to the system unit even while the unit is in suspend or powered off. Two types of alert support are provided:

- ◆ Alert-On-LAN (as supported by some Intel products).
- ◆ Remote System Alert (as supported by some 3Com products).

NOTE: For auxiliary power to be available in a system-off condition the unit must be plugged into an active AC outlet. **Controlling unit power through an AC outlet strip will, with the strip turned off, disable network alert functionality.**

5.9.3.1 Alert-On-LAN Support

Alert-On-LAN (AOL) support allows a compatible network interface controller/card to communicate the occurrence of certain system events over a network even while the system is powered off. In a system-off condition, auxiliary 3.3-volt power from the power supply assembly is applied to on-board components such as the LPC 47B34x I/O controller and the 82801 ICH that provide AOL support. The 3.3-volt auxiliary power is also available on the PCI bus for an AOL-compliant NIC card in a PCI slot.

As shown in the following figure, AOL implementation is built into Deskpro EN SFF models, which come standard with an Intel 82559 NIC. Support with AOL-compliant NIC PCI cards (such as the Intel PRO/100+ Management Adapter Solution) requires no auxiliary cables since the communication of events is handled through the PCI bus interface.

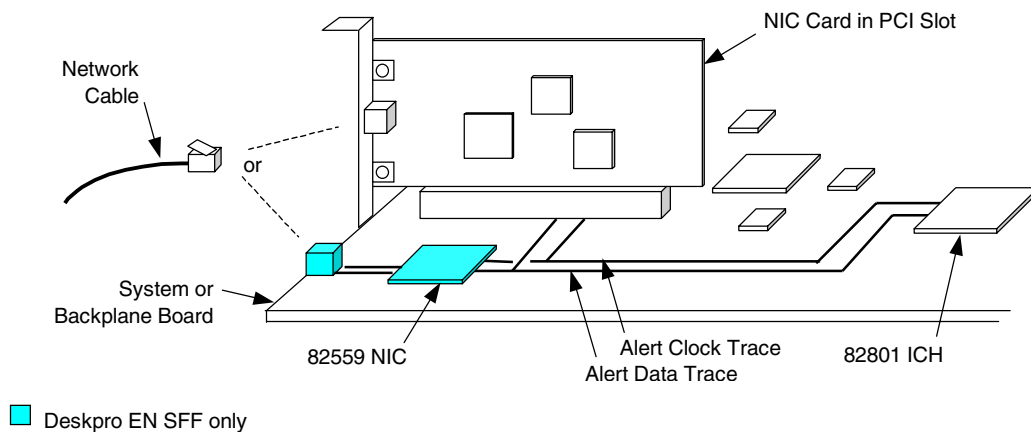
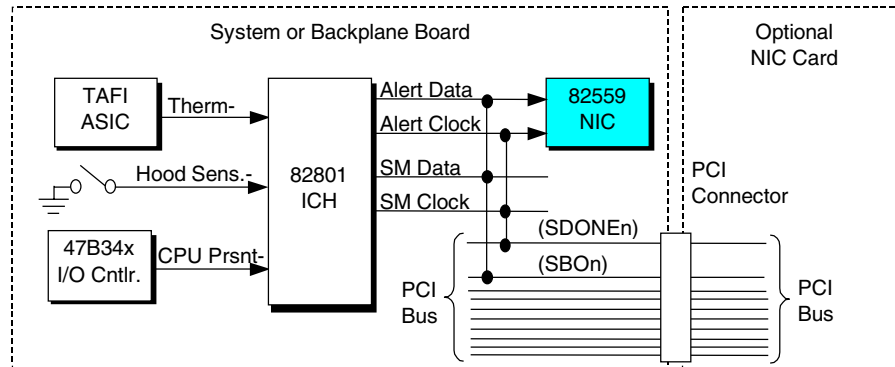


Figure 5-14. AOL Implementation (Generic Representation)

The 82801 ICH initiates event notification by transmitting an alert message over the SMBus-type Alert Clock/Alert Data interface to the network interface controller. On these systems the Alert Clock/Alert Data signals are wired-Or'd with the SMBus signals and use the SDONEn/SBOn signals lines for routing to a NIC card on the PCI bus (Figure 5-15).

The ICH's alert message will be the result of a signal from a sensor (thermal, intrusion, or CPU state) or from the ICH's detection of the system's running status. Upon receiving the alert message from the ICH the NIC transmits the appropriate, pre-constructed message over the network.



■ Deskpro EN SFF only

Figure 5-15. AOL Logic, Block Diagram

Reportable AOL events are listed in the following table:

Table 5-24.
AOL Events

Event	Description
BIOS Failure	System fails to boot successfully.
OS Problem	System fails to load operating system after POST.
Missing/Faulty Processor	Processor fails to fetch first instruction.
Thermal Condition	TAFI ASIC reports high temperature.
Chassis Intrusion [1]	Smart Cover Sensor detected cover removal. This event is battery backed, meaning that should the unit be unplugged (from AC power) during cover removal, notification will occur after AC power is restored.
Heartbeat	Indication of system's network presence (sent approximately every 30 seconds in normal operation).

NOTE:

[1] Not supported on Deskpro EP or Workstation AP250 models.

The AOL implementation requirements are as follows:

1. Intel PRP/100+ Management Adapter driver 3.1x or later (available from Compaq).
2. Client-side utility agent software (available from Compaq).
3. Management console running one of the following:
 - a. HP OpenView Network Node Manager 6.x
 - b. Intel LANDesk Client Manager
 - c. Compaq Insight Manager

5.9.3.2 Remote System Alert Support

These systems provide Remote System Alert (RSA) support for such NIC cards as the 3Com 3C905C-TX NIC card. The RSA function is similar to AOL in that the unit provides, even while powered off, system status alert messages to a network console. However, NIC cards implementing the RSA method do not use the SMBus for receiving alert information and therefore require, in addition to the PCI connection, an auxiliary cable connection with the system (Figure 5-16).

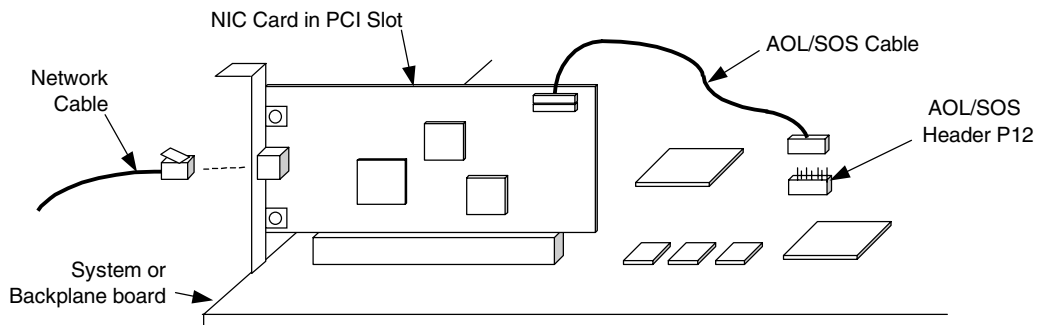
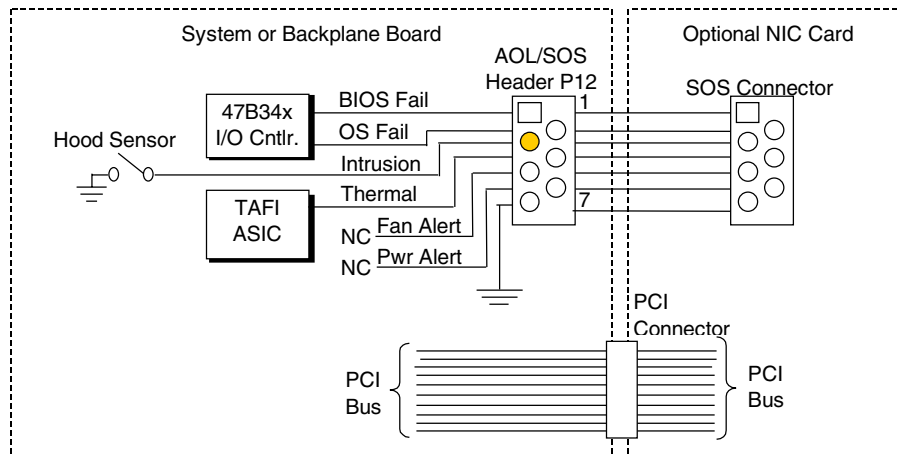


Figure 5-16. Remote Sense Alert Implementation (Generic Representation)

In the Remote Sense Alert implementation, the NIC card receives event notification directly from the system's thermal and hood sensors and the LPC47B34x I/O controller over an AOL/SOS cable connection (Figure 5-17). During system-off conditions the NIC card receives auxiliary power from the 3.3 VDC auxiliary power rail on the PCI bus.



● Not connected on Deskpro EP or Workstation AP250 models.

Figure 5-17. RSA Logic, Block Diagram

Reportable RSA events are listed in the following table:

Table 5-25. Remote System Alert Events	
Event	Description
BIOS Failure	System fails to boot successfully.
Thermal Condition	TAFI ASIC reports high temperature. Some systems may generate an alert message when increasing fan speed.
Chassis Intrusion [1]	Smart Cover Sensor detected cover removal. This event is battery backed, meaning that should the unit be unplugged (from AC power) during cover removal, notification will occur after AC power is restored.
Heartbeat	Indication of system's network presence (sent approximately every 30 seconds in normal operation).

NOTE:

[1] Not supported on Deskpro EP or Workstation AP250 models.

The current Remote System Alert implementation requirements are as follows:

1. 3Com Etherlink 3C905C-TX NIC.
2. 7-pin AOL/SOS cable.
3. 3Com EtherDisk Driver 5.x or later (available from Compaq).
4. Client-side utility software (included with driver).
5. Server-side utility software (available from Compaq).
6. Management console running one of the following:
 - a. HP OpenView Network Node Manager 6.x
 - b. Intel LANDesk Client Manager

5.9.4 NETWORK INTERFACE CONTROLLER

Compaq Deskpro EN Small Form Factor models include a network interface controller (NIC) embedded on the system board. The NIC (Figure 5-13) includes the 82559 controller, two LED indicators, and support firmware. The support firmware is contained in the system (BIOS) ROM. The NIC can operate in half- or full-duplex modes, and provides auto-negotiation of both mode and speed. Half-duplex operation features an Intel-proprietary collision reduction mechanism while full-duplex operation follows the IEEE 802.3x flow control specification. Transmit and receive FIFOs of 3 kilobytes each reduce the chance of overrun while waiting for bus access.

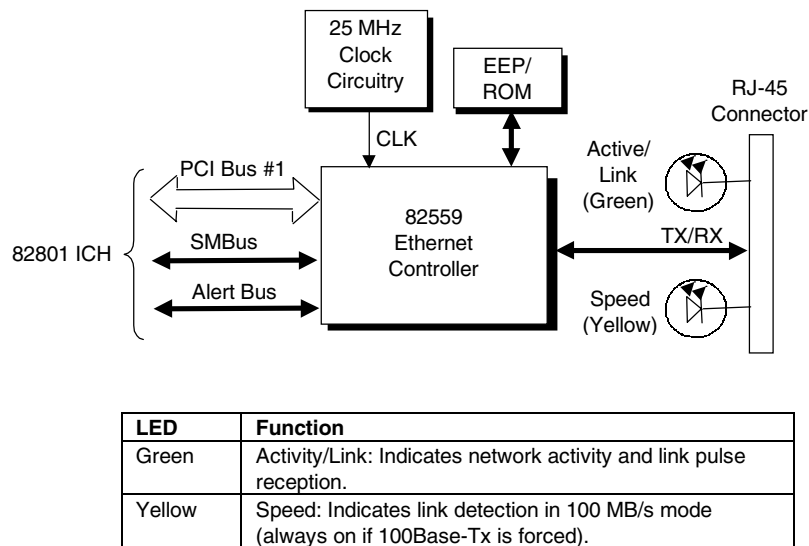


Figure 5-18. 10/100 TX Network Interface Controller Block Diagram

The Intel 82559 Fast Ethernet Controller includes the following features:

- ◆ Intel 82559 Fast Ethernet controller with 32-bit architecture and 3-KB TX/RX buffers.
- ◆ Dual-mode support with auto-switching between 10BASE-T and 100BASE-TX.
- ◆ Power down and Wake up support in both APM and ACPI environments (PME- and WOL).
- ◆ Alert-on-LAN (AOL v1.0) support.
- ◆ Dual control (PCI and SM bus interfaces).
- ◆ Link and Activity LED indicator drivers

The 82559 controller features high and low priority queues and provides priority-packet processing for networks that can support that feature. The controller's micro-machine processes transmit and receive frames independently and concurrently. Receive runt (under-sized) frames are not passed on as faulty data but discarded by the controller, which also directly handles such errors as collision detection or data under-run. An EEPROM, accessed by the 82559 controller over a serial interface, is used to store identification, configuration and connection parameters.

The NIC uses 3.3 VDC auxiliary power, which allows the 82559 controller to support Wake-On-LAN (WOL) and Alert-On-LAN (AOL) functions while the main system is powered down.

5.9.4.1 Power Management Support

The 82559 controller features Wired-for-Management (WfM) support providing system wake up from network events (WOL) as well as generating system status messages (AOL) and supports both APM and ACPI power management environments. The controller receives 3.3 VDC (auxiliary) power as long as the system is plugged into a live AC receptacle, allowing support of wake-up events occurring over a network while the system is powered down or in a low-power state.

APM Environment

The Advanced Power Management (APM) functionality of system wake up is implemented through the system's APM-compliant BIOS and the controller's Magic Packet-compliant hardware. This environment bypasses operating system (OS) intervention allowing a plugged in unit to be turned on remotely over the network (i.e., "remote wake up"). In APM mode the controller, will respond upon receiving a Magic Packet, which is a packet where the node's address is repeated 16 times. Upon Magic packet detection, the controller asserts the PME signal where power control logic turns on the system and initiates the boot sequence. After the boot sequence the BIOS clears the PME- signal so that subsequent wakeup events will be detected.

ACPI Environment

The Advanced Configuration and Power Interface (ACPI) functionality of system wake up is implemented through an ACPI-compliant OS such as Windows NT 5.0 and is the default power management mode. The following wakeup events may be individually enabled/disabled through the supplied software driver:

- ◆ Magic Packet – Packet with node address repeated 16 times in data portion

NOTE: The following functions are supported in NDIS5 drivers but implemented through remote management software applications (such as LanDesk).

- ◆ Individual address match – Packet with matching user-defined byte mask
- ◆ Multicast address match – Packet with matching user-defined sample frame
- ◆ ARP (address resolution protocol) packet
- ◆ Flexible packet filtering – Packets that match defined CRC signature

When an enabled event is received the controller asserts the PME- signal that is used to initiate the wakeup sequence.

5.9.4.2 NIC Programming

Programming the 82559 NIC controller consists of configuration, which occurs during POST, and control, which occurs at runtime.

Configuration

The 82559 controller is a PCI device and configured through PCI configuration space registers using PCI protocol described in chapter 4. The PCI configuration registers are listed in the following table:

Table 5-26.
NIC Controller PCI Configuration Registers (82559 Device 2/Function 0)

PCI Conf. Addr.	Register	Value on Reset	PCI Conf. Addr.	Register	Value on Reset
00-01h	Vender ID	8086h	10-13h	Cntrl. Reg. Base Addr. (Mem)	0000h
02-03h	Device ID	1229h	14-17h	Cntrl. Reg. Base Addr. (I/O)	00h
04-05h	PCI Command	0000h	18-1Bh	Flash Mem. Base Addr.	00h
06-07h	PCI Status	0280h	2C-2Dh	Subsystem Vender ID	
08h	Revision ID	xxh	2E-2Fh	Subsystem ID	
09-0Bh	Class Code	01h	30-33h	Expansion ROM Base Addr.	
0Ch	Cache Line Size	01h	34h	Cap-Ptr	
0Dh	Latency Timer	04h	3C-3D	Interrupt Line/Pin	
0Eh	Header Type	00h	3E-3Fh	Min Gnt/Max Lat	
0Fh	BIST	00h	DC-E3h	Power Mgmt. Functions	

NOTE:

Assume unmarked gaps are reserved and/or not used.

Control

The 82559 controller is controlled through registers that may be mapped in system memory space or variable I/O space. The registers are listed in the following table:

Table 5-27.
NIC Control Registers

Offset Addr. / Register	No. of Bytes	Offset Addr. / Register	No. of Bytes
00h SCB Status	2	19h Flow Control Register	2
02h SCB Command	2	1Bh PMDR	1
04h SCB General Pointer	4	1Ch General Control	1
08h PORT	4	1Dh General Status	1
0Ch Flash Control Reg.	2	1E-2Fh Reserved	10
0Eh EEPROM Control Reg.	2	30h Function Event Register	4
10h Mgmt. Data I/F Cntrl. Reg.	4	34h Function Event Mask Register	4
14h Rx Direct Mem. Access Byte Cnt.	4	38h Function Present State Register	4
18h Early Receive Interrupt	1	20h Force Event Register	4

Not implemented in these systems (CardBus registers).

5.9.4.3 RJ-45 Connector

Figure 5-19 shows the RJ-45 connector used for the NIC interface. This connector includes the two status LEDs as part of the connector assembly.

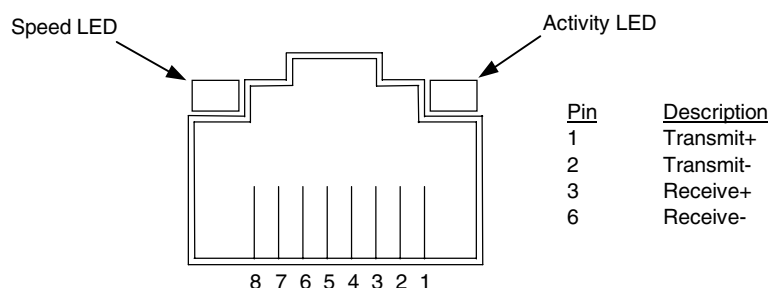


Figure 5-19. Ethernet TPE Connector (RJ-45, viewed from card edge)

5.9.4.4 82559 NIC Specifications

Table 5-28.
82559 NIC Specifications

Parameter	
Modes Supported	10BASE-T half duplex @ 10 MB/s 10Base-T full duplex @ 20 MB/s 100BASE-TX half duplex @ 100 MB/s 100Base-TX full duplex @ 200 MB/s
Standards Compliance	IEEE VLAN (802.1A) IEEE 802.2 IEEE 802.3 & 802.3u IEEE Intel priority packet (801.1p)
OS Driver Support	MS Windows 95,98, and 2000 beta MS Windows NT 3.51 & 4.0 Novell Netware 3.11, 3.12, & 4.1x; 5 Server Sunsoft Solaris SCO UnixWare Open Desktop OpenServer
Boot ROM Support	Intel PRO/100 Boot Agent (PXE 2.0, RPL)
F12 BIOS Support	Yes
Bus Interface	PCI 2.2
Power Management Support	APM, ACPI, PCI Power Management Spec.

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Chapter 6

EMBEDDED GRAPHICS SUBSYSTEMS

6.1 INTRODUCTION

This chapter describes graphics subsystems that are embedded on the system board. All 810- and 810e-based systems feature the Intel 82810/DC-100 and 82810e/DC-100 GMCH components (respectively) that integrates an Intel i740 graphics controller. The 820-based Deskpro EN SFF system features a Matrox G400 graphics controller that is also embedded on the system board. Both graphics subsystems employ the AGP interface allowing the use of system memory as well as local RAM to provide efficient, economical 2D and 3D performance.

This chapter covers the following subjects:

- ◆ 810-/810e-based graphics subsystem (6.2) page 6-2
- ◆ Matrox G400-based graphics subsystem (6.3) page 6-4

6.2 810-/810e-BASED GRAPHICS SUBSYSTEM

The Intel 810 and 810e chipsets both integrated the equivalent of an Intel i740 graphics controller into their GMCH components (Figure 6-1).

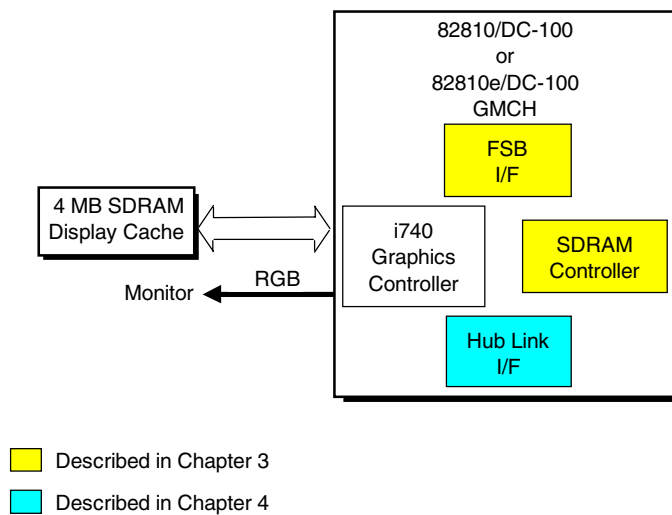


Figure 6-1. GMCH Block diagram

6.2.1 FUNCTIONAL DESCRIPTION

The Intel graphics controller (Figure 6-2) integrated into the GMCH component includes 2D and 3D accelerator engines working with a deeply-pipelined pre-processor. The controller supports perspective-correct texture mapping, bilinear and anisotropic Mip-mapping, Alpha blending, Gouraud shading, and fogging.

The controller uses the AGP 2X interface and supports Type 1, Type 2, and Type 3 sideband cycles for a peak transfer rate of 533 MB/s. The AGP interface also allows the Intel graphics controller to use a portion of system memory for instructions, textures, and frame (display) buffering. Either a 32- or 64-MB block of system memory may be configured for use by the graphics controller for graphics use. Another 512-KB block (fixed) is used for memory-mapped control and status registers.

The controller also uses four megabytes of SDRAM (soldered down) as a display cache especially suited for 3D operation. The external Display Cache allows the graphics controller to simultaneously render graphics to the Z-buffer (in the display cache) while processing textures in a portion of system memory. The 4-MB SDRAM Display Cache is accessed through a 32-bit 100-MHz interface.

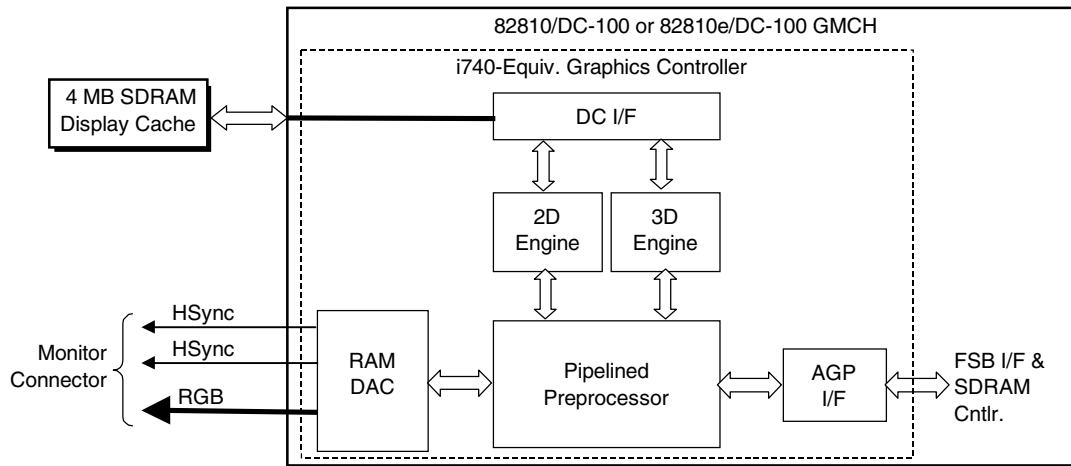


Figure 6-2. 810-/810e-Based Graphics Subsystem

The Intel graphics controller includes special enhancements for 2D operations. Motion compensation logic is included to improve performance during software decoding of MPEG2 video. Hardware cursor and overlay engines relieve software processing and provide independent gamma correction, saturation, and brightness control.

The 230-MHz RAMDAC can support a variable-scan rate monitor up to a maximum resolution of 1600 x 1200 with 256 colors. Video BIOS for the controller is held in the system BIOS ROM and copied into systems memory at runtime for maximum performance.

6.2.1.1 Feature Summary

- ◆ Accelerated driver support for Windows 3.1/95/98/2000, Windows NT 4.0, OS/2
- ◆ MS ActiveMovie and Media Player support for Win95
- ◆ Direct 3D support
- ◆ MS Direct Draw 5/6 support
- ◆ AGP 2X interface
- ◆ DDC2B compliant
- ◆ Accelerator engine support for:
 - 3-ROP BitBLT
 - Line Draw
 - Color expansion
 - Video color conversion/scaling
 - Motion video
 - Triangle setup

6.2.2 DISPLAY MODES

The Intel graphics controller supports the following 2D display modes:

Table 6-1.
Intel 2D Graphics Display Modes

Resolution	Bits per pixel	Color Depth	Refresh Rate
640 x 480	8	256	60, 70, 72, 75, 85
640 x 480	16	65K	60, 70, 72, 75, 85
640 x 480	24	16.7M	60, 70, 72, 75, 85
720 x 480	8	256	75, 85
720 x 480	16	65K	75, 85
720 x 480	24	16.7M	75, 85
720 x 576	8	256	60, 75, 85
720 x 576	16	65K	60, 75, 85
720 x 576	24	16.7M	60, 75, 85
800 x 600	8	256	60, 70, 72, 75, 85
800 x 600	16	65K	60, 70, 72, 75, 85
800 x 600	24	16.7M	60, 70, 72, 75, 85
1024 x 768	8	256	60, 70, 72, 75, 85
1024 x 768	16	65K	60, 70, 72, 75, 85
1024 x 768	24	16.7M	60, 70, 72, 75, 85
1152 x 864	8	256	60, 70, 72, 75, 85
1152 x 864	16	65K	60, 70, 72, 75, 85
1152 x 864	24	16.7M	60, 70, 72, 75, 85
1280 x 720	8	256	60, 75, 85
1280 x 720	16	65K	60, 75, 85
1280 x 720	24	16.7M	60, 75, 85
1280 x 960	8	256	60, 75, 85
1280 x 960	16	65K	60, 75, 85
1280 x 960	24	16.7M	60, 75, 85
1280 x 1024	8	256	60, 70, 72, 75, 85
1280 x 1024	16	65K	60, 70, 72, 75, 85
1280 x 1024	24	16.7M	60, 70, 75, 85
1600 x 900	8	256	60, 75, 85
1600 x 900	16	65K	60, 75, 85
1600 x 1200	8	256	60, 70, 72, 75, 85

6.2.3 UPGRADING

Upgrading the graphics controller on an 810- or 810e-based system is accomplished with the following procedure:

1. Power down the system.
2. Remove the chassis cover (hood).
3. Install a PCI-type graphics controller in an available slot.
4. Close cover.
5. Power up the system. The BIOS should detect the presence of the installed graphics card and disable the graphics controller integrated into the 82810/DC-100 or 82810e/DC-100 GMCH.

6.3 MATROX G400-BASED GRAPHICS SUBSYSTEM

The Matrox G400 AGP graphics controller is featured as the system board-resident graphics controller on Compaq Deskpro EN SFF systems that feature the Intel 820 chipset. The Matrox G400 graphics controller provides high-performance 2D/3D display processing with AGP 4X support and supplemented with 16 megabytes of SDRAM for the frame buffer (Figure 6-3).

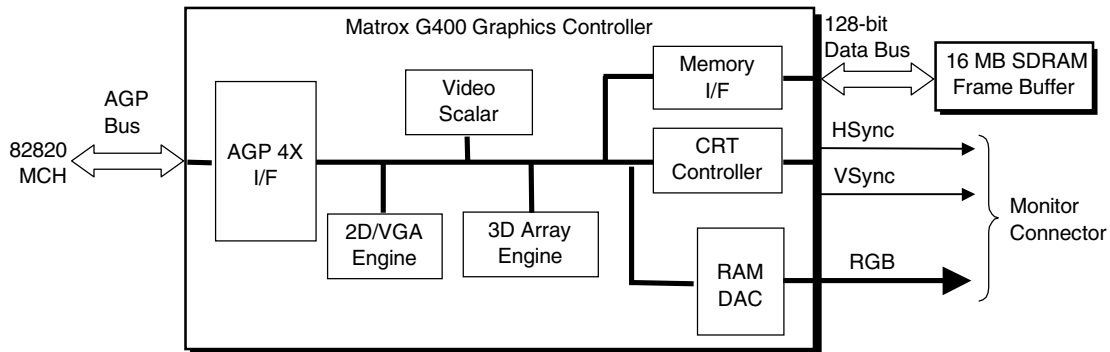


Figure 6-3. Matrox G400-Based Graphics Subsystem

The Matrox G400 supports AGP 4X protocol, providing a peak transfer rate of 1GB/s. The controller achieves high 3D performance with special rendering techniques such as single-cycle multi-texturing and parallel triangle processing. The controller utilizes a portion of system memory for texturing, instructions, and control while employing 16 megabytes of SDRAM for the frame (display) buffer. Video BIOS is included in the system BIOS ROM and copied into system memory at runtime.

Key features of the Matrox G400-based subsystem include:

- ◆ 300-MHz DAC
- ◆ 256-bit DualBus architecture
- ◆ QuickDraw, DirectX 6, PC98/99, Broadcast PC, DirectShow, OpenGL compatible
- ◆ 2D accelerator with:
 - Programmable, transparent BitBLT
 - Full acceleration MS DirectDraw support
 - High speed 32-bit VGA core
- ◆ 3D accelerator with:
 - Ultra-pipelined floating point engine
 - Optimized for Direct 3D and OpenGL triangles, strips, fans, and vectors
 - Native support for vertex format
 - Hardware dithering including LUT textures
- ◆ Video support features including:
 - Color conversion and scaling
 - DVD subpicture with alpha blending and BOB and Weave support
- ◆ VESA DDC1 and DDC2B support

6.3.1 DISPLAY MODES

The graphics modes supported by the Matrox G400 controller are listed in Tables 6-2.

Table 6-2.
Matrox G400 Graphics Display Modes

Resolution	Bits per pixel	Color Depth	Max. Refresh Frequency (Hz)
640 x 480	8	256	85
640 x 480	16	65K	85
640 x 480	24	16.7M	85
800 x 600	8	256	85
800 x 600	16	65K	85
800 x 600	24	16.7M	85
1024 x 768	8	256	85
1024 x 768	16	65K	85
1024 x 768	24	16.7M	85
1152 x 864	8	256	85
1152 x 864	16	65K	85
1152 x 864	24	16.7M	85
1280 x 1024	8	256	85
1280 x 1024	16	65K	85
1280 x 1024	24	16.7M	85
1600 x 1200	8	256	85
1600 x 1200	16	65K	85
1600 x 1200	24	16.7M	85
1800 x 1440	8	256	85
1800 x 1440	16	65K	85
1800 x 1440	24	16.7M	85
1920 x 1080	8	256	85
1920 x 1080	16	65K	85
1920 x 1080	24	16.7M	85
1920 x 1440	8	256	75
1920 x 1440	16	65K	75
1920 x 1440	24	16.7	75
2048 x 1536	8	256	65
2048 x 1536	16	65K	65
2048 x 1536	24	16.7M	65

6.3.2 UPGRADING

Upgrading the system board-resident graphics controller is accomplished with the following procedure:

6. Power down the system.
7. Remove the chassis cover (hood).
8. Install a PCI-type graphics controller in an available slot.
9. Close cover.
10. Power up the system. The BIOS should detect the presence of the installed graphics card and disable the embedded Matrox G400 graphics controller.

6.4 PROGRAMMING

6.4.1 CONFIGURATION

The graphics subsystem works off the AGP bus and is configured through PCI configuration space registers using PCI protocol. These registers (Table 6-3) are configured by BIOS during POST.

Table 6-3.
PCI Configuration Space Registers

PCI Config. Address	Function	PCI Config. Address	Function
00h	Vender ID/Device ID	14h	Relocateable I/O Base Address
04h	PCI Command	30h	Expansion ROM Base Address
08h	Status	3Ch	Interrupt Line / Interrupt Pin
10h	Display Memory Base Address	--	--

For a discussion of accessing PCI configuration space registers refer to chapter 4. For a detailed description of registers refer to applicable ATI Technologies, Inc. documentation.

6.4.2 CONTROL

6.4.2.1 Standard VGA Modes

Table 6-4 list the control registers used for operating in standard VGA mode. No special drivers are required for VGA, EGA, and CGA modes. For a detailed description of the registers refer to applicable ATI Technologies, Inc. documentation.

Table 6-4.
Standard VGA Mode I/O Mapping

I/O Address	Function	I/O Address	Function
3B5.00..26h*	CRT Controller (mono)	3C6h..3C9h	RAMDAC
3BAh	VSYNC Control, Display Status	3CAh	Read VSYNC Status
3C1.00..14h*	Attribute Controller	3CCh	Misc. Control, Read
3C2h	Misc. Control / Status	3CF.00..08h	Graphics Controller
3C5h.00..04h*	Sequencer	3D5.00..26h*	CRT Controller (color)
--	--	3DAh	VSYNC Control, Display Status (color)

* Index at base minus 1 (i.e., if base is 3B5h, index is at 3B4h).

6.4.2.2 Extended VGA Modes

Extended modes use the video BIOS (contained in the system flash ROM) and the supplied driver.

6.5 MONITOR POWER MANAGEMENT CONTROL

This controller provides monitor power control for monitors that conform to the VESA display power management signaling (DPMS) protocol. This protocol defines different power consumption conditions and uses the HSYNC and VSYNC signals to select a monitor's power condition. Table 6-5 lists the monitor power conditions.

Table 6-5.
Monitor Power Management Conditions

HSYNC	VSYNC	Power Mode	Description
Active	Active	On	Monitor is completely powered up. If activated, the inactivity counter counts down during system inactivity and if allowed to timeout, generates an SMI to initiate the Suspend mode.
Active	Inactive	Suspend	Monitor's high voltage section is turned off and CRT heater (filament) voltage is reduced from 6.6 to 4.4 VDC. The Off mode inactivity timer counts down from the preset value and if allowed to timeout, another SMI is generated and serviced, resulting in the monitor being placed into the Off mode. Wake up from Suspend mode is typically a few seconds.
Inactive	Inactive	Off	Monitor's high voltage section and heater circuitry is turned off. Wake up from Off mode is a little longer than from Suspend.

6.6 MONITOR CONNECTOR

The Deskpro EN SFF models provide a DB-15 connector on the rear chassis panel for connection to an analog monitor. The pinout for this connector is shown in Figure 6-3 and Table 6-6.

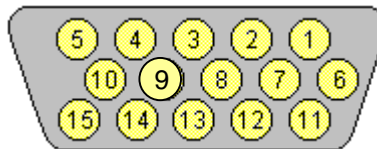


Figure 6-3. VGA Monitor Connector, (Female DB-15, as viewed from rear).

Table 6-6.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	PWR	+5 VDC (fused) [1]
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	NC	Not Connected
4	NC	Not Connected	12	SDA	DDC2-B Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSynC	Vertical Sync
7	G GND	Blue Analog Ground	15	SCL	DDC2-B Clock
8	B GND	Green Analog Ground	--	--	--

NOTES:

[1] Fuse automatically resets when excessive load is removed.

Chapter 7

POWER and SIGNAL DISTRIBUTION

7.1 INTRODUCTION

This chapter describes the power supply and method of general power and signal distribution. Topics covered in this chapter include:

- ◆ Power supply assembly/control (7.2) page 7-1
- ◆ Power distribution (7.3) page 7-5
- ◆ Signal distribution (7.4) page 7-7

7.2 POWER SUPPLY ASSEMBLY/CONTROL

This system features a power supply assembly that is controlled through programmable logic (Figure 7-1).

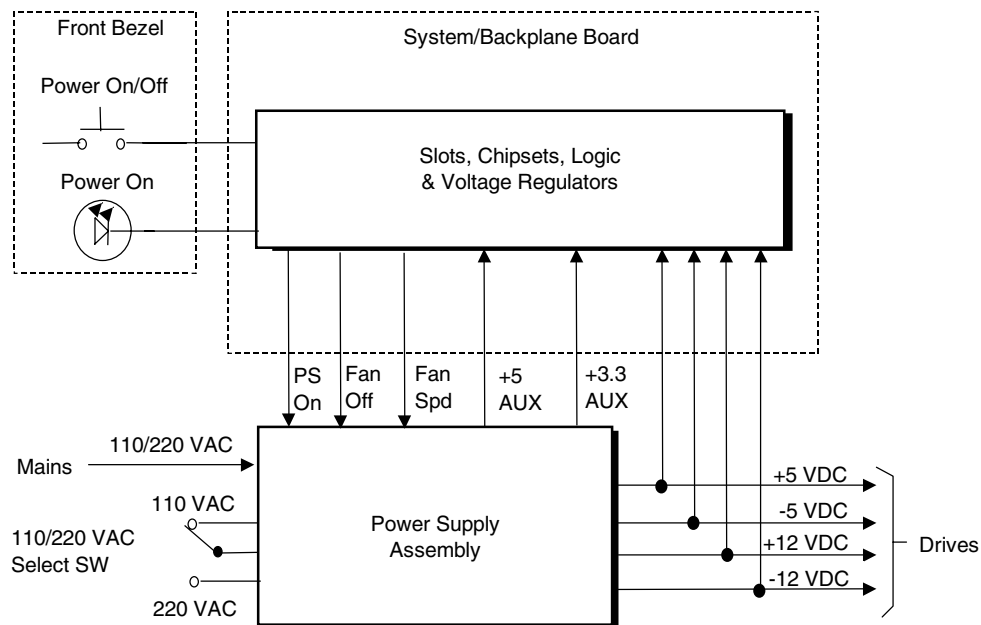


Figure 7-1. Power Distribution and Control, Block Diagram

7.2.1 POWER SUPPLY ASSEMBLY

The power supply assembly is contained in a single unit that features a selectable input voltage: 90-132 VAC and 180-264 VAC. Deskpro EN SFF systems use a 120-watt supply while all other systems employ a 200-watt supply. Tables 7-1 and 7-2 list the specifications of the power supplies.

Table 7-1.
120-Watt Power Supply Assembly Specifications (P/N 401003)

	Range/ Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
110 VAC Setting	90 - 132 VAC	--	--	--	--
220 VAC Setting	180-264 VAC	--	--	--	--
Line Frequency	47 - 63 Hz	--	--	--	--
Steady State Input (VAC) Current	--	--	4.0 A	--	--
+3.3 VDC Output	+/- 5%	0.20 A	11.0 A	11.0 A	50 mV
+5 VDC Output	+/- 5%	0.50 A	10.0 A	10.0 A	65 mV
+3 AUX Output	+/- 5%	0.20 A	1.00 A	1.00 A	50 mV
+5 AUX Output	+/- 4%	0.20 A	2.00 A	2.00 A	65 mV
+12 VDC Output	+/- 5%	0.00 A	2.00 A	3.50 A	120 mV
-12 VDC Output	+/- 10%	0.00 A	0.15 A	0.15 A	200 mV

NOTES:

[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.

[2] Surge duration no longer than 10 seconds and +12 tolerance +/- 10%.

Table 7-2.
200-Watt Power Supply Assembly Specifications (P/N 386461)

	Range/ Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
110 VAC Setting	90 - 132 VAC	--	--	--	--
220 VAC Setting	180-264 VAC	--	--	--	--
Line Frequency	47 - 63 Hz	--	--	--	--
Steady State Input (VAC) Current	--	--	6.00 A	--	--
+3.3 VDC Output	+/- 4%	1.40 A	18.0 A [3]	18.0 A	50 mV
+3.3 AUX	+/- 5%	0.00	2.00 A	2.00 A	50 mV
+5 VDC Output	+/- 5%	1.40 A	20.0 A [3]	20.0 A	50 mV
-5 VDC Output	+/- 10%	0.00 A	0.15 A	0.15 A	100 mV
+5 AUX Output	+/- 4%	0.00 A	1.70 A	1.70 A	50 mV
+12 VDC Output	+/- 5%	0.07 A	6.50 A	8.50 A	120 mV
-12 VDC Output	+/- 10%	0.00 A	0.15 A	0.15 A	200 mV

NOTES:

[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.

[2] Surge duration no longer than 10 seconds and +12 tolerance +/- 10%.

[3] Maximum combined power provided by +3.3 and +5 VDC outputs should not exceed 135 watts.

7.2.2 POWER CONTROL

The power supply assembly is controlled digitally by the PS On signal (Figure 7-1). When PS On is asserted, the Power Supply Assembly is activated and all voltage outputs are produced. When PS On is de-asserted, the Power Supply Assembly is off and all voltages (except +3.3 AUX and +5 AUX) are not generated. **Note that the +3.3 AUX and +5 AUX voltages are always produced as long as the system is connected to a live AC source.**

7.2.2.1 Power Button

The PS On signal is typically controlled through the Power Button which, when pressed and released, applies a negative (grounding) pulse to the power control logic. The resultant action of pressing the power button depends on the state and mode of the system at that time and is described as follows:

System State	Pressed Power Button Results In:
Off	Negative pulse, of which the falling edge results in power control logic asserting PS On signal to Power Supply Assembly, which then initializes. ACPI four-second counter is not active.
On, ACPI Disabled	Negative pulse, of which the falling edge causes power control logic to de-assert the PS On signal. ACPI four-second counter is not active.
On, ACPI Enabled	<p>Pressed and Released Under Four Seconds:</p> <p>Negative pulse, of which the falling edge causes power control logic to generate SMI-, set a bit in the SMI source register, set a bit for button status, and start four-second counter. Software should clear the button status bit within four seconds and the Suspend state is entered. If the status bit is not cleared by software in four seconds PS On is de-asserted and the power supply assembly shuts down (this operation is meant as a guard if the OS is hung).</p> <p>Pressed and Held At least Four Seconds Before Release:</p> <p>If the button is held in for at least four seconds and then released, PS On is negated, de-activating the power supply.</p>

7.2.2.2 Power LED Indications

Three LEDs are used to indicate system power status. The front panel (bezel) power LED provides a visual indication of three key system conditions listed as follows:

Power LED	Condition
Steady green	Normal full-on operation
Blinking green @ 0.5 Hz	Sleep (suspend) state (S4, S5)
Blinking green @ 1 Hz	Sleep (suspend) state (S1, S3)
Steady red	Backplane board or processor not seated
Blinks red @ 0.5 Hz	Power supply crowbar activated
Blinks red @ 1 Hz	BIOS ROM error
Blinks red @ 4 Hz	Thermal condition: processor has overheated and shut down

7.2.2.3 Wake Up Events

The PS On signal can be activated with a power “wake-up” of the system due to the occurrence of a magic packet, serial port ring, or PCI power management (PME) event. These events can be individually enabled through the Setup utility to wake up the system from a sleep (low power) state.

NOTE: Wake-up functionality requires that certain circuits receive auxiliary power while the system is turned off. The system unit must be plugged into a live AC outlet for wake up events to function. **Using an AC power strip to control system unit power will disable wake-up event functionality.**

The wake up sequence for each event occurs as follows:

Wake-On-LAN

A compliant network interface controller (NIC) can be configured for detection of a “Magic Packet” and wake the system up from sleep mode through the assertion of the PME- signal on the PCI bus.

An optional NIC card may also be installed and used for remote wake-up. A NIC card that provides a WOL signal connectable to WOL header P9 can activate the PS On signal. Note that the NIC card must be able to run off the five volts of power from header P9 during the system’s sleep state. Refer to Chapter 5, “Network Support” for more information.

Modem Ring

A ring condition on serial port A (COM1) or serial port B (COM2) can be detected by the power control logic and, if so configured, cause the PS On signal to be asserted.

Power Management Event

A power management event that asserts the PME- signal on the PCI bus can be enabled to cause the power control logic to generate the PS On. Note that the PCI card must be PCI ver. 2.2 compliant to support this function.

7.3 POWER DISTRIBUTION

7.3.1 3.3/5/12 VDC DISTRIBUTION

The power supply assembly includes a multi-connector cable assembly that routes +3.3 VDC, +5 VDC, -5 VDC, +12 VC, and -12 VDC to the system board as well as to the individual drive assemblies. Figure 7-2 shows the power supply cabling for the Deskpro EN SFF series.

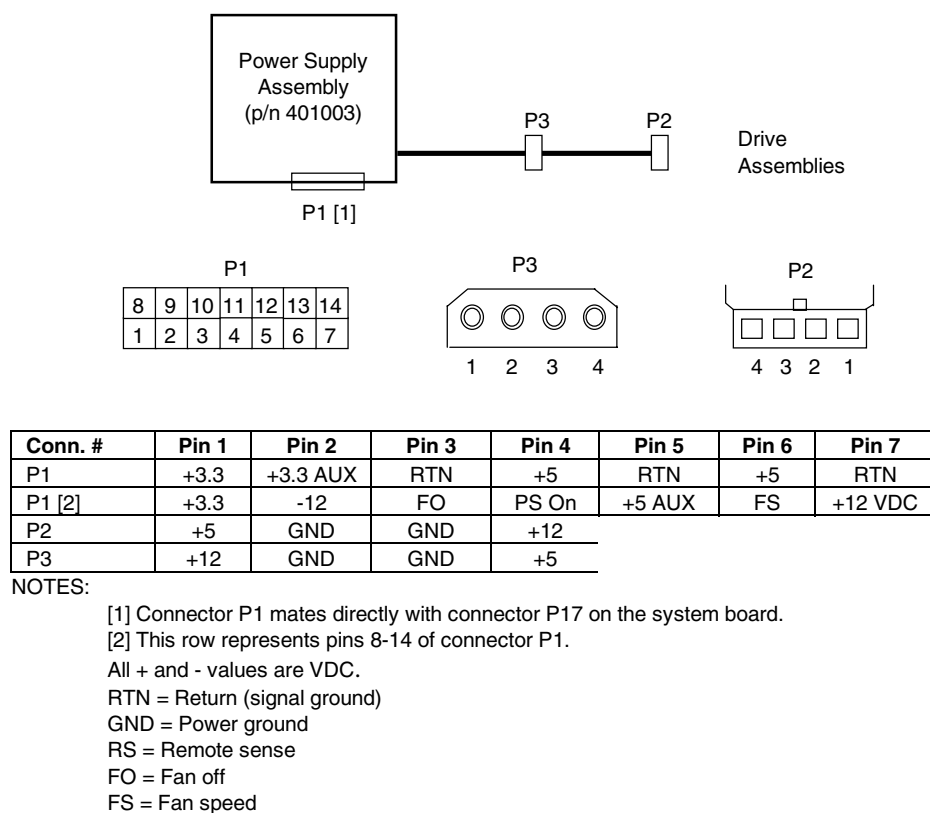
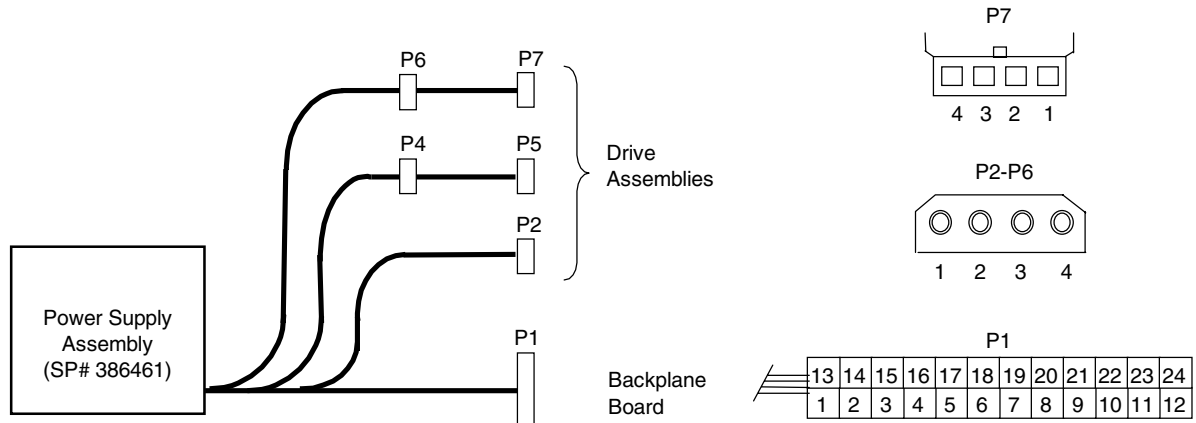


Figure 7-2. Deskpro EN SFF Power Cable Diagram

Figure 7-3 shows the power supply cabling for Deskpro EP, Workstation, and EN DT/MT series units.



Conn. #	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12
P1	+3.3	+3.3RS	RTN	+5	RTN	+5	AuxRtn	FO	+5 Aux	+12	+3.3Aux	FSpd
P1 [1]	+3.3	-12	Rtn	PS On	RTN	RSRTN	RTN	-5	+5	+5	+3.3RS	FS
P2	+5	GND	GND	+12								
P3	+12	GND	GND	+5								

NOTES:

[1] This row represents pins 13-24 of connector P1.

All + and - values are VDC.

RTN = Return (signal ground)

GND = Power ground

RS = Remote sense

FO = Fan off

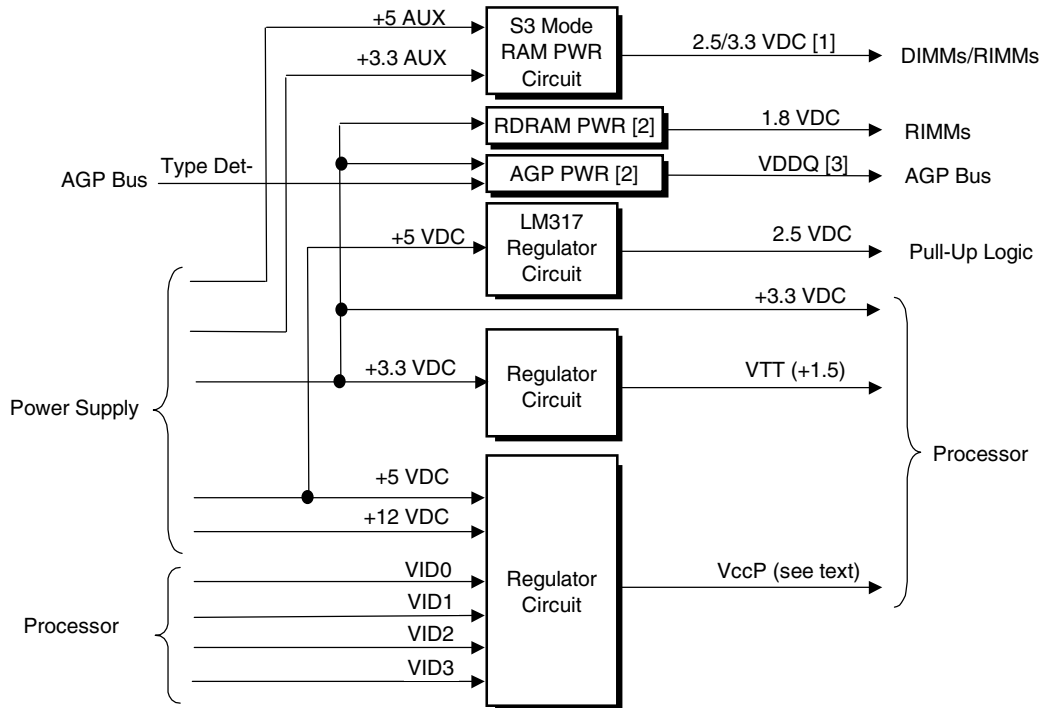
FSpd = Fan speed

FS = Fan Sink

Figure 7-3. Deskpro EP, EN DT/MT, or Workstation Power Cable Diagram

7.3.2 LOW VOLTAGE DISTRIBUTION

Voltages less than 3.3 VDC and processor core (VccP) voltage are produced through regulator circuitry on the system board.



NOTE:

[1] 2.5 VDC on 810/810e-based systems; 3.3 on 820-based systems.

[2] 820-based systems only.

[3] VDDQ = 1.5 for AGP 4X cards (Type Det- grounded), 3.3 for AGP 1X/2X cards (Type Det- left open)

Figure 7-4. Low Voltage Supply and Distribution Diagram

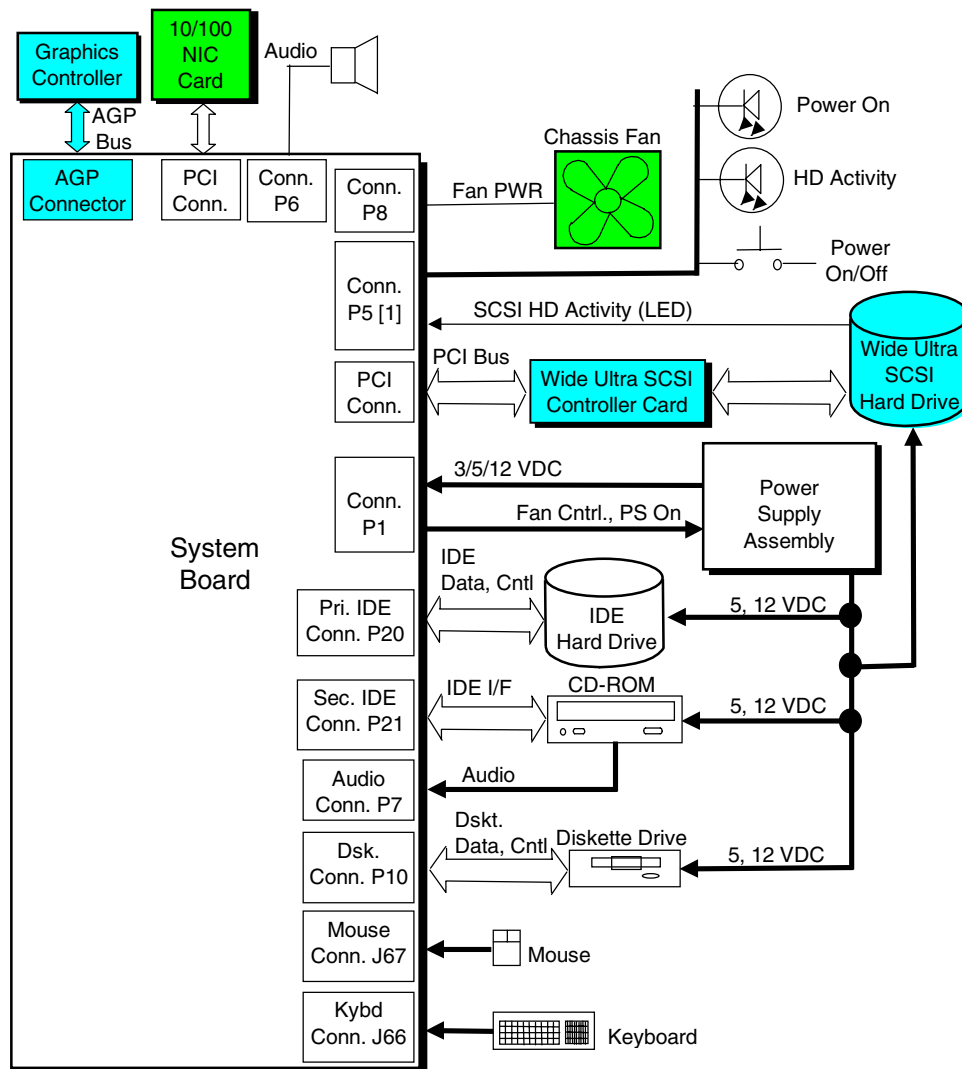
The VccP regulator produces the VccP (processor core) voltage according to the strapping of signals VID3..0 by the processor. The possible voltages available are listed as follows:

VID 3..0	VccP	VID 3..0	VccP
0000	2.05 VDC	1000	1.65 VDC
0001	2.00 VDC	1001	1.60 VDC
0010	1.95 VDC	1010	1.55 VDC
0011	1.90 VDC	1011	1.50 VDC
0100	1.85 VDC	1100	1.45 VDC
0101	1.80 VDC	1101	1.40 VDC
0110	1.75 VDC	1110	1.35 VDC
0111	1.70 VDC	1111	1.30 VDC

Refer to Chapter 3 for a listing of the core voltages set by the Celeron (Table 3-1) and Pentium III (Table 3-2) processors.

7.4 SIGNAL DISTRIBUTION

Figures 7-4 and 7-5 show general signal distribution between the main subassemblies of the system unit.



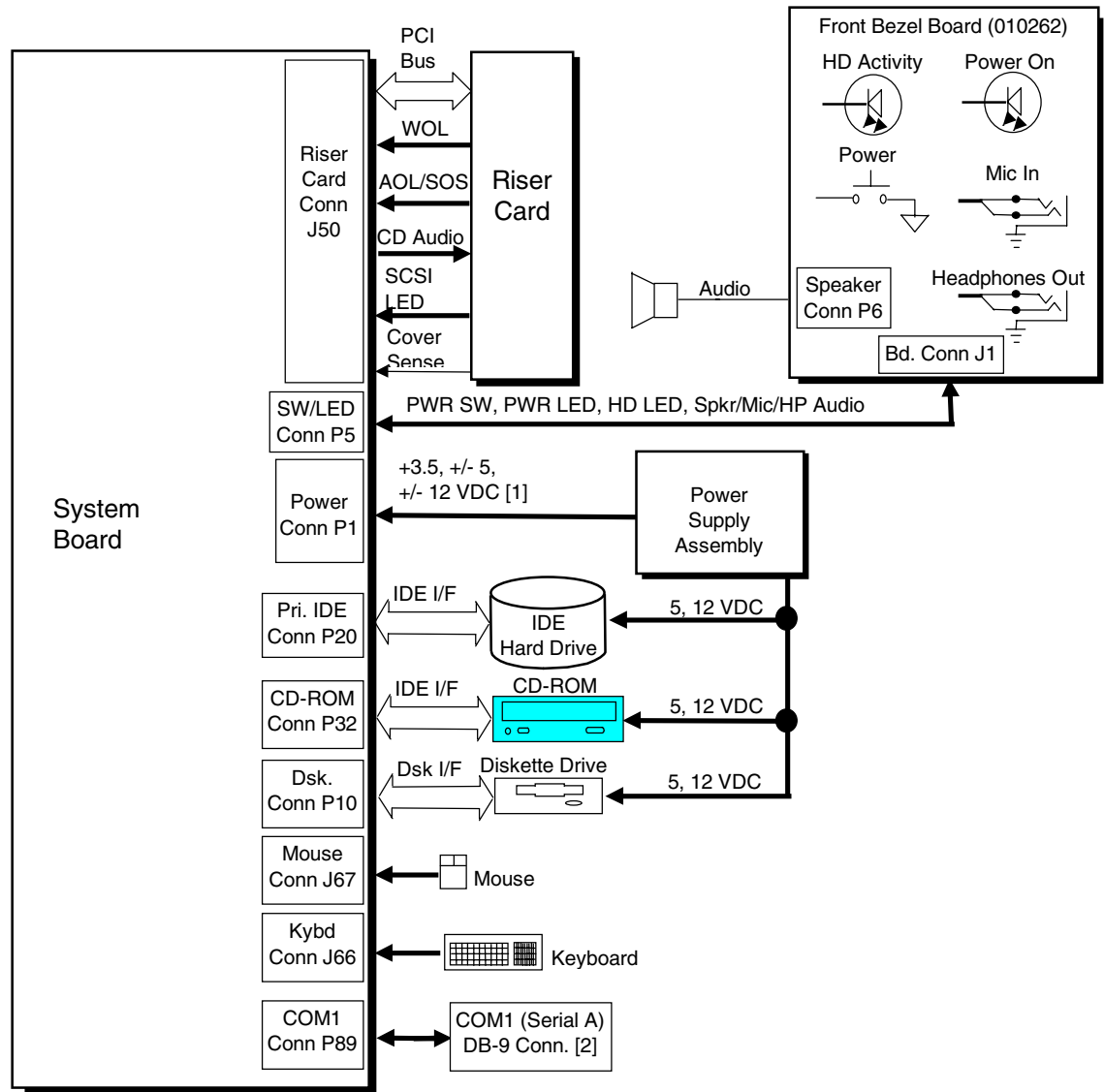
NOTES:

■ Deskpro Workstation AP250 only.

■ Some models

[1] See Figure 7-8 for header pinout.

Figure 7-5. Deskpro EP or Workstation AP250 Signal Distribution Diagram



NOTES:

[1] No cable used for interface; direct connection between PS assembly and system board.

[2] Connector mounted on rear chassis panel.

CDS Models only.

Figure 7-6. Deskpro EN SFF Signal Distribution Diagram

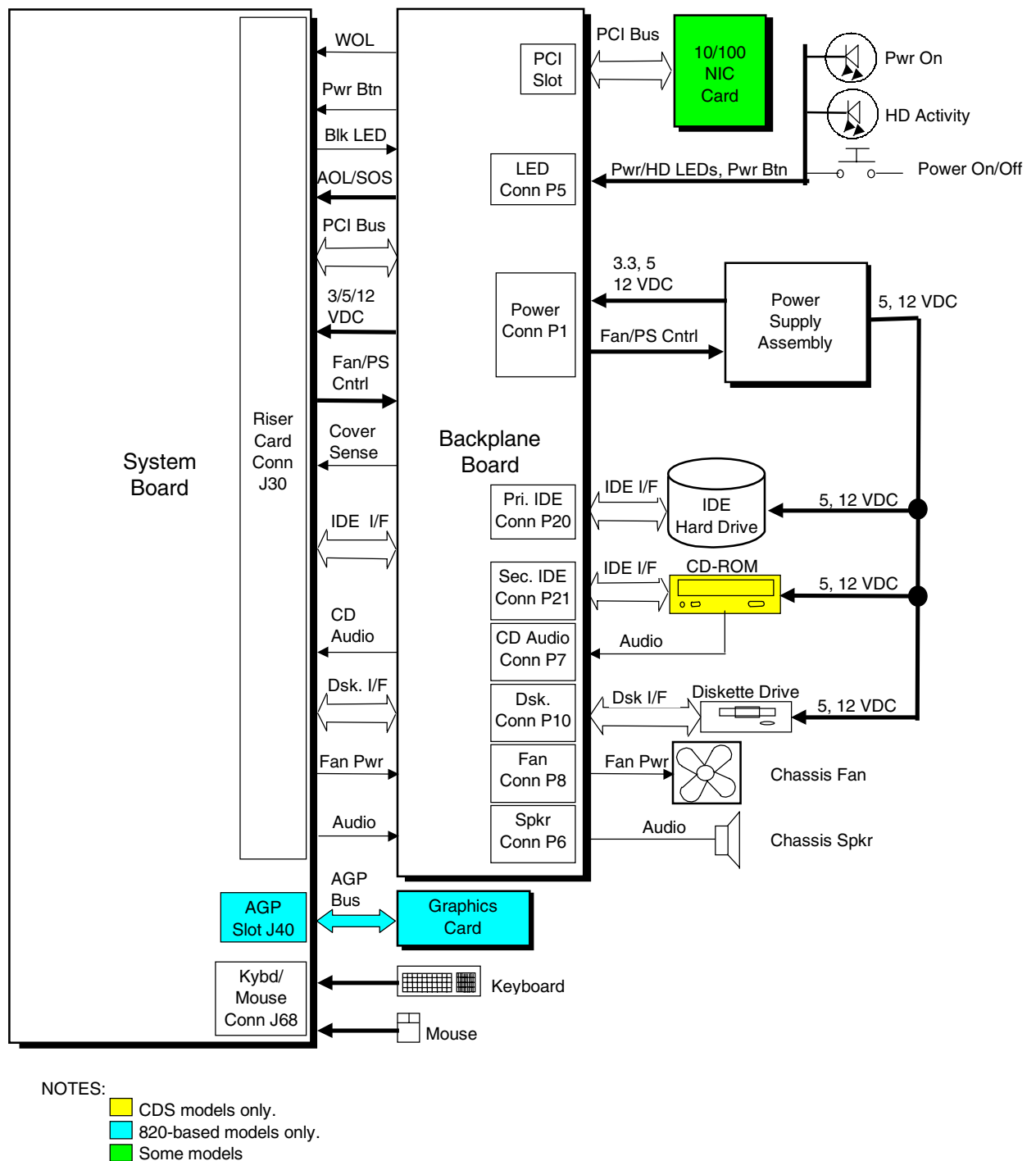
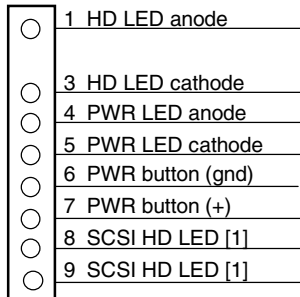
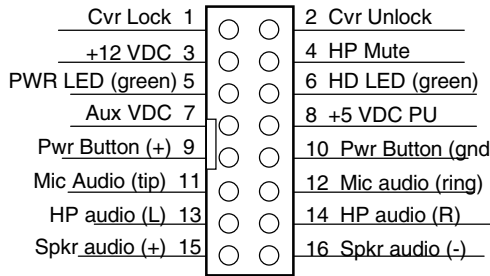


Figure 7-7. Deskpro EN DT/MT and Workstation AP240 Signal Distribution Diagram

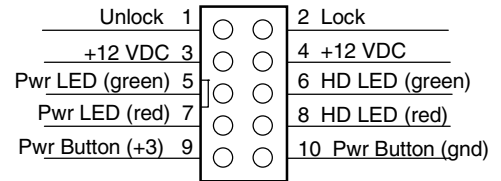
Power Button/LED Header P5
(Deskpro EP, Wkstn AP250)



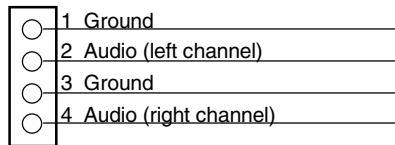
Power Button/LED Header P5
(Deskpro EN SFF)



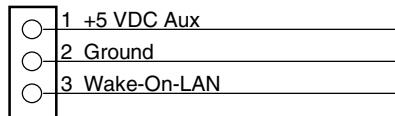
Power Button/LED Header P5
(Deskpro EN DT/MT, Wkstn AP240)



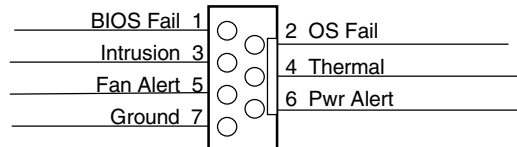
CD Audio Header P7



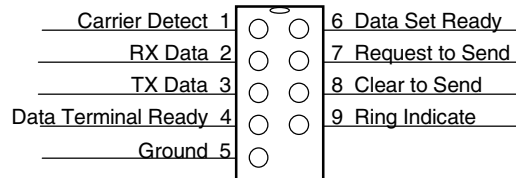
Wake-On-LAN Header P9



AOL/SOS Header P12



Serial Port A/COM1 Header P16
(Deskpro EN SFF)



NOTE:

No polarity consideration required for connection to speaker header P6 or SCSI HD LED header P29.
[1] Separate cable connection for these two pins (equivalent of header P29 on other systems).

Figure 7-8. Header Pinouts

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8.2 BOOT/RESET FUNCTIONS

The system supports new system boot functions to support remote ROM flashing and PC97 requirements. This system also supports the EL Torito specification for bootable CDs.

8.2.1 ROM FLASHING

The system BIOS firmware is contained in a flash ROM device that can be re-written with updated code if necessary. The system ROM is write-protected as follows:

<u>Start Addr.</u>	<u>End Addr.</u>	<u>Data Type</u>	<u>Protection</u>
C0000h	FFFFFh	Option ROM	Password write-protected
F0000h	F7FFFh	System BIOS	Password write-protected
F8000h	F9FFFh	ESCD	Never write-protected
FA000h	FFFFFh	Boot Block	Always write-protected

The flashing functions are handled using the INT15 AX-E822h BIOS interface.

8.2.2 BOOT BLOCK

This system includes 24 KB of write-protected boot block ROM that provides a way to recover from a failed remote flashing of the system BIOS ROM. Early during the boot process, the boot block code checks the system ROM. If validated, the system BIOS continues the boot sequence. If the system ROM fails the check, the boot block code provides the minimum amount of support necessary to allow booting the system from the diskette drive (bypassing the security measures) re-flashing the system ROM with a ROMPAQ diskette. Since video is not available during the initial boot sequence the boot block routine uses the keyboard LEDs to communicate status as follows:

<u>Num Lock</u>	<u>Caps Lock</u>	<u>Scroll Lock</u>	<u>Meaning</u>
Off	On	Off	Administrator password required.
On	Off	Off	Boot failed. Reset required for retry.
Off	Off	On	Flash failed (set by ROMPAQ).
On	On	On	Flash complete (set by ROMPAQ).

8.2.3 QUICKBOOT

The QuickBoot mode (programmable through the INT 15, AX=E845h call) skips certain portions of the POST (such as the memory count) during the boot process **unless** the hood has been detected as being removed. The QuickBoot mode is programmable as to be invoked always, never (default) or every x-number of days.

8.3 MEMORY DETECTION AND CONFIGURATION

This system uses the Serial Presence Detect (SPD) method of determining the installed DIMM configuration. The BIOS communicates with an EEPROM on each DIMM through an I²C-type bus to obtain data on the following DIMM parameters:

- ◆ Presence
- ◆ Size
- ◆ Type
- ◆ Timing/CAS latency

NOTE: Refer to Chapter 3, “Processor/Memory Subsystem” for the SPD format and DIMM data specific to this system.

The BIOS performs memory detection and configuration with the following steps:

1. Set Memory Buffer Strength – The memory controller must be configured for correct buffer drive strength. The BIOS provides this function by reading the number of module banks, ECC enable/disable status, and SDRAM width data from the DIMMs and transferring that data to the memory controller. SPD bytes checked: 5, 11, 13
2. Determine DIMM Presence/Type – The BIOS checks each memory socket for DIMM presence. If present, the DIMM type and CAS latency is determined. SPD bytes checked: 2, 9, 10, 18, 23, 24.
Check Sequence:
 - a. SPD byte 2 is read for all slots first. A failed read or returned value of other than 02h (EDO) or 04h (SDRAM) results in the slot marked as empty. If mixed types are detected then only SDRAMs are used (see chapter 3 for details).
 - b. SPD byte 18 is read for maximum CAS latency, followed by reads of bytes 9 and 10 for bus speed compatibility. A DIMM detected as too-slow results in an error.
 - c. If the DIMM can handle the memory bus speed at maximum CAS latency then bytes 23 and 24 are checked to see if the DIMM can work maximum CAS latency minus 1. Once all slots are checked, the greatest CAS latency (2 or 3) is used. A DIMM detected as incompatible will result in a bit in CMOS being set and the Num Lock LED on the keyboard will blink for a short time. Depending on the progress of the BIOS routine a POST message may be displayed before the system locks up.
3. Initialize SDRAM – If SDRAM are installed then each row containing SDRAM will be initialized. This step includes pre-charging all banks, sending a CAS-before-RAS command, sending a Mode-Register-Set-Enable command, reading DIMM location/CAS latency data, and sending a Normal Op command.
4. Memory Sizing – The SPD bytes 3, 4, and 17 are checked for number of row and column addresses and (for SDRAM) the number of internal banks.
5. Memory Timing – For SDRAM, the memory controller requires the RAS pre-charge time and the RAS-to-CAS delay time. SPD bytes checked: 27 and 29.

8.4 DESKTOP MANAGEMENT SUPPORT

Desktop Management deals with issues of security, identification, and system management functions. Desktop Management is provided by BIOS INT 15 functions listed Table 8-1.

Table 8-1. Desktop Management Functions (INT15)		
AX	Function	Mode
E800h	Get system ID	Real, 16-, & 32-bit Prot.
E807h	Get System Information Table	Real, 16-, & 32-bit Prot.
E813h	Get monitor information	Real, 16-, & 32-bit Prot.
E814h	Get system revision	Real, 16-, & 32-bit Prot.
E816h	Get temperature status	Real, 16-, & 32-bit Prot.
E817h	Get drive attribute	Real
E818h	Get drive off-line test	Real
E819h	Get chassis serial number	Real, 16-, & 32-bit Prot.
E81Ah	Write chassis serial number	Real
E81Bh	Get drive threshold	Real
E81Eh	Get drive ID	Real
E820h	System Memory Map	Real
E822h	Flash ROM/Sys. Admin. Fnc.	Real, 16-, & 32-bit Prot.
E827h	DIMM EEPROM Access	Real, 16-, & 32-bit Prot.
E828h	Inhibit power button	Real, 16-, & 32-bit Prot.
E845h	Access CMOS Feature Bits	Real, 16-, & 32-bit Prot.
E846h	Security Functions	Real, 16-, & 32-bit Prot.

All 32-bit protected mode calls are accessed by using the industry-standard BIOS32 Service Directory. Using the service directory involves three steps:

1. Locating the service directory.
2. Using the service directory to obtain the entry point for the client management functions.
3. Calling the client management service to perform the desired function.

The BIOS32 Service Directory is a 16-byte block that begins on a 16-byte boundary between the physical address range of 0E0000h-0FFFFFFh. The format is as follows:

<u>Offset</u>	<u>No. Bytes</u>	<u>Description</u>
00h	4	Service identifier (four ASCII characters)
04h	4	Entry point for the BIOS32 Service Directory
08h	1	Revision level
09h	1	Length of data structure (no. of 16-byte units)
0Ah	1	Checksum (should add up to 00h)
0Bh	5	Reserved (all 0s)

To support Windows NT an additional table to the BIOS32 table has been defined to contain 32-bit pointers for the DDC and SIT locations. The Windows NT extension table is as follows:

; Extension to BIOS SERVICE directory table (next paragraph)

```

db      "32OS"          ; sig
db      2                ; number of entries in table
db      "$DDC"          ; DDC POST buffer sig
dd      ?                ; 32-bit pointer
dw      ?                ; byte size
db      "$SIT"          ; SIT sig
dd      ?                ; 32-bit pointer
dw      ?                ; byte size
db      "$ERB"          ; ESCD sig
dd      ?                ; 32-bit pointer
dw      ?                ; bytes size

```

The service identifier for Desktop Management functions is "\$CLM." Once the service identifier is found and the checksum verified, a FAR call is invoked using the value specified at offset 04h to retrieve the CM services entry point. The following entry conditions are used for calling the Desktop Management service directory:

INPUT:

```

EAX      = Service Identifier [$CLM]
EBX (31..8) = Reserved
EBX (7..0) = Must be set to 00h
CS        = Code selector set to encompass the physical page holding
           entry point as well as the immediately following physical page.
           It must have the same base. CS is execute/read.
DS        = Data selector set to encompass the physical page holding
           entry point as well as the immediately following physical page.
           It must have the same base. DS is read only.
SS        = Stack selector must provide at least 1K of stack space and be 32-bit.
           (I/O permissions must be provided so that the BIOS can support as necessary)

```

OUTPUT:

```

AL        = Return code:
           00h, requested service is present
           80h, requested service is not present
           81h, un-implemented function specified in BL
           86h and CF=1, function not supported
EBX        = Physical address to use as the selector BASE for the service
ECX        = Value to use as the selector LIMIT for the service
EDX        = Entry point for the service relative to the BASE returned in EBX

```

The following subsections describe aspects of Desktop Management **unique to this system**. For a general description of these BIOS functions refer to the *Compaq BIOS Technical Reference Guide*.

8.4.1 SYSTEM ID

The INT 15, AX=E800h BIOS function can be used to identify the type of system. This function will return the system ID in the BX register.

System	ROM Type	System ID
Deskpro EP: 810 / Celeron-based	686J1	055Ch
810e / Pentium III-based	686J1	061Ch
Deskpro EN SFF: 810 / Celeron-based	686J1	0560h
810e / Pentium III-based	686J1	0620h
820 / Pentium III-based	686J2	0558h
Deskpro EN DT/MT: 810 / Celeron-based	686J1	054Ch
820 / Pentium III-based	686J2	0550h
Deskpro Workstation AP240	686J2	0550h
Deskpro Workstation AP250	686J2	0554h

8.4.2 SYSTEM INFORMATION TABLE

The System Information Table (SIT) is a comprehensive list of fixed configuration information arranged into records. The INT 15 AX=E807h BIOS function accesses the SIT by returning a pointer in ES:BX to indicate the location of the SIT. This section lists the default values that should be read from the SIT.

Power Conservation Record, SIT Record 01h

Byte	Function	Default Value
00h	Record ID	01h
01h	No. of Data Bytes in Record	0Bh
02h	Volume, CPU Speed, Screensave, PWR Consv. Mode	07h
03h	LED Blink, Popup, APM, PC Level, MAXBRIGHT Control	C4h
04h	SW Power Cntrl., Screensave/Hard Drive Timeouts, PWR	90h
05h	Magic Packet Flag, SMI, Modem Installed	[1]
06h-0Bh	Popup Location	[2]
0Ch	Quick Engy. Save, Magic Packet PWR, Suspend, CPU Sp.	39h

NOTES:

[1] Will be determined at runtime

[2] Unsupported function - read all 0s.

Timeout Counter Record (System Standby), SIT Record 02h

Byte	Function	Default Value
00h	Record ID for System Standby Timeout	02h
01h	No. of Data Bytes in Record	09h
02h	First Value	0
03h		10
04h		15
05h		20
06h		30
07h		60
08h		120
09h		180
0Ah	Last Value	240

Timeout Counter Record (Video Screensave), SIT Record 03h

Byte [1]	Function	Default Value
00h	Record ID for Video Screensave Timeout	03h
01h	No. of Data Bytes in Record	0Ch
02h	First Value	0
03h		5
04h		10
05h		15
06h		20
07h		30
08h		40
09h		50
0Ah		60
0Bh		120
0Ch		180
0Dh	Last Value	240

NOTE:

[1] Offset from byte 00h of timeout record 02h.

Timeout Counter Record (Hard Drive), SIT Record 04h

Byte [1]	Function	Default Value
15h	Record ID for Hard Drive Timeout	04h
16h	No. of Data Bytes in Record	06h
17h	First Value	0
18h		10
19h		15
1Ah		20
1Bh		30
1Ch	Last Value	60

NOTE:

[1] Offset from byte 00h of timeout record 02h.

Security Record, SIT Record 05h

Byte	Function	Default Value
00h	Record ID	05h
01h	No. of Data Bytes in Record	04h
02h	NVRAM/HD Lock, QuickLock/QuickBlank, FD Boot, PWR Pwd	7Fh
03h	Virus Detect, Serial/Parallel Cntrl., FD Drive Cntrl., Stby Cntrl.	1Fh
04h	Diskette Drive Fnct., Password Functions	7Ah
05h	Password Locking, Ownership Tag Length	[1]

NOTE:

[1] Determined by system at runtime.

Processor/Memory/Cache Record, SIT Record 06h

Byte	Function	Default Value
00h	Record ID	06h
01h	No. of Data Bytes in Record	0Eh
02h, 03h	Installed Microprocessor Speed	[1]
04h	Cache Configuration	07h
05h	L2 Cache Size	20h
06h	L2 Cache Speed	00h
07h	Total Memory Amount Adjustment	06h
08h, 09h	Total Soldered Memory	0000h
0Ah, 0Bh	Maximum Memory Installable	8001h
0Ch, 0Dh	Reserved	0000h
0Eh	Processor Designer	00h
0Fh	System Cache Error Correction	01h

NOTE: [1] Determined by system at runtime.

Peripheral and Input Device Record, SIT Record 07h

Byte	Function	Default Value
00h	Record ID	07h
01h	No. of Data Bytes in Record	3Ah
02h	DMA Functions, SCSI Support, Flashable ROM, Setup Partition, 101 Keyboard	27h
03h	Erase-Eaze Kybd. Support in ROM, El Torito CD Boot Support, QuickBoot, ROM Functions	53h
04h	Formfactor	[1]
05h	Softdrive 1 & 2 Data	FFh
06h	Softdrive 3 & 4 Data	FFh
07h-0Ah	Softdrive 1-4 Starting Address	B0 B5 BA BFh
0Bh	Panel ID	00h
0Ch	Integrated Monitor, ROM Socket, No. of Prog. Serial Ports	12h
0Dh	Parallel Port Mode, Modem Type	00h
0Eh	Drive Fault Prediction Support for Drives 0-3	[1]
0Fh, 10h	PCI Bus Master CMOS Data	0000h
11h, 12h	VGA Palette Snoop Function	0000h
13h	Misc. PCI Information	01h
14h, 15h	I/O Address for I ² C Device	0000h
16h	I ² C Information Byte	00h
17h	ATAPI Device Information (Logical Devices 1 & 2)	[1]
18h	ATAPI Device Information (Logical Devices 3 & 4)	[1]
19h	3-D Audio Support	00h
1Ah	BIOS Supported Features	01h
1Bh	Misc. Features (Power Inhibit Support)	01h
1Ch, 1Dh	Back-to-Back I/O Delay Index 0	[1]
1Eh, 1Fh	Back-to-Back I/O Delay Index 1	[1]
20h, 21h	Back-to-Back I/O Delay Index 2	[1]
22h, 23h	Back-to-Back I/O Delay Index 3	[1]
24h	Back-to-Back I/O Delay NVRAM Location	n/a
25h	Bit Mask for Byte 24h	n/a
26h	O/S Boot NVRAM Location	00h
27h	Bit Mask for Byte 26h	00h
28h-2Bh	IDE Drive 0-3 Max DMA/PIO Mode	[1]
2Ch-2Dh	Offset Address in EBDA for Bezel Button	n/a
2Eh	Processor Upgrade Mounting	06h
2Fh	Parallel Port Connector Type/Pinout	41h
30h	Serial Port Connector Type	01h
31h	Serial Port Maximum Speed	01h
32h	Serial Port Maximum Speed	C2h
33h	Serial Port Maximum Speed	00h
34h	DMA Burst Mode Support	[1]
35h	Keyboard Connector Type	03h
36h	System UDMA Capabilities	0Fh
37h	Diskette Type Installed	01h
38h	On-Board NIC Speed	00h
39h	On-Board NIC Attributes	00h
3Ah	General Purpose Software Support	[1]
3Bh	System EDMA Support	0Fh

NOTE:

[1] Determined at run time.

Memory Module Information Record, SIT Record 08h

Byte	Function	Default Value
00h	Record ID	08h
01h	No. of Data Bytes in Record	0Dh
02h	No. of Sockets	03h
03h	Memory Socket Location 0	00h
04h	Memory Installed In Location 0	[1]
05h	Memory Speed In Location 0	[1]
06h	Memory Form Factor 0	03h
07h	Memory Socket Location 1	01h
08h	Memory Installed In Location 1	[1]
09h	Memory Speed In Location 1	[1]
0Ah	Memory Form Factor 1	03h
0Bh	Memory Socket Location 2	02h
0Ch	Memory Installed In Location 2	[1]
0Dh	Memory Speed In Location 2	[1]
0Eh	Memory Form Factor 2	03h

NOTE: [1] Determined at runtime.

Timeout Default Record, SIT Record 09h

Byte	Function	Default Value
00h	Record ID	09h
01h	No. of Data Bytes in Record	0Ah
02h	High Power - Standby	15 min
03h	High Power - Hard Drive/System Idle	15 min
04h	High Power - Screensave	15 min
05h	High Power - Maximum Brightness	100 min
06h	High Power - Processor Speed	100 min
07h	Medium Power - Standby	15 min
08h	Medium Power - Hard Drive/System Idle	15 min
09h	Medium Power - Screensave	15 min
0Ah	Medium Power - Maximum Brightness	100 min
0Bh	Medium Power - Processor Speed	100 min

CMOS/NVRAM Information Record, SIT Record 0Ah

Byte	Function	Default Value
00h	Record ID	0Ah
01h	No. of Data Bytes in Record	05h
02h	Size of EISA NVRAM or Extended CMOS (Low Byte)	00h
03h	Size of EISA NVRAM or Extended CMOS (High Byte)	00h
04h	Size of High CMOS (Low Byte)	00h
05h	Size of High CMOS (High Byte)	00h
06h	NVRAM Storage Device Access Type	00h

Automatic Server Recovery Record, SIT Record 0Bh (Not Used)**Memory Banks Information Record, SIT Record 0Ch (Not Used)****Multiprocessor Feature Information Record, SIT Record 0Dh (Not Used)**

Extended Disk Support Record, SIT Record 0Eh

Byte	Function	Default Value
00h	Record ID	0Eh
01h	No. of Data Bytes in Record	02h
02h	Pointer To Extended Disk table (High Byte)	[1]
03h	Pointer To Extended Disk table (Low Byte)	[1]

NOTE: [1] Determined at runtime.

System Record, SIT Record 0Fh (Not Used)

Product Name Header Record, SIT Record 10h

Byte	Function	Default Value
00h	Record ID	10h
01h	No. of Data Bytes in Record	12h
02h-12	Product Name	"Compaq Deskpro EN"
13h	Terminator Byte	00h

DC-DC Converter Record, SIT Record 11h (Not Used)

Processor Microcode Patch Record, SIT Record 12h

Byte	Function	Default Value
00h	Record ID	12h
01h	No. of Data Bytes in Record	3Ch
02h-05h	Patch 1 Version	00000020h
06h-09h	Patch 1 Date	09031996h
0Ah-0Dh	Patch 1 Family/Model/Stepping	00000632h
0Eh-11h	Patch 2 Version	00000032h
12h-15h	Patch 2 Date	12121996h
16h-19h	Patch 2 Family/Model/Stepping	00000633h
1Ah-1Dh	Patch 3 Version	00000033h
1Eh-21h	Patch 3 Date	06161997h
22h-25h	Patch 3 Family/Model/Stepping	00000634h
26h-29h	Patch 4 Version	00000005h
2Ah-2Dh	Patch 4 Date	08151997h
2Eh-31h	Patch 4 Family/Model/Stepping	00000650h
32h-35h	Patch 5 Version	00000015h
36h-39h	Patch 5 Date	11241997h
3Ah-3Dh	Patch 5 Family/Model/Stepping	00000650h

System Hood Removal Record, SIT Record 13h

Byte	Function	Default Value
00h	Record ID	13h
01h	No. of Data Bytes in Record	09h
02h-05h	Hood Removed Time Stamp (Year/Month/Day/Hours/Min/Sec)	[1]
06h	Hood Removal Support CMOS Byte Offset	00h
07h	Hood Removal Support Bit Location	30h
08h	Hood Removal NOBOOT CMOS Byte Offset	00h
09h	Hood Removal NOBOOT CMOS Bit Location	00h
0Ah	Software Hood Lock	[1]

NOTE: [1] Determined at runtime.

DMI System Slots Support Record, SIT Record 16h

Byte	Function	Default Value
00h	Record ID	16h
01h	No. of Data Bytes in Record	1Ah
02h	Number of Slots	[1]
03h	Type of Slot	0Fh
04h	Data Width of Slot	05h
05h	Slot Usage/Length/Virtual	[1]
06h	Slot Category	03h
07h	Slot ID	00h
08h	Type of Slot	06h
09h	Data Width of Slot	05h
0Ah	Slot Usage/Length/Virtual	[1]
0Bh	Slot Category	03h
0Ch	Slot ID	01h
0Dh	Type of Slot	06h
0Eh	Data Width of Slot	05h
0Fh	Slot Usage/Length/Virtual	[1]
10h	Slot Category	03h
11h	Slot ID	02h
12h	Type of Slot	06h
13h	Data Width of Slot	05h
14h	Slot Usage/Length/Virtual	[1]
15h	Slot Category	03h
16h	Slot ID	03h
17h	Type of Slot	06h
18h	Data Width of Slot	05h
19h	Slot Usage/Length/Virtual	[1]
1Ah	Slot Category	03h
1Bh	Slot ID	04h

NOTE:

[1] Determined at runtime.

8.4.3 EDID RETRIEVE

The BIOS function INT 15, AX=E813h is a tri-modal call that retrieves the VESA extended display identification data (EDID). Two subfunctions are provided: AX=E813h BH=00h retrieves the EDID information while AX=E813h BX=01h determines the level of DDC support.

Input:

AX = E813h
 BH = 00 Get EDID .
 BH = 01 Get DDC support level

If BH = 00 then

DS:(E)SI = Pointer to a buffer (128 bytes) where ROM will return block

If 32-bit protected mode then

DS:(E)SI = Pointer to \$DDC location

Output:

(Successful)

If BH = 0:
 DS:SI=Buffer with EDID file.
 CX = Number of bytes written
 CF = 0
 AH =00h Completion of command

If BH = 1:

BH = System DDC support
 <0>=1 DDC1 support
 <1>=1 DDC2 support
 BL = Monitor DDC support
 <0>=1 DDC1 support
 <1>=1 DDC2 support
 <2>=1 Screen blanked during transfer

(Failure)

CF = 1
 AH = 86h or 87h

8.4.4 DRIVE FAULT PREDICTION

The Compaq BIOS provides direct Drive Fault Prediction support for IDE-type hard drives. This feature is provided through two BIOS calls. Function INT 15, AX=E817h is used to retrieve a 512-byte block of drive attribute data while the INT 15, AX=E81Bh is used to retrieve the drive's warranty threshold data. If data is returned indicating possible failure then the following message is displayed:

“1720-Intellisafe Hard Drive detects imminent failure”

8.4.5 SYSTEM MAP RETRIEVAL

The BIOS function INT 15, AX=E820h will return base memory and ISA/PCI memory contiguous with base memory as normal memory ranges. This real mode call will indicate chipset-defined address holes that are not in use, motherboard memory-mapped devices, and all occurrences of the system BIOS as reserved. Standard PC address ranges will not be reported.

Input:

EBX = continuation value or 00000000h to start at beginning of map
ECX = number of bytes to copy (>=20)
EDX = 534D4150h ('SMAP')
ES:DI = buffer for result (see below)

Offset	Size	Description
00h	QWORD	base address
08h	QWORD	length in bytes
10h	DWORD	type of address range
01h		memory, available to OS
02h		reserved, not available (e.g. system ROM, memory-mapped device)
other:		not defined

Output:

If CF=0 (success)

EAX = 534D4150h ('SMAP')
EBX = next offset from which to copy or 00000000h if finished
ECX = actual length returned in bytes
ES:DI = buffer filled

If CF=1 (failure)

AH = Error Code (86h)

In order to determine the entire memory map, multiple calls must be made.
For example, the first call would be:

Input:

EDX = 534D4150h
EBX = 00h
ECX = 14h
ES:DI = some buffer to store information.

Output:

EAX = 534D4150h
EBX = 01h
ECX = 14h
ES:DI = 00 00 00 00 00 00 00 00 00 FC 09 00 00 00 00 00 01 00 00 00
(indicates 0-639k is available to the OS)

Consecutive calls would continue until EBX returns with 0, indicating that the memory map is complete.

8.4.6 FLASH ROM FUNCTIONS

The system BIOS may be upgraded by flashing the ROM using the INT 15, AX=E822h BIOS interface, which includes the necessary subfunctions. An upgrade utility is provided on a ROMPAQ diskette. The upgrade procedure is described at the end of this chapter. Corrupted BIOS code will be indicated by the keyboard LEDs during the boot sequence as described previously in section 8.2.1.

8.4.7 POWER BUTTON FUNCTIONS

The BIOS includes an interface for controlling the system unit's power button. The power button can be disabled and enabled.

The INT 15, AX=E822h, BL=08h function can be invoked to disable the power button, preventing a user from inadvertently powering down the system. This tri-modal function is typically used in the ROM flashing procedure to reduce the chance of an accidental power down while the BIOS is being upgraded.

Entry:

```
AX    = E822h
BL    = 08h
```

Return:

(Successful)

```
CF    = 0
AH    = 00
```

(Failure)

```
CF    = 1
AH    = 86, not supported
```

NOTE: With the Disable function invoked the system can **still** be powered down by holding the power button in for four seconds or more.

The INT 15, AX=E822h, BL=09h function is used to restore the power button to the state it was in prior to invoking the Disable (BL=08h) function.

Entry:

```
AX    = E822h
BL    = 09h
```

Return:

(Successful)

```
CF    = 0
AH    = 00
```

(Failure)

```
CF    = 1
AH    = 86, call not supported
```


8.4.8 ACCESSING CMOS

Configuration memory data can be retrieved with the BIOS call INT 15, AX=E823h. This tri-modal function retrieves a single byte from the CMOS map described in Chapter 4. The function is described as follows:

INPUT:

EAX	= E823h
BH	= 0, Read
	= 1, Write
BL	= Value to write (if a write is specified)
CX	= Bytes number (zero-based)

OUTPUT:

(Successful)

CF	= 0
AH	= 00h
AL	= Byte value (on a read)

(Failure)

CF	= 1
AH	= 86h, Function not supported
	= FFh, byte does not exist

8.4.9 ACCESSING CMOS FEATURE BITS

The BIOS function INT 15, AX=E845h is a tri-modal call for accessing areas in non-volatile memory (CMOS) used for storing variables for various features. Note that this function differs from the previously discussed call since data blocks of varying lengths are retrieved.

INPUT:

EAX	= E845h
BL	= 0, Read
	= 1, Write
BH	= Value Read/to Write
CX	= Feature Bits Number (refer to Table 8-2)
DS:SI	= Pointer to buffer passing multiple byte features

OUTPUT:

(Successful)

CF	= 0
EAX	= Reserved
BH	= Value read (on a read)

(Failure)

CF	= 1
AH	= 86h, Function not supported

Table 8-2.
CMOS Feature Bits

CX	Function	Default Value	Default Setting	CX	Function	Default Value	Default Setting
0000h	PCI 2.1 Mode Enable	01h	Yes	0025h	Asset Tag	[3]	[3]
0001h	Erase Eaze Kybd	03h	Ign.	0026h	Bck-to-bck I/O Delay	00h	Norm
0002h	COM/IR Port Select	00h	COM	0027h	CMOS 10-2Fh BU	[3]	[3]
0003h	PnP Rejects SET	00h	Yes	0028h	QuickLock after Stby	00h	No
0004h	PCI VGA Snoop	00h	No	0029h	Audio Chip Enable	01h	Yes
0005h	PCI Bus Mastering	01h	No	002Ah	Audio IRQ	01h	IRQ5
0006h	Auto Prompt Setup	00h	Yes	002Bh	Audio DMA	02h	DMA1
0007h	Mode 2 Config. Enable	01h	Yes	002Ch	Audio Addr.	00h	22xh
0008h	Sec. IDE Cntrlr. En.	01h	Yes	002Dh	ECP DMA Config.	03h	DMA3
0009h	Sec. IDE Cntrlr. IRQ	03h	IRQ15	002Eh	COM1 Base Addr.	3Fh	3F8h
000Ah	Custom Drive Type 1	00h	[3]	002Fh	COM1 IRQ	00h	Rsrvd
000Bh	Custom Drive Type 2	00h	[3]	0030h	COM2 Base Addr.	1Fh	2F8h
000Ch	Custom Drive Type 3	00h	[3]	0031h	COM2 IRQ	00h	Rsrvd
000Dh	Custom Drive Type 4	00h	[3]	0032h	UDMA33 Enable		
000Eh	POST Verbose/Terse	01h	Terse	0033h	Net Server Md En.	00h	No
000Fh	Translate SCSI Drive	00h	Yes	0034h	CIA BOM No. Bytes	[3]	[3]
0010h	Mfg. Process no.	[3]	[3]	0035h	Copy Std. CMOS	[3]	[3]
0011h	Admin. Password	[3]	[3]	0036h	AGP Adapter Srch.	01h	Yes
0012h	Pwr-On Password	[3]	[3]	0037h	APM Fan Throttle	00h	Auto
0013h	Ownership Tag	[3]	[3]	0038h	Mfg. Diags. Enable	00h	No
0014h	Warm Boot Pswrd En.	00h	Yes	0039h	RIPL ROM Boot En.	01h	Yes
0015h	Hood Lock Enable [1]	00h	Yes	003Ah	Exit CleanBoot Scrn.	[3]	[3]
0016h	Hood Removal En. [1]	00h	No	003Bh	Ethernet Speed Sel.	00h	Auto
0017h	USB Security Enable	01h	Yes	003Ch	Ethernet Mode Sel.	00h	Auto
0018h	Power Supply Mode	01h	ACPI	003Dh	Ethernet Conn. Type	01h	UTP
0019h	QuickBoot Mode	1Fh	Fast	003Eh	ACPI Enable	01h	Yes
001Ah	Onbd NIC Enable [2]	01h	Yes	003Fh	S/W BOM S/N	[10]	[10]
001Bh	Onbd. SCSI Enable	01h	Yes	0040h	ECP Mode Selected	01h	Yes
001Ch	Onbd. Pri. IDE Enable	01h	Yes	0041h	NT Shutdown Dvr.	00h	No
001Dh	Ultra SCSI Md. Enable	00h	No	0042h	Em. SCSI Priority [1]	00h	Lowest
001Eh	QuickLock Enable	00h	No	0043h	Factor Boot Sel. [1]	00h	
001Fh	QuickBlank Enable	00h	No	0044h	Product Name	00h	[3]
0020h	Serial Port 1 Security	01h	No	0045h	UUID	00h	[3]
0021h	Serial Port 2 Security	01h	No	0046h	Processor # Enable	01h	Yes
0022h	Printer Port Security	01h	No	0047h	After G3 State	01h	On
0023h	CD/Diskette Boot	00h	Yes	0048h	UUID Enable	01h	Yes
0024h	CD/Diskette Write	00h	Yes	--	--	--	--

NOTE:

■ Not applicable to these systems.

[1] Deskpro EN systems only.

[2] Deskpro EN SFF systems only.

[3] Default Value will be pointer to buffer DS:SI (16-bit mode) or DS:(E)SI (32-bit mode) where actual data is held. Default Setting will be unique for each system.

8.4.10 SECURITY FUNCTIONS

The INT 15 AX=E846h BIOS function is used to control various security features of the system. This function may be issued by a remote system (over a network). The issuing driver must build a request buffer for each security feature prior to making the call. This system supports the following security features:

- ◆ QuickLock
- ◆ Diskette drive boot disable
- ◆ Diskette drive write disable
- ◆ IDE controller disable
- ◆ Serial ports disable
- ◆ Parallel port disable
- ◆ Change administrator password
- ◆ QuickLock on suspend
- ◆ Ownership tag
- ◆ USB disable

The write-protect function that determines diskette write control is extended to cover all drives that use removable read/write media (i.e., if diskette write protect is invoked, then any diskette drive, power drive (SCSI and/or ATAPI), and floptical drive installed will be inaccessible for (protected from) writes). Client management software should check the following bytes of SIT record 07h for the location and access method for this bit:

System Information Table, Peripheral and Input Device Record (07h) (partial listing)

Byte	Bit	Function
1Fh	7-0	Removable Read/Write Media Write Protect Enable Byte Offset (0-255)
20h	7..4	Removable Read/Write Media Write Protect Enable Bit Location: CMOS Type: 0000 = CMOS 0001 = High CMOS 0010 = NVRAM 0011 = Flat model NVRAM
	3..0	Bit Location: 0000 = Bit 0 0100 = Bit 4 0001 = Bit 1 0101 = Bit 5 0010 = Bit 2 0110 = Bit 6 0011 = Bit 3 0111 = Bit 7

8.5 PNP SUPPORT

The BIOS includes Plug 'n Play (PnP) support for PnP version 1.0A.

NOTE: For full PnP functionality to be realized, all peripherals used in the system must be designed as “PnP ready.” Any installed ISA peripherals that are not “PnP ready” can still be used in the system, although configuration parameters may need to be considered (and require intervention) by the user.

Table 8-2 shows the PnP functions supported (for detailed PnP information refer to the Compaq BIOS Technical Reference Guide):

Table 8-2.
PnP BIOS Functions

Function	Register
00h	Get number of system device nodes
01h	Get system device node
02h	Set system device node
03h	Get event
04h	Send message
50h	Get SMBIOS Structure Information
51h	Get Specific SMBIOS Structure

The BIOS call INT 15, AX=E841h, BH=01h can be used by an application to retrieve the default settings of PnP devices for the user. The application should use the following steps for the display function:

1. Call PnP function 01(get System Device Node) for each devnode with bit 1 of the control flag set (get static configuration) and save the results.
2. Call INT 15, AX=E841h, BH=01h.
3. Call PnP “Get Static Configuration” for each devnode and display the defaults.
4. If the user chooses to save the configuration, no further action is required. The system board devices will be configured at the next boot. If the user wants to abandon the changes, then the application must call PnP function 02 (Set System Device Node) for each devnode (with bit 1 of the control flag set for static configuration) with the results from the calls made prior to invoking this function.

8.5.1 SMBIOS

In support of the DMI specification the PnP functions 50h and 51h are used to retrieve the SMBIOS data. Function 50h retrieves the number of structures, size of the largest structure, and SMBIOS version. Function 51h retrieves a specific structure. This system supports SMBIOS version 2.1 and the following structure types:

<u>Type</u>	<u>Data</u>
0	BIOS Information
1	System Information
3	System Enclosure or Chassis
4	Processor Information
5	Memory Controller Information
6	Memory Module Information
7	Cache Information
8	Port Connector Information
9	System Slots
10	On Board Device Information
12	System Configuration Options
13	BIOS Language Information
16	Physical Memory Array
17	Memory Devices
18	Memory Error Information
19	Memory Array Mapped Addresses
20	Memory Device Mapped Addresses

8.6 POWER MANAGEMENT FUNCTIONS

The BIOS ROM provides three types of power management support: independent PM support; APM support, and ACPI support.

8.6.1 INDEPENDENT PM SUPPORT

The BIOS ROM can provide power management of the system independently from any software (OS or application) that is running on the system. In this mode the BIOS uses a timer to determine when to switch the system to a different power state. State switching is not reported to the OS and occurs as follows:

On – The computer is running normally and is drawing full power.

Standby – The computer is in a low power state. In this state the processor and chipset are still running and the VSYNC signal to the monitor is turned off. Returning to the On state requires very little time and will be initiated by any of the following actions:

- a. key stroke
- b. mouse movement

Off – The computer is not running and drawing practically no power at all.

8.6.2 ACPI SUPPORT

This system meets the hardware and firmware requirements for being ACPI compliant. The BIOS function INT 15 AX=E845h can be used to check or set the ACPI enable/disable status of the system, which defaults to the “ACPI enabled” state. The setup option for ACPI should be disabled if APM/PnP is to be used with Windows 98 or when disabling power management and PnP support for NT5.0. A hardware redetection should be made with Windows 98 and a reinstall of Windows NT5.0 should be performed when an ACPI switch is made.

This system supports the following ACPI functions:

- ◆ PM timer
- ◆ Power button
- ◆ Power button override
- ◆ RTC alarm
- ◆ Sleep/Wake logic (S1, S4 (NT), S5
- ◆ Legacy/ACPI select
- ◆ C1 state (Halt)
- ◆ C2 state (STOPGRANT)
- ◆ C3 state (no clock)
- ◆ PCI PME

8.6.3 APM 1.2 SUPPORT

Advanced Power Management (APM) BIOS support provides interaction between the BIOS ROM and the operating system (OS). The BIOS advises the OS when a power state transition should occur. The OS then notifies the appropriate driver(s) and reports back to the BIOS. For maximum energy-conservation benefit, APM functionality should be implemented using the following three layers:

- ◆ BIOS layer (APM BIOS (ver. 1.2, 1.1, 1.0))
- ◆ Operating system (OS) layer (APM driver)
- ◆ Application layer (APM-aware application or device driver)

The process starts with the OS or driver making a connection with the BIOS through an APM BIOS call. In a DOS environment POWER.EXE makes a Real mode connection. In Windows 3.1 and in Windows 95, a 32-bit connection is made. Currently Windows NT does not make an APM connection.

With power management enabled, inactivity timers are monitored. When an inactivity timer times out, an SMI is sent to the microprocessor to invoke the SMI handler. The SMI handler works with the APM driver and APM BIOS to take appropriate action based on which inactivity timer timed out.

Two I/O ports are used for APM communication with the SMI handler:

<u>Port Address</u>	<u>Name</u>
0B2h	APM Control
0B3h	APM Status

Three power states are defined under power management:

On - The computer is running, all subsystems are on and drawing full power. Any activity in the following subsystems will reset the activity timer, which has a default setting of 15 minutes before Standby entered:

- a. Keyboard
- b. Mouse
- c. Serial port
- d. Diskette drive
- e. Hard drive

Standby - The computer is in a low power state: video is off, some subsystems may be drawing less power, and the microprocessor is halted except for servicing interrupts. Video graphics controller is under driver control and/or VSYNC is off and the power supply fan is turned off. Any of the following activities will generate a wake-up SMI and return the system to On:

- a. Keyboard
- b. Mouse
- c. Serial port
- d. Diskette drive
- e. Hard drive
- f. RTC Alarm

If no APM connection is present, the BIOS will set an APM timer to 45 minutes, at which time the Suspend will be entered if no activity has occurred. This function can be defeated (so that Suspend will **not** be achieved). If an APM connection is present, the BIOS APM timer is not used and Suspend is entered only by user request either through an icon in Windows 95 or by pressing and releasing the power button under 4 seconds.

Suspend - The computer is in a low power state: video graphics controller is under driver control and/or HSYNC and VSYNC are off, some subsystems may be drawing less power, and the microprocessor is halted except for servicing interrupts. Any of the following activities will generate a wake-up SMI and return the system to On:

- a. Keyboard
- b. Mouse
- c. Serial port
- d. Diskette drive
- e. Hard drive
- f. RTC Alarm
- g. Network interface controller

The APM BIOS for this system supports APM 1.2 as well as previous versions 1.1 and 1.0. The APM BIOS functions are listed in Table 8-3.

Table 8-3.
APM BIOS Functions (INT15)

AX	Function
5300h	APM Installation Check
5301h	APM Connect (Real Mode)
5302h	APM Connect (16-bit Protected Mode)
5303h	APM Connect (32-bit Protected Mode)
5304h	Interface Disconnect
5305h	CPU Idle
5306h	CPU Busy
5307h	Set Power State [1]
5308h	Enable/Disable Power Management
5309h	Restore Power On Defaults
530Ah	Get Power Status
530Bh	Get PM Event
530Ch	Get Power State
530Dh	Enable/Disable Device Power Management
530Eh	APM Driver Version
530Fh	Engage/Disengage Power Management
5380h	OEM (Compaq) Specific APM Function

8.7 USB LEGACY SUPPORT

The BIOS ROM checks the USB port, during POST, for the presence of a USB keyboard. This allows a system with only a USB keyboard to be used during ROM-based setup and also on a system with an OS that does not include a USB driver.

On such a system a keystroke will generate an SMI and the SMI handler will retrieve the data from the device and convert it to PS/2 data. The data will be passed to the keyboard controller and processed as in the PS/2 interface. Changing the delay and/or typematic rate of a USB keyboard though BIOS function INT 16 is not supported.

The system does not support hot-plugging of a USB keyboard, nor is a keyboard attached to a USB hub supported. A PS/2 keyboard and a USB keyboard can, however, be connected and used simultaneously.

8.8 BIOS UPGRADING

The flash ROM device can be re-written with updated BIOS code if necessary. The flashing procedure is as follows:

1. Create a system (bootable) diskette using the **FORMAT A: /S** command in DOS.
2. Download the appropriate BIOS firmware from the Compaq web site.
3. Copy the downloaded BIOS file and the flash utility file onto the boot diskette.
4. Unzip the BIOS and flash utility files, which should result in an .exe file and a .bin file.
5. Place the boot diskette into drive A: and reboot the system.
6. At the A: prompt, type in "**filename.exe filename.bin**" (there is a space between the file names) and press **Enter**.
7. At the Flash Memory Write menu, to the question "Do you want to save BIOS?" select Y. If you want to save the current BIOS then type the current BIOS name and the extension after "File name to save" (example: type in 613j900.bin). Alternately, select N if you do not want to save the current BIOS.
8. To the question "Are you sure to program?" select Y.
9. Wait until the message "Power Off or Reset the system," indicating the BIOS has been loaded successfully. Then remove the boot diskette. **Should power be lost or the system reset during this time (before the message is displayed) the BIOS code in ROM will likely be corrupted and the procedure will have to be repeated (starting at step 5).**
10. Turn off (power down) the system.
11. While holding the **End** key down, turn on (power up) the system, making sure the **End** key is held down until the Setup utility is entered.
12. Complete the Setup utility as appropriate.
13. Re-boot the system.

If the BIOS code is corrupted due to a failed ROM flash the keyboard LEDs provide an indication of the problem during the boot process as described in section 8.2.1.

Appendix A

ERROR MESSAGES AND CODES

A.1 INTRODUCTION

This appendix lists the error codes and a brief description of the probable cause of the error. Note that not all errors listed in this appendix may be applicable to a particular system depending on the model and/or configuration.

A.2 POWER-ON MESSAGES

Table A-1.
Power-On Messages

Message	Beeps	Probable Cause
CMOS Time and Date Not Set	(None)	Invalid time or date
(none)	2 short	Power-On successful
Run Setup	(None)	Any failure

A.3 BEEP/KEYBOARD LED CODES

Table A-2.
Beep/Keyboard LED Codes

Beeps	LED [1]	Probable Cause
1 short, 2 long	NUM lock blinking	Base memory failure.
1 long, 2 short	CAP lock blinking	Video/graphics controller failure.
2 long, 1 short	Scroll lock blinking	System failure (prior to video initialization).
N/a	All three blink in sequence	Keyboard locked in network mode.
N/a	NUM lock steady on	ROMPAQ diskette not present, bad, or drive not ready.
N/a	CAP lock steady on	Password prompt.
N/a	All three blink together	ROM flash failed.
N/a	All three steady on	Successful ROM flash.

NOTE:

[1] PS/2 keyboard only.

A.4 POWER-ON SELF TEST (POST) MESSAGES

Table A-3.
Power-On Self Test (POST) Messages

Error Message	Probable Cause
Bad PnP Serial ID Checksum	Serial ID checksum of PnP card was invalid.
Address Lines Short!	Error in address decoding circuitry on system board.
Cache Memory Failure, Do Not Enable Cache!	Defective cache memory, CPU has failed.
CMOS Battery Failed	Low RTC/CMOS battery
CMOS Checksum Invalid	Previous and current checksum value mismatch.
CMOS System Options Not Set	Corrupt or non-existent CMOS values.
CMOS Display Type Mismatch	Graphics/video type in CMOS does not match type detected by BIOS.
CMOS Memory Size Mismatch	Memory amount detected does not match value stored in CMOS.
CMOS Time and Date Not Set	Time and date are invalid.
Diskette Boot Failure	Boot disk in drive A: is corrupt.
DMA Bus Timeout	Bus driven by device for more than 7.8 us
DMA Controller Error	Error in one or both DMA controllers.
Drive Not Ready Error	BIOS cannot access the diskette drive.
Diskette Drive Controller Failure	BIOS cannot communicate with diskette drive controller.
Diskette Drive Controller Resource Conflict	Diskette drive controller has requested a resource already in use.
Diskette Drive A: Failure	BIOS cannot access drive A:.
Diskette Drive B: Failure	BIOS cannot access drive B:.
Gate A20 Failure	Gate A20 of keyboard controller not working.
Invalid Boot Diskette	BIOS can read but cannot boot system from drive A:.
Keyboard Controller Error	Keyboard controller failure.
Keyboard is Locked...Please Unlock It	Locked keyboard.
Keyboard Stuck Key Detected	Key pressed down.
Master DMA Controller Error	Error exists in master DMA controller.
Master Interrupt Controller Error	Master interrupt controller failure.
Memory Size Decreased	Amount of memory detected is less than stated value in CMOS.
NVRAM Checksum Error, NVRAM Cleared	ESCD data was re-initialized due to NVRAM checksum error.
NVRAM Cleared By Jumper	NVRAM has been cleared by removal of jumper.
NVRAM Data Invalid, NVRAM Cleared	Invalid entry in ESCD.
Off Board Parity Error Addr. (HEX) = X	Parity error occurred in expansion memory, x= address of error.
Parallel Port Resource Conflict	Parallel port has requested a resource already in use.
PCI Error Log is Full	PCI conflict error limit (15) has been reached.
PCI I/O Port Conflict	Two devices requested the same resource.
PCI Memory Conflict	Two devices requested the same resource.
Primary Boot Device Not Found	Designated primary boot device could not be found.
Primary IDE Cntrl. Resource Conflict	Primary IDE controller requested a resource already in use.
Primary Input Device Not Found	Designated primary input device could not be found.
Secondary IDE Controller Resource	Secondary IDE controller has requested a resource already in use.
Serial Port 1 Resource Conflict	Serial port 1 requested a resource already in use.
Serial Port 2 Resource Conflict	Serial port 2 requested a resource already in use.
Slave DMA Controller Error	Error exists in slave DMA controller.
Slave Interrupt Controller Error	Slave interrupt controller failure.
Static Device Resource Conflict	A non-PnP ISA card has requested a resource already in use.
System Board Device Resource Conflict	A non-PnP ISA card has requested a resource already in use.
System Memory Size Mismatch	Amount of memory detected on system board is different from amount indicated in CMOS.

NOTE:

PCI and PnP messages are displayed with bus, device, and function information.

A.5 PROCESSOR ERROR MESSAGES (1xx-xx)

Table A-4.
Processor Error Messages

Message	Probable Cause	Message	Probable Cause
101-01	CPU test failed	105-10	Port 61 I/O test failed
101-02	32-bit CPU test failed	105-11	Port 61 bit <7> not at zero
101-91..94	Multiplication test failed	105-12	Port 61 bit <2> not at zero
102-01	FPU initial sts. word incorrect	105-13	No interrupt generated by failsafe timer
102-02	FPU initial cntrl. Word incorrect	105-14	NMI not triggered by failsafe timer
102-03	FPU tag word not all ones	106-01	Keyboard controller test failed
102-04	FPU tag word not all zeros	107-01	CMOS RAM test failed
102-05	FPU exchange command failed	108-02	CMOS interrupt test failed
102-06	FPU masked exception error	108-03	CMOS not properly initialized (interrupt test)
102-07	FPU unmasked exception error	109-01	CMOS clock load data test failed
102-08	FPU wrong mask status bit set	109-02	CMOS clock rollover test failed
102-09	FPU unable to store real number	109-03	CMOS not properly initialized (clock test)
102-10	FPU real number calc test failed	110-01	Programmable timer load data test failed
102-11	FPU speed test failed	110-02	Programmable timer dynamic test failed
102-12	FPU pattern test failed	110-03	Program timer 2 load data test failed
102-15	FPU is inoperative or not present	111-01	Refresh detect test failed
102-16	Weitek not responding	112-01	Speed test Slow mode out of range
102-17	Weitek failed register trnsfr. Test	112-02	Speed test Mixed mode out of range
102-18	Weitek failed arithmetic ops test	112-03	Speed test Fast mode out of range
102-19	Weitek failed data conv. Test	112-04	Speed test unable to enter Slow mode
102-20	Weitek failed interrupt test	112-05	Speed test unable to enter Mixed mode
102-21	Weitek failed speed test	112-06	Speed test unable to enter Fast mode
103-01	DMA page registers test failed	112-07	Speed test system error
103-02	DMA byte controller test failed	112-08	Unable to enter Auto mode in speed test
103-03	DMA word controller test failed	112-09	Unable to enter High mode in speed test
104-01	Master int. cntrl. test failed	112-10	Speed test High mode out of range
104-02	Slave int. cntrl. test failed	112-11	Speed test Auto mode out of range
104-03	Int. cntrl. SW RTC inoperative	112-12	Speed test variable speed mode inoperative
105-01	Port 61 bit <6> not at zero	113-01	Protected mode test failed
105-02	Port 61 bit <5> not at zero	114-01	Speaker test failed
105-03	Port 61 bit <3> not at zero	116-xx	Way 0 read/write test failed
105-04	Port 61 bit <1> not at zero	162-xx	System options failed (mismatch in drive type)
105-05	Port 61 bit <0> not at zero	163-xx	Time and date not set
105-06	Port 61 bit <5> not at one	164-xx	Memory size
105-07	Port 61 bit <3> not at one	199-00	Installed devices test failed
105-08	Port 61 bit <1> not at one	--	--
105-09	Port 61 bit <0> not at one	--	--

A.6 MEMORY ERROR MESSAGES (2xx-xx)

Table A-5.
Memory Error Messages

Message	Probable Cause
200-04	Real memory size changed
200-05	Extended memory size changed
200-06	Invalid memory configuration
200-07	Extended memory size changed
200-08	CLIM memory size changed
201-01	Memory machine ID test failed
202-01	Memory system ROM checksum failed
202-02	Failed RAM/ROM map test
202-03	Failed RAM/ROM protect test
203-01	Memory read/write test failed
203-02	Error while saving block in read/write test
203-03	Error while restoring block in read/write test
204-01	Memory address test failed
204-02	Error while saving block in address test
204-03	Error while restoring block in address test
204-04	A20 address test failed
204-05	Page hit address test failed
205-01	Walking I/O test failed
205-02	Error while saving block in walking I/O test
205-03	Error while restoring block in walking I/O test
206-xx	Increment pattern test failed
207-xx	ECC failure
210-01	Memory increment pattern test
210-02	Error while saving memory during increment pattern test
210-03	Error while restoring memory during increment pattern test
211-01	Memory random pattern test
211-02	Error while saving memory during random memory pattern test
211-03	Error while restoring memory during random memory pattern test
213-xx	Incompatible DIMM in slot x
214-xx	Noise test failed
215-xx	Random address test

A.7 KEYBOARD ERROR MESSAGES (30x-xx)

Table A-6.
Keyboard Error Messages

Message	Probable Cause	Message	Probable Cause
300-xx	Failed ID test	303-05	LED test, LED command test failed
301-01	Kybd short test, 8042 self-test failed	303-06	LED test, LED command test failed
301-02	Kybd short test, interface test failed	303-07	LED test, LED command test failed
301-03	Kybd short test, echo test failed	303-08	LED test, command byte restore test failed
301-04	Kybd short test, kybd reset failed	303-09	LED test, LEDs failed to light
301-05	Kybd short test, kybd reset failed	304-01	Keyboard repeat key test failed
302-xx	Failed individual key test	304-02	Unable to enter mode 3
302-01	Kybd long test failed	304-03	Incorrect scan code from keyboard
303-01	LED test, 8042 self-test failed	304-04	No Make code observed
303-02	LED test, reset test failed	304-05	Cannot /disable repeat key feature
303-03	LED test, reset failed	304-06	Unable to return to Normal mode
303-04	LED test, LED command test failed	--	--

A.8 PRINTER ERROR MESSAGES (4xx-xx)

Table A-7.
Printer Error Messages

Message	Probable Cause	Message	Probable Cause
401-01	Printer failed or not connected	402-11	Interrupt test, data/cntrl. reg. failed
402-01	Printer data register failed	402-12	Interrupt test and loopback test failed
402-02	Printer control register failed	402-13	Int. test, LpBk. test., and data register failed
402-03	Data and control registers failed	402-14	Int. test, LpBk. test., and cntrl. register failed
402-04	Loopback test failed	402-15	Int. test, LpBk. test., and data/cntrl. reg. failed
402-05	Loopback test and data reg. failed	402-16	Unexpected interrupt received
402-06	Loopback test and cntrl. reg. failed	402-01	Printer pattern test failed
402-07	Loopback tst, data/cntrl. reg. failed	403-xx	Printer pattern test failed
402-08	Interrupt test failed	404-xx	Parallel port address conflict
402-09	Interrupt test and data reg. failed	498-00	Printer failed or not connected
402-10	Interrupt test and control reg. failed	--	--

A.9 VIDEO (GRAPHICS) ERROR MESSAGES (5xx-xx)

Table A-8.
Video (Graphics) Error Messages

Message	Probable Cause	Message	Probable Cause
501-01	Video controller test failed	508-01	320x200 mode, color set 0 test failed
502-01	Video memory test failed	509-01	320x200 mode, color set 1 test failed
503-01	Video attribute test failed	510-01	640x200 mode test failed
504-01	Video character set test failed	511-01	Screen memory page test failed
505-01	80x25 mode, 9x14 cell test failed	512-01	Gray scale test failed
506-01	80x25 mode, 8x8 cell test failed	514-01	White screen test failed
507-01	40x25 mode test failed	516-01	Noise pattern test failed

See Table A-14 for additional graphics messages.

A.10 DISKETTE DRIVE ERROR MESSAGES (6xx-xx)

Table A-9.
Diskette Drive Error Messages

Message	Probable Cause	Message	Probable Cause
6xx-01	Exceeded maximum soft error limit	6xx-20	Failed to get drive type
6xx-02	Exceeded maximum hard error limit	6xx-21	Failed to get change line status
6xx-03	Previously exceeded max soft limit	6xx-22	Failed to clear change line status
6xx-04	Previously exceeded max hard limit	6xx-23	Failed to set drive type in ID media
6xx-05	Failed to reset controller	6xx-24	Failed to read diskette media
6xx-06	Fatal error while reading	6xx-25	Failed to verify diskette media
6xx-07	Fatal error while writing	6xx-26	Failed to read media in speed test
6xx-08	Failed compare of R/W buffers	6xx-27	Failed speed limits
6xx-09	Failed to format a tract	6xx-28	Failed write-protect test
6xx-10	Failed sector wrap test	--	--

600-xx = Diskette drive ID test	609-xx = Diskette drive reset controller test
601-xx = Diskette drive format	610-xx = Diskette drive change line test
602-xx = Diskette read test	611-xx = Pri. diskette drive port addr. conflict
603-xx = Diskette drive R/W compare test	612-xx = Sec. diskette drive port addr. conflict
604-xx = Diskette drive random seek test	694-00 = Pin 34 not cut on 360-KB drive
605-xx = Diskette drive ID media	697-00 = Diskette type error
606-xx = Diskette drive speed test	698-00 = Drive speed not within limits
607-xx = Diskette drive wrap test	699-00 = Drive/media ID error (run Setup)
608-xx = Diskette drive write-protect test	

A.11 SERIAL INTERFACE ERROR MESSAGES (11xx-xx)

Table A-10.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1101-01	UART DLAB bit failure	1101-13	UART cntrl. signal interrupt failure
1101-02	Line input or UART fault	1101-14	DRVR/RCVR data failure
1101-03	Address line fault	1109-01	Clock register initialization failure
1101-04	Data line fault	1109-02	Clock register rollover failure
1101-05	UART cntrl. signal failure	1109-03	Clock reset failure
1101-06	UART THRE bit failure	1109-04	Input line or clock failure
1101-07	UART Data RDY bit failure	1109-05	Address line fault
1101-08	UART TX/RX buffer failure	1109-06	Data line fault
1101-09	Interrupt circuit failure	1150-xx	Comm port setup error (run Setup)
1101-10	COM1 set to invalid INT	1151-xx	COM1 address conflict
1101-11	COM2 set to invalid INT	1152-xx	COM2 address conflict
1101-12	DRVR/RCVR cntrl. signal failure	1155-xx	COM port address conflict

A.12 MODEM COMMUNICATIONS ERROR MESSAGES (12xx-xx)

Table A-11.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1201-XX	Modem internal loopback test	1204-03	Data block retry limit reached [4]
1201-01	UART DLAB bit failure	1204-04	RX exceeded carrier lost limit
1201-02	Line input or UART failure	1204-05	TX exceeded carrier lost limit
1201-03	Address line failure	1204-06	Time-out waiting for dial tone
1201-04	Data line fault	1204-07	Dial number string too long
1201-05	UART control signal failure	1204-08	Modem time-out waiting for remote response
1201-06	UART THRE bit failure	1204-09	Modem exceeded maximum redial limit
1201-07	UART DATA READY bit failure	1204-10	Line quality prevented remote response
1201-08	UART TX/RX buffer failure	1204-11	Modem time-out waiting for remote connection
1201-09	Interrupt circuit failure	1205-XX	Modem auto answer test
1201-10	COM1 set to invalid interrupt	1205-01	Time-out waiting for SYNC [5]
1201-11	COM2 set to invalid	1205-02	Time-out waiting for response [5]
1201-12	DRVVR/RCVR control signal failure	1205-03	Data block retry limit reached [5]
1201-13	UART control signal interrupt failure	1205-04	RX exceeded carrier lost limit
1201-14	DRVVR/RCVR data failure	1205-05	TX exceeded carrier lost limit
1201-15	Modem detection failure	1205-06	Time-out waiting for dial tone
1201-16	Modem ROM, checksum failure	1205-07	Dial number string too long
1201-17	Tone detect failure	1205-08	Modem time-out waiting for remote response
1202-XX	Modem internal test	1205-09	Modem exceeded maximum redial limit
1202-01	Time-out waiting for SYNC [1]	1205-10	Line quality prevented remote response
1202-02	Time-out waiting for response [1]	1205-11	Modem time-out waiting for remote connection
1202-03	Data block retry limit reached [1]	1206-XX	Dial multi-frequency tone test
1202-11	Time-out waiting for SYNC [2]	1206-17	Tone detection failure
1202-12	Time-out waiting for response [2]	1210-XX	Modem direct connect test
1202-13	Data block retry limit reached [2]	1210-01	Time-out waiting for SYNC [6]
1202-21	Time-out waiting for SYNC [3]	1210-02	Time-out waiting for response [6]
1202-22	Time-out waiting for response [3]	1210-03	Data block retry limit reached [6]
1202-23	Data block retry limit reached [3]	1210-04	RX exceeded carrier lost limit
1203-XX	Modem external termination test	1210-05	TX exceeded carrier lost limit
1203-01	Modem external TIP/RING failure	1210-06	Time-out waiting for dial tone
1203-02	Modem external data TIP/RING fail	1210-07	Dial number string too long
1203-03	Modem line termination failure	1210-08	Modem time-out waiting for remote response
1204-XX	Modem auto originate test	1210-09	Modem exceeded maximum redial limit
1204-01	Time-out waiting for SYNC [4]	1210-10	Line quality prevented remote response
1204-02	Time-out waiting for response [4]	1210-11	Modem time-out waiting for remote connection

NOTES:

- [1] Local loopback mode
- [2] Analog loopback originate mode
- [3] Analog loopback answer mode
- [4] Modem auto originate test
- [5] Modem auto answer test
- [6] Modem direct connect test

A.13 SYSTEM STATUS ERROR MESSAGES (16xx-xx)

Table A-12.
System Status Error Messages

Message	Probable Cause
1601-xx	Temperature violation
1611-xx	Fan failure

See Table A-18 for additional messages.

A.14 HARD DRIVE ERROR MESSAGES (17xx-xx)

Table A-13.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
17xx-01	Exceeded max. soft error limit	17xx-51	Failed I/O read test
17xx-02	Exceeded max. Hard error limit	17xx-52	Failed file I/O compare test
17xx-03	Previously exceeded max. soft error limit	17xx-53	Failed drive/head register test
17xx-04	Previously exceeded max.hard error limit	17xx-54	Failed digital input register test
17xx-05	Failed to reset controller	17xx-55	Cylinder 1 error
17xx-06	Fatal error while reading	17xx-56	Failed controller RAM diagnostics
17xx-07	Fatal error while writing	17xx-57	Failed controller-to-drive diagnostics
17xx-08	Failed compare of R/W buffers	17xx-58	Failed to write sector buffer
17xx-09	Failed to format a track	17xx-59	Failed to read sector buffer
17xx-10	Failed diskette sector wrap during read	17xx-60	Failed uncorrectable ECC error
17xx-19	Cntrl. failed to deallocate bad sectors	17xx-62	Failed correctable ECC error
17xx-40	Cylinder 0 error	17xx-63	Failed soft error rate
17xx-41	Drive not ready	17xx-65	Exceeded max. bad sectors per track
17xx-42	Failed to recalibrate drive	17xx-66	Failed to initialize drive parameter
17xx-43	Failed to format a bad track	17xx-67	Failed to write long
17xx-44	Failed controller diagnostics	17xx-68	Failed to read long
17xx-45	Failed to get drive parameters from ROM	17xx-69	Failed to read drive size
17xx-46	Invalid drive parameters from ROM	17xx-70	Failed translate mode
17xx-47	Failed to park heads	17xx-71	Failed non-translate mode
17xx-48	Failed to move hard drive table to RAM	17xx-72	Bad track limit exceeded
17xx-49	Failed to read media in file write test	17xx-73	Previously exceeded bad track limit
17xx-50	Failed I/O write test	--	--

1700-xx = Hard drive ID test
 1701-xx = Hard drive format test
 1702-xx = Hard drive read test
 1703-xx = Hard drive read/write compare test
 1704-xx = Hard drive random seek test
 1705-xx = Hard drive controller test
 1706-xx = Hard drive ready test
 1707-xx = Hard drive recalibrate test
 1708-xx = Hard drive format bad track test
 1709-xx = Hard drive reset controller test
 1710-xx = Hard drive park head test
 1714-xx = Hard drive file write test
 1715-xx = Hard drive head select test
 1716-xx = Hard drive conditional format test
 1717-xx = Hard drive ECC test

1719-xx = Hard drive power mode test
 1720-xx = SMART drive detects imminent failure
 1721-xx = SCSI hard drive imminent failure
 1724-xx = Net work preparation test
 1736-xx = Drive monitoring test
 1771-xx = Pri. IDE controller address conflict
 1772-xx = Sec. IDE controller address conflict
 1780-xx = Disk 0 failure
 1781-xx = Disk 1 failure
 1782-xx = Pri. IDE controller failure
 1790-xx = Disk 0 failure
 1791-xx = Disk 1 failure
 1792-xx = Se. controller failure
 1793-xx = Sec. Controller or disk failure
 1799-xx = Invalid hard drive type

A.15 HARD DRIVE ERROR MESSAGES (19xx-xx)

Table A-14.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
19xx-01	Drive not installed	19xx-21	Got servo pulses second time but not first
19xx-02	Cartridge not installed	19xx-22	Never got to EOT after servo check
19xx-03	Tape motion error	19xx-23	Change line unset
19xx-04	Drive busy error	19xx-24	Write-protect error
19xx-05	Track seek error	19xx-25	Unable to erase cartridge
19xx-06	Tape write-protect error	19xx-26	Cannot identify drive
19xx-07	Tape already Servo Written	19xx-27	Drive not compatible with controller
19xx-08	Unable to Servo Write	19xx-28	Format gap error
19xx-09	Unable to format	19xx-30	Exception bit not set
19xx-10	Format mode error	19xx-31	Unexpected drive status
19xx-11	Drive recalibration error	19xx-32	Device fault
19xx-12	Tape not Servo Written	19xx-33	Illegal command
19xx-13	Tape not formatted	19xx-34	No data detected
19xx-14	Drive time-out error	19xx-35	Power-on reset occurred
19xx-15	Sensor error flag	19xx-36	Failed to set FLEX format mode
19xx-16	Block locate (block ID) error	19xx-37	Failed to reset FLEX format mode
19xx-17	Soft error limit exceeded	19xx-38	Data mismatch on directory track
19xx-18	Hard error limit exceeded	19xx-39	Data mismatch on track 0
19xx-19	Write (probably ID) error	19xx-40	Failed self-test
19xx-20	NEC fatal error	19xx-91	Power lost during test

1900-xx = Tape ID test failed

1901-xx = Tape servo write failed

1902-xx = Tape format failed

1903-xx = Tape drive sensor test failed

1904-xx = Tape BOT/EOT test failed

1905-xx = Tape read test failed

1906-xx = Tape R/W compare test failed

1907-xx = Tape write-protect failed

A.16 VIDEO (GRAPHICS) ERROR MESSAGES (24xx-xx)

Table A-15.
Video (Graphics) Error Messages

Message	Probable Cause	Message	Probable Cause
2402-01	Video memory test failed	2418-02	EGA shadow RAM test failed
2403-01	Video attribute test failed	2419-01	EGA ROM checksum test failed
2404-01	Video character set test failed	2420-01	EGA attribute test failed
2405-01	80x25 mode, 9x14 cell test failed	2421-01	640x200 mode test failed
2406-01	80x25 mode, 8x8 cell test failed	2422-01	640x350 16-color set test failed
2407-01	40x25 mode test failed	2423-01	640x350 64-color set test failed
2408-01	320x200 mode color set 0 test failed	2424-01	EGA Mono. text mode test failed
2409-01	320x200 mode color set 1 test failed	2425-01	EGA Mono. graphics mode test failed
2410-01	640x200 mode test failed	2431-01	640x480 graphics mode test failed
2411-01	Screen memory page test failed	2432-01	320x200 256-color set test failed
2412-01	Gray scale test failed	2448-01	Advanced VGA controller test failed
2414-01	White screen test failed	2451-01	132-column AVGA test failed
2416-01	Noise pattern test failed	2456-01	AVGA 256-color test failed
2417-01	Lightpen text test failed, no response	2458-xx	AVGA BitBLT test failed
2417-02	Lightpen text test failed, invalid response	2468-xx	AVGA DAC test failed
2417-03	Lightpen graphics test failed, no resp.	2477-xx	AVGA data path test failed
2417-04	Lightpen graphics test failed, invalid resp.	2478-xx	AVGA BitBLT test failed
2418-01	EGA memory test failed	2480-xx	AVGA linedraw test failed

A.17 AUDIO ERROR MESSAGES (3206-xx)

Table A-16.
Audio Error Message

Message	Probable Cause
3206-xx	Audio subsystem internal error

A.18 DVD/CD-ROM ERROR MESSAGES (33xx-xx)

Table A-17.
DVD/CD-ROM Drive Error Messages

Message	Probable Cause
3301-xx	Drive test failed
3305-XX	Seek test failed

See Table A-18 for additional messages.

A.19 NETWORK INTERFACE ERROR MESSAGES (60xx-xx)

Table A-18.
Network Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6000-xx	Pointing device interface error	6054-xx	Token ring configuration test failed
6014-xx	Ethernet configuration test failed	6056-xx	Token ring reset test failed
6016-xx	Ethernet reset test failed	6068-xx	Token ring int. loopback test failed
6028-xx	Ethernet int. loopback test failed	6069-xx	Token ring ext. loopback test failed
6029-xx	Ethernet ext. loopback test failed	6089-xx	Token ring open

A.20 SCSI INTERFACE ERROR MESSAGES (65xx-xx, 66xx-xx, 67xx-xx)

Table A-19.
SCSI Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6nny-02	Drive not installed	6nny-33	Illegal controller command
6nny-03	Media not installed	6nny-34	Invalid SCSI bus phase
6nny-05	Seek failure	6nny-35	Invalid SCSI bus phase
6nny-06	Drive timed out	6nny-36	Invalid SCSI bus phase
6nny-07	Drive busy	6nny-39	Error status from drive
6nny-08	Drive already reserved	6nny-40	Drive timed out
6nny-09	Reserved	6nny-41	SSI bus stayed busy
6nny-10	Reserved	6nny-42	ACK/REQ lines bad
6nny-11	Media soft error	6nny-43	ACK did not deassert
6nny-12	Drive not ready	6nny-44	Parity error
6nny-13	Media error	6nny-50	Data pins bad
6nny-14	Drive hardware error	6nny-51	Data line 7 bad
6nny-15	Illegal drive command	6nny-52	MSG, C/D, or I/O lines bad
6nny-16	Media was changed	6nny-53	BSY never went busy
6nny-17	Tape write-protected	6nny-54	BSY stayed busy
6nny-18	No data detected	6nny-60	Controller CONFIG-1 register fault
6nny-21	Drive command aborted	6nny-61	Controller CONFIG-2 register fault
6nny-24	Media hard error	6nny-65	Media not unloaded
6nny-25	Reserved	6nny-90	Fan failure
6nny-30	Controller timed out	6nny-91	Over temperature condition
6nny-31	Unrecoverable error	6nny-92	Side panel not installed
6nny-32	Controller/drive not connected	6nny-99	Autoloader reported tape not loaded properly

n = 5, Hard drive
 = 6, CD-ROM drive
 = 7, Tape drive.

 yy = 00, ID
 = 03, Power check
 = 05, Read
 = 06, SA/Media
 = 08, Controller
 = 23, Random read
 = 28, Media load/unload

A.21 POINTING DEVICE INTERFACE ERROR MESSAGES (8601-xx)

Table A-20.
Pointing Device Interface Error Messages

Message	Probable Cause	Message	Probable Cause
8601-01	Mouse ID fails	8601-07	Right block not selected
8601-02	Left mouse button is inoperative	8601-08	Timeout occurred
8601-03	Left mouse button is stuck closed	8601-09	Mouse loopback test failed
8601-04	Right mouse button is inoperative	8601-10	Pointing device is inoperative
8601-05	Right mouse button is stuck closed	8602-xx	I/F test failed
8601-06	Left block not selected	--	--

A.22 CEMM PRIVILEGED OPS ERROR MESSAGES

Table A-21.
CEMM Privileged Ops Error Messages

Message	Probable Cause	Message	Probable Cause
00	LGDT instruction	04	LL3 instruction
01	LIDT instruction	05	MOV CRx instruction
02	LMSW instruction	06	MOV DRx instruction
03	LL2 instruction	07	MOV TRx instruction

A.23 CEMM EXCEPTION ERROR MESSAGES

Table A-22.
CEMM Exception Error Messages

Message	Probable Cause	Message	Probable Cause
00	Divide	10	Invalid TSS
01	Debug	11	Segment not present
02	NMI or parity	12	Stack full
03	INT 0 (arithmetic overflow)	13	General protection fault
04	INT 3	14	Page fault
05	Array bounds check	16	Coprocessor
06	Invalid opcode	32	Attempt to write to protected area
07	Coprocessor device not available	33	Reserved
08	Double fault	34	Invalid software interrupt
09	Coprocessor segment overrun	--	--

Appendix B

ASCII CHARACTER SET

B.1 INTRODUCTION

This appendix lists, in Table B-1, the 256-character ASCII code set including the decimal and hexadecimal values. All ASCII symbols may be called while in DOS or using standard text-mode editors by using the combination keystroke of holding the **Alt** key and using the Numeric Keypad to enter the decimal value of the symbol. The extended ASCII characters (decimals 128-255) can only be called using the **Alt** + Numeric Keypad keys.

NOTE: Regarding keystrokes, refer to notes at the end of the table. Applications may interpret multiple keystroke accesses differently or ignore them completely.

Table B-1.
ASCII Character Set

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
0	00	Blank	32	20	Space	64	40	@	96	60	`
1	01	☺	33	21	!	65	41	A	97	61	a
2	02	☹	34	22	"	66	42	B	98	62	b
3	03	♥	35	23	#	67	43	C	99	63	c
4	04	♦	36	24	\$	68	44	D	100	64	d
5	05	♣	37	25	%	69	45	E	101	65	e
6	06	♠	38	26	&	70	46	F	102	66	f
7	07	●	39	27	'	71	47	G	103	67	g
8	08	○	40	28	(72	48	H	104	68	h
9	09	○	41	29)	73	49	I	105	69	i
10	0A	○	42	2A	*	74	4A	J	106	6A	j
11	0B	○	43	2B	+	75	4B	K	107	6B	k
12	0C	○	44	2C	,	76	4C	L	108	6C	l
13	0D	↵	45	2D	-	77	4D	M	109	6D	m
14	0E	☼	46	2E	.	78	4E	N	110	6E	n
15	0F	☼	47	2F	/	79	4F	O	111	6F	o
16	10	▶	48	30	0	80	50	P	112	70	p
17	11	◀	49	31	1	81	51	Q	113	71	q
18	12	↕	50	32	2	82	52	R	114	72	r
19	13	!!	51	33	3	83	53	S	115	73	s
20	14	¶	52	34	4	84	54	T	116	74	t
21	15	\$	53	35	5	85	55	U	117	75	u
22	16	↕	54	36	6	86	56	V	118	76	v
23	17	↕	55	37	7	87	57	W	119	77	w
24	18	↕	56	38	8	88	58	X	120	78	x
25	19	↕	57	39	9	89	59	Y	121	79	y
26	1A	↕	58	3A	:	90	5A	Z	122	7A	z
27	1B	↕	59	3B	;	91	5B	[123	7B	{
28	1C	┌	60	3C	<	92	5C	\	124	7C	
29	1D	↕	61	3D	=	93	5D]	125	7D	}
30	1E	▲	62	3E	>	94	5E	^	126	7E	~
31	1F	▼	63	3F	?	95	5F	_	127	7F	△ [1]

Continued

Table B-1. ASCII Code Set (Continued)

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
128	80	Ç	160	A0	á	192	C0	Ł	224	E0	α
129	81	û	161	A1	â	193	C1	ł	225	E1	β
130	82	é	162	A2	ó	194	C2	┐	226	E2	Γ
131	83	â	163	A3	û	195	C3	└	227	E3	Π
132	84	ä	164	A4	ñ	196	C4	┌	228	E4	Σ
133	85	à	165	A5	Ñ	197	C5	├	229	E5	σ
134	86	å	166	A6	ª	198	C6	┤	230	E6	μ
135	87	ç	167	A7	º	199	C7	┘	231	E7	τ
136	88	ê	168	A8	¿	200	C8	└┐	232	E8	ϕ
137	89	ë	169	A9	┐	201	C9	┐┌	233	E9	Θ
138	8A	è	170	AA	┐	202	CA	┐┐	234	EA	Ω
139	8B	ï	171	AB	½	203	CB	┐┐┐	235	EB	ō
140	8C	î	172	AC	¼	204	CC	┐┐┐┐	236	EC	∞
141	8D	ì	173	AD	ı	205	CD	═	237	ED	ϕ
142	8E	Ä	174	AE	«	206	CE	┐┐┐┐┐	238	EE	ε
143	8F	Å	175	AF	»	207	CF	┐┐┐┐┐┐	239	EF	∩
144	90	É	176	B0	░	208	D0	┐┐┐┐┐┐┐	240	F0	≡
145	91	æ	177	B1	▒	209	D1	┐┐┐┐┐┐┐┐	241	F1	±
146	92	Æ	178	B2	▓	210	D2	┐┐┐┐┐┐┐┐┐	242	F2	√
147	93	ô	179	B3	┐	211	D3	┐┐┐┐┐┐┐┐┐┐	243	F3	∨
148	94	ö	180	B4	┐┐	212	D4	┐┐┐┐┐┐┐┐┐┐┐	244	F4	┐
149	95	ò	181	B5	┐┐┐	213	D5	┐┐┐┐┐┐┐┐┐┐┐┐	245	F5	┐
150	96	û	182	B6	┐┐┐┐	214	D6	┐┐┐┐┐┐┐┐┐┐┐┐┐	246	F6	┐
151	97	ù	183	B7	┐┐┐┐┐	215	D7	┐┐┐┐┐┐┐┐┐┐┐┐┐┐	247	F7	≈
152	98	ÿ	184	B8	┐┐┐┐┐┐	216	D8	┐┐┐┐┐┐┐┐┐┐┐┐┐┐┐	248	F8	°
153	99	Û	185	B9	┐┐┐┐┐┐┐	217	D9	┐┐┐┐┐┐┐┐┐┐┐┐┐┐┐┐	249	F9	•
154	9A	Ü	186	BA	┐┐┐┐┐┐┐┐	218	DA	┐┐┐┐┐┐┐┐┐┐┐┐┐┐┐┐┐	250	FA	•
155	9B	ç	187	BB	┐┐┐┐┐┐┐┐┐	219	DB	▀	251	FB	√
156	9C	£	188	BC	┐┐┐┐┐┐┐┐┐┐	220	DC	▀	252	FC	²
157	9D	¥	189	BD	┐┐┐┐┐┐┐┐┐┐┐	221	DD	▀	253	FD	²
158	9E	₣	190	BE	┐┐┐┐┐┐┐┐┐┐┐┐	222	DE	▀	254	FE	■
159	9F	ƒ	191	BF	┐	223	DF	▀	255	FF	Blank

NOTES:

[1] Symbol not displayed.

Keystroke Guide:

Dec #	Keystroke(s)
0	Ctrl 2
1-26	Ctrl A thru Z respectively
27	Ctrl [
28	Ctrl
29	Ctrl]
30	Ctrl 6
31	Ctrl -
32	Space Bar
33-43	Shift and key w/corresponding symbol
44-47	Key w/corresponding symbol
48-57	Key w/corresponding symbol, numerical keypad w/Num Lock active
58	Shift and key w/corresponding symbol
59	Key w/corresponding symbol
60	Shift and key w/corresponding symbol
61	Key w/corresponding symbol
62-64	Shift and key w/corresponding symbol
65-90	Shift and key w/corresponding symbol or key w/corresponding symbol and Caps Lock active
91-93	Key w/corresponding symbol
94, 95	Shift and key w/corresponding symbol
96	Key w/corresponding symbol
97-126	Key w/corresponding symbol or Shift and key w/corresponding symbol and Caps Lock active
127	Ctrl -
128-255	Alt and decimal digit(s) of desired character

Appendix C

KEYBOARD

C.1 INTRODUCTION

This appendix describes the Compaq keyboard that is included as standard with the system unit. The keyboard complies with the industry-standard classification of an “enhanced keyboard” and includes a separate cursor control key cluster, twelve “function” keys, and enhanced programmability for additional functions.

This appendix covers the following keyboard types:

- ◆ Standard enhanced keyboard.
- ◆ Space-Saver Windows-version keyboard featuring three additional keys for specific support of the Windows operating system.

Only one type of keyboard is supplied with each system. Other types may be available as an option.

NOTE: This appendix discusses only the keyboard unit. The keyboard interface is a function of the system unit and is discussed in Chapter 5, Input/Output Interfaces.

Topics covered in this appendix include the following:

- ◆ Keystroke processing (C.2) page C-2

C.2 KEYSTROKE PROCESSING

A functional block diagram of the keystroke processing elements is shown in Figure C-1. Power (+5 VDC) is obtained from the system through the PS/2-type interface. The keyboard uses a Z86C14 (or equivalent) microprocessor. The Z86C14 scans the key matrix drivers every 10 ms for pressed keys while at the same time monitoring communications with the keyboard interface of the system unit. When a key is pressed, a Make code is generated. A Break code is generated when the key is released. The Make and Break codes are collectively referred to as scan codes. All keys generate Make and Break codes with the exception of the Pause key, which generates a Make code only.

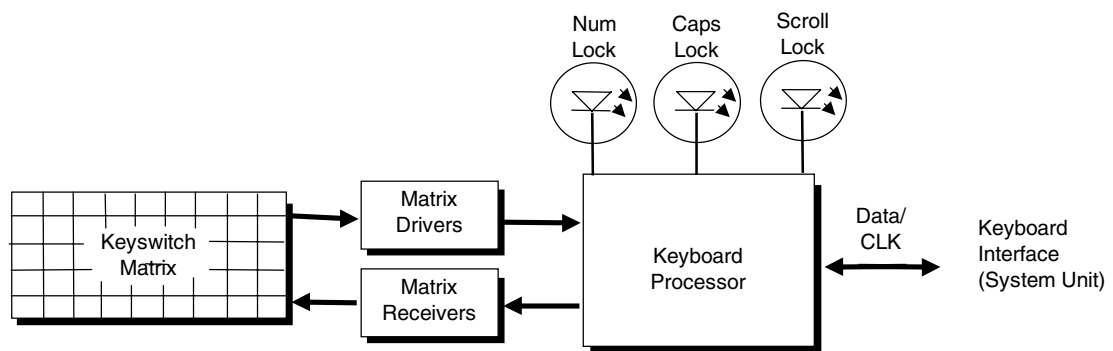


Figure C-1. Keystroke Processing Elements, Block Diagram

When the system is turned on, the keyboard processor generates a Power-On Reset (POR) signal after a period of 150 ms to 2 seconds. The keyboard undergoes a Basic Assurance Test (BAT) that checks for shorted keys and basic operation of the keyboard processor. The BAT takes from 300 to 500 ms to complete.

If the keyboard fails the BAT, an error code is sent to the CPU and the keyboard is disabled until an input command is received. After successful completion of the POR and BAT, a completion code (AAh) is sent to the CPU and the scanning process begins.

The keyboard processor includes a 16-byte FIFO buffer for holding scan codes until the system is ready to receive them. Response and typematic codes are not buffered. If the buffer is full (16 bytes held) a 17th byte of a successive scan code results in an overrun condition and the overrun code replaces the scan code byte and any additional scan code data (and the respective key strokes) are lost. Multi-byte sequences must fit entirely into the buffer before the respective keystroke can be registered.

C.2.1 TRANSMISSIONS TO THE SYSTEM

The keyboard processor sends two main types of data to the system; commands (or responses to system commands) and keystroke scan codes. Before the keyboard sends data to the system (specifically, to the 8042-type logic within the system), the keyboard verifies the clock and data lines to the system. If the clock signal is low (0), the keyboard recognizes the inhibited state and loads the data into a buffer. Once the inhibited state is removed, the data is sent to the system. Keyboard-to-system transfers consist of 11 bits as shown in Figure C-2.

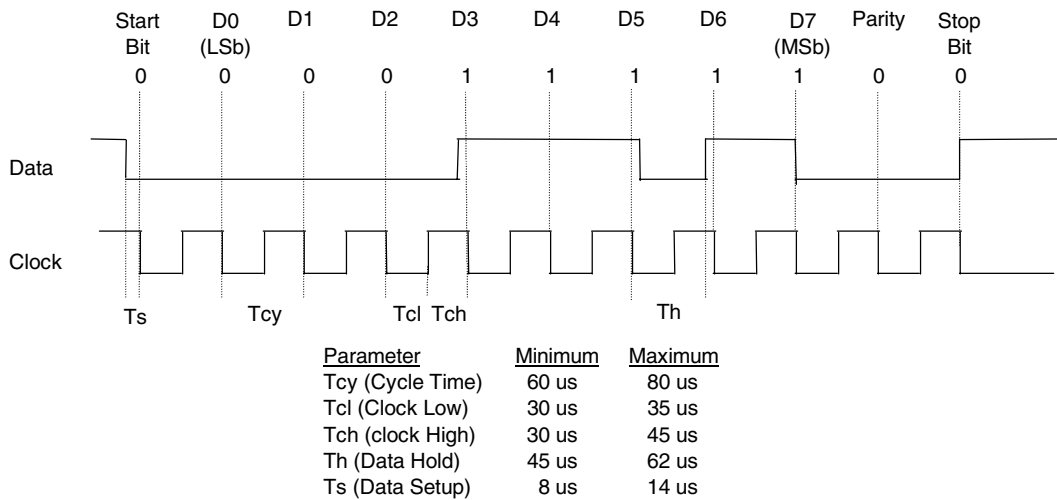


Figure C-2. Keyboard-To-System Transmission of Code 58h, Timing Diagram

The system can halt keyboard transmission by setting the clock signal low. The keyboard checks the clock line every 60 us to verify the signal state. If a low is detected, the keyboard will finish the current transmission if the rising edge of the clock pulse for the parity bit has not occurred.

The enhanced keyboard has three operating modes:

- ◆ Mode 1 - PC-XT compatible
- ◆ Mode 2 - PC-AT compatible (default)
- ◆ Mode 3 - Select mode (keys are programmable as to make-only, break-only, typematic)

Modes can be selected by the user or set by the system. Mode 2 is the default mode. Each mode produces a different set of scan codes. When a key is pressed, the keyboard processor sends that key's make code to the 8042 logic of the system unit. When the key is released, a release code is transmitted as well (except for the Pause key, which produces only a make code). The 8042-type logic of the system unit responds to scan code reception by asserting IRQ1, which is processed by the interrupt logic and serviced by the CPU with an interrupt service routine. The service routine takes the appropriate action based on which key was pressed.

C.2.2 KEYBOARD LAYOUTS

C.2.2.1 Standard Enhanced Keyboards

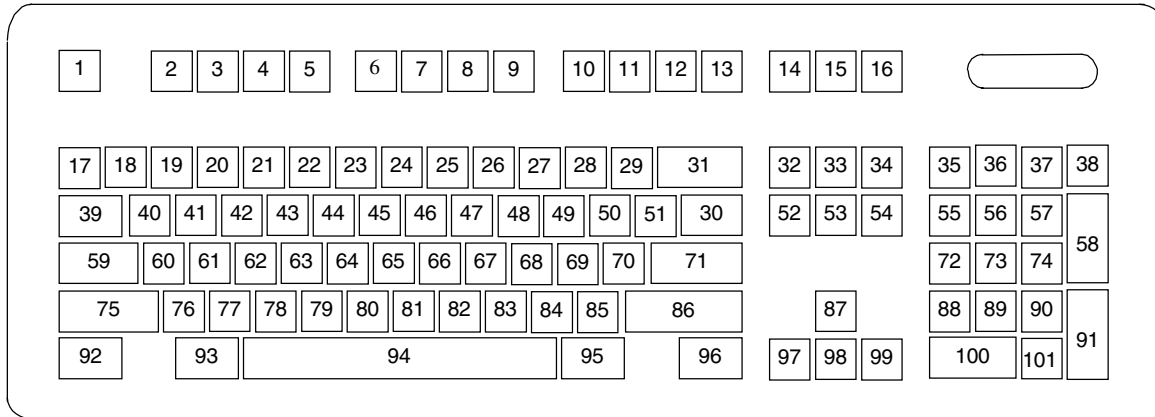


Figure C-3. U.S. English (101-Key) Keyboard Key Positions

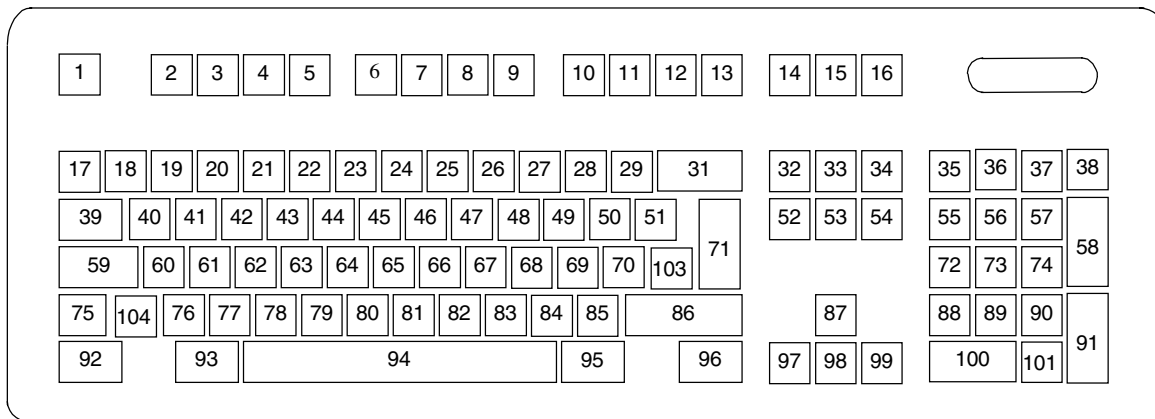


Figure C-4. National (102-Key) Keyboard Key Positions

C.2.2.2 Windows Enhanced Keyboards

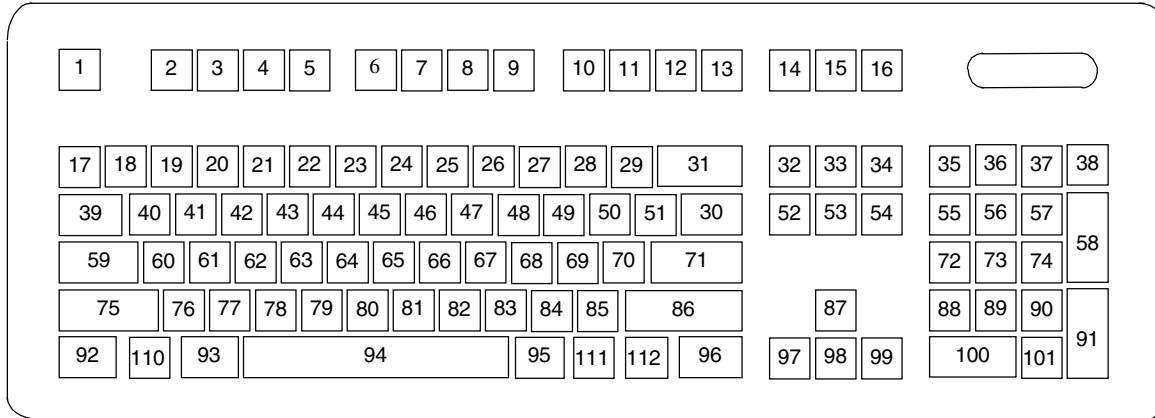


Figure C-5. U.S. English Windows (101W-Key) Keyboard Key Positions

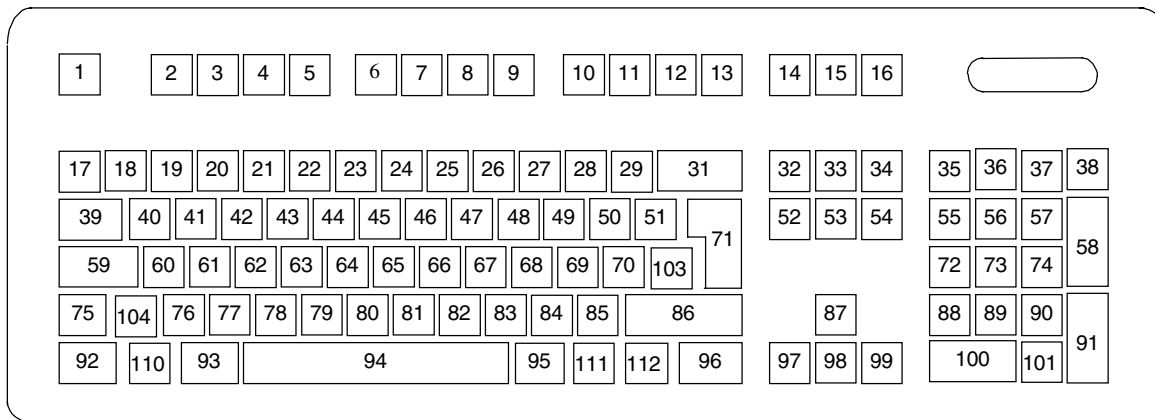


Figure C-6. National Windows (102W-Key) Keyboard Key Positions

C.2.3 KEYS

All keys generate a make code (when pressed) and a break code (when released) with the exception of the **Pause** key (pos. 16), which produces a make code only. All keys, again, with the exception of the **Pause** key, are also typematic, although the typematic action of the **Shift**, **Ctrl**, **Alt**, **Num Lock**, **Scroll Lock**, **Caps Lock**, and **Ins** keys is suppressed by the BIOS. Typematic keys, when held down, send the make code repetitively at a predetermined rate until the key is released. If two keys are held down, the last key pressed will be typematic.

C.2.3.1 Special Single-Keystroke Functions

The following keys provide the intended function in most applications and environments.

Caps Lock - The **Caps Lock** key (pos. 59), when pressed and released, invokes a BIOS routine that turns on the caps lock LED and shifts into upper case key positions 40-49, 60-68, and 76-82. When pressed and released again, these keys revert to the lower case state and the LED is turned off. Use of the **Shift** key will reverse which state these keys are in based on the **Caps Lock** key.

Num Lock - The **Num Lock** key (pos. 32), when pressed and released, invokes a BIOS routine that turns on the num lock LED and shifts into upper case key positions 55-57, 72-74, 88-90, 100, and 101. When pressed and released again, these keys revert to the lower case state and the LED is turned off.

The following keys provide special functions that require specific support by the application.

Print Scrn - The **Print Scrn** (pos. 14) key can, when pressed, generate an interrupt that initiates a print routine. This function may be inhibited by the application.

Scroll Lock - The **Scroll Lock** key (pos. 15) when pressed and released, , invokes a BIOS routine that turns on the scroll lock LED and inhibits movement of the cursor. When pressed and released again, the LED is turned off and the function is removed. This keystroke is always serviced by the BIOS (as indicated by the LED) but may be inhibited or ignored by the application.

Pause - The **Pause** (pos. 16) key, when pressed, can be used to cause the keyboard interrupt to loop, i.e., wait for another key to be pressed. This can be used to momentarily suspend an operation. The key that is pressed to resume operation is discarded. This function may be ignored by the application.

The **Esc**, **Fn** (function), **Insert**, **Home**, **Page Up/Down**, **Delete**, and **End** keys operate at the discretion of the application software.

C.2.3.2 Multi-Keystroke Functions

Shift - The **Shift** key (pos. 75/86), when held down, produces a shift state (upper case) for keys in positions 17-29, 30, 39-51, 60-70, and 76-85 as long as the **Caps Lock** key (pos. 59) is toggled off. If the **Caps Lock** key is toggled on, then a held **Shift** key produces the lower (normal) case for the identified pressed keys. The **Shift** key also reverses the **Num Lock** state of key positions 55-57, 72, 74, 88-90, 100, and 101.


Ctrl - The **Ctrl** keys (pos. 92/96) can be used in conjunction with keys in positions 1-13, 16, 17-34, 39-54, 60-71, and 76-84. The application determines the actual function. Both **Ctrl** key positions provide identical functionality. The pressed combination of **Ctrl** and **Break** (pos. 16) results in the generation of BIOS function INT 1Bh. This software interrupt provides a method of exiting an application and generally halts execution of the current program.

Alt - The **Alt** keys (pos. 93/95) can be used in conjunction with the same keys available for use with the **Ctrl** keys with the exception that position 14 (**SysRq**) is available instead of position 16 (**Break**). The **Alt** key can also be used in conjunction with the numeric keypad keys (pos. 55-57, 72-74, and 88-90) to enter the decimal value of an ASCII character code from 1-255. The application determines the actual function of the keystrokes. Both **Alt** key positions provide identical functionality.

The combination keystroke of **Alt** and **SysRq** results in software interrupt 15h, AX=8500h being executed. It is up to the application to use or not use this BIOS function.


The **Ctrl** and **Alt** keys can be used together in conjunction with keys in positions 1-13, 17-34, 39-54, 60-71, and 76-84. The **Ctrl** and **Alt** key positions used and the sequence in which they are pressed make no difference as long as they are held down at the time the third key is pressed. The **Ctrl**, **Alt**, and **Delete** keystroke combination (required twice if in the Windows environment) initiates a system reset (warm boot) that is handled by the BIOS.

C.2.3.3 Windows Keystrokes

Windows-enhanced keyboards include three additional key positions. Key positions 110 and 111 (marked with the Windows logo ) have the same functionality and are used by themselves or in combination with other keys to perform specific “hot-key” type functions for the Windows operating system. The defined functions of the Windows logo keys are listed as follows:

<u>Keystroke</u>	<u>Function</u>
Window Logo	Open Start menu
Window Logo + F1	Display pop-up menu for the selected object
Window Logo + TAB	Activate next task bar button
Window Logo + E	Explore my computer
Window Logo + F	Find document
Window Logo + CTRL + F	Find computer
Window Logo + M	Minimize all
Shift + Window Logo + M	Undo minimize all
Window Logo + R	Display Run dialog box
Window Logo + PAUSE	Perform system function
Window Logo + 1-0	Reserved for OEM use (see following text)

The combination keystroke of the Window Logo + 1-0 keys are reserved for OEM use for auxiliary functions (speaker volume, monitor brightness, password, etc.).

Key position 112 (marked with an application window icon ) is used in combination with other keys for invoking Windows application functions.

C.2.4 KEYBOARD COMMANDS

Table C-1 lists the commands that the keyboard can send to the system (specifically, to the 8042-type logic).

Table C-1.
Keyboard-to-System Commands

Command	Value	Description
Key Detection Error/Over/run	00h [1] FFh [2]	Indicates to the system that a switch closure couldn't be identified.
BAT Completion	AAh	Indicates to the system that the BAT has been successful.
BAT Failure	FCh	Indicates failure of the BAT by the keyboard.
Echo	EEh	Indicates that the Echo command was received by the keyboard.
Acknowledge (ACK)	FAh	Issued by the keyboard as a response to valid system inputs (except the Echo and Resend commands).
Resend	FEh	Issued by the keyboard following an invalid input.
Keyboard ID	83ABh	Upon receipt of the Read ID command from the system, the keyboard issues the ACK command followed by the two IDS bytes.

Note:

[1] Modes 2 and 3.

[2] Mode 1 only.

C.2.5 SCAN CODES

The scan codes generated by the keyboard processor are determined by the mode the keyboard is operating in.

- ◆ **Mode 1:** In Mode 1 operation, the keyboard generates scan codes compatible with 8088-/8086-based systems. To enter Mode 1, the scan code translation function of the keyboard controller must be disabled. Since translation is not performed, the scan codes generated in Mode 1 are identical to the codes required by BIOS. Mode 1 is initiated by sending command F0h with the 01h option byte. Applications can obtain system codes and status information by using BIOS function INT 16h with AH=00h, 01h, and 02h.
- ◆ **Mode 2:** Mode 2 is the default mode for keyboard operation. In this mode, the 8042 logic translates the make codes from the keyboard processor into the codes required by the BIOS. This mode was made necessary with the development of the Enhanced III keyboard, which includes additional functions over earlier standard keyboards. Applications should use BIOS function INT 16h, with AH=10h, 11h, and 12h for obtaining codes and status data. In Mode 2, the keyboard generates the Break code, a two-byte sequence that consists of a Make code immediately preceded by F0h (i.e., Break code for 0Eh is "F0h 0Eh").
- ◆ **Mode 3:** Mode 3 generates a different scan code set from Modes 1 and 2. Code translation must be disabled since translation for this mode cannot be done.

Table C-2.
Keyboard Scan Codes

Key Pos.	Legend	Make / Break Codes (Hex)		
		Mode 1	Mode 2	Mode 3
1	Esc	01/81	76/F0 76	08/na
2	F1	3B/BB	05/F0 05	07/na
3	F2	3C/BC	06/F0 06	0F/na
4	F3	3D/BD	04/F0 04	17/na
5	F4	3E/BE	0C/F0 0C	1F/na
6	F5	3F/BF	03/F0 03	27/na
7	F6	40/C0	0B/F0 0B	2F/na
8	F7	41/C1	83/F0 83	37/na
9	F8	42/C2	0A/F0 0A	3F/na
10	F9	43/C3	01/F0 01	47/na
11	F10	44/C4	09/F0 09	4F/na
12	F11	57/D7	78/F0 78	56/na
13	F12	58/D8	07/F0 07	5E/na
14	Print Scrn	E0 2A E0 37/E0 B7 E0 AA E0 37/E0 B7 [1] [2] 54/84 [3]	E0 2A E0 7C/E0 F0 7C E0 F0 12 E0 7C/E0 F0 7C [1] [2] 84/F0 84 [3]	57/na
15	Scroll Lock	46/C6	7E/F0 7E	5F/na
16	Pause	E1 1D 45 E1 9D C5/na E0 46 E0 C6/na [3]	E1 14 77 E1 F0 14 F0 77/na E0 7E E0 F0 7E/na [3]	62/na
17	`	29/A9	0E/F0 E0	0E/F0 0E
18	1	02/82	16/F0 16	46/F0 46
19	2	03/83	1E/F0 1E	1E/F0 1E
20	3	04/84	26/F0 26	26/F0 26
21	4	05/85	25/F0 25	25/F0 25
22	5	06/86	2E/F0 2E	2E/F0 2E
23	6	07/87	36/F0 36	36/F0 36
24	7	08/88	3D/F0 3D	3D/F0 3D
25	8	09/89	3E/F0 3E	3E/F0 3E
26	9	0A/8A	46/F0 46	46/F0 46
27	0	0B/8B	45/F0 45	45/F0 45
28	-	0C/8C	4E/F0 4E	4E/F0 4E
29	=	0D/8D	55/F0 55	55/F0 55
30	\	2B/AB	5D/F0 5D	5C/F0 5C
31	Backspace	0E/8E	66/F0 66	66/F0 66
32	Insert	E0 52/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 52/E0 D2 E0 AA [6]	E0 70/E0 F0 70 E0 F0 12 E0 70/E0 F0 70 E0 12 [5] E0 12 E0 70/E0 F0 70 E0 F0 12 [6]	67/na
33	Home	E0 47/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 47/E0 C7 E0 AA [6]	E0 6C/E0 F0 6C E0 F0 12 E0 6C/E0 F0 6C E0 12 [5] E0 12 E0 6C/E0 F0 6C E0 F0 12 [6]	6E/na
34	Page Up	E0 49/E0 C7 E0 AA E0 49/E0 C9 E0 2A [4] E0 2A E0 49/E0 C9 E0 AA [6]	E0 7D/E0 F0 7D E0 F0 12 E0 7D/E0 F0 7D E0 12 [5] E0 12 E0 7D/E0 F0 7D E0 F0 12 [6]	6F/na
35	Num Lock	45/C5	77/F0 77	76/na
36	/	E0 35/E0 B5 E0 AA E0 35/E0 B5 E0 2A [1]	E0 4A/E0 F0 4A E0 F0 12 E0 4A/E0 F0 4A E0 12 [1]	77/na
37	*	37/B7	7C/F0 7C	7E/na
38	-	4A/CA	7B/F0 7B	84/na
39	Tab	0F/8F	0D/F0 0D	0D/na
40	Q	10/90	15/F0 15	15/na

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes (Continued)

Key Pos	Legend	Make / Break Codes (Hex)		
		Mode 1	Mode 2	Mode 3
41	W	11/91	1D/F0 1D	1D/F0 1D
42	E	12/92	24/F0 24	24/F0 24
43	R	13/93	2D/F0 2D	2D/F0 2D
44	T	14/94	2C/F0 2C	2C/F0 2C
45	Y	15/95	35/F0 35	35/F0 35
46	U	16/96	3C/F0 3C	3C/F0 3C
47	I	17/97	43/F0 43	43/F0 43
48	O	18/98	44/F0 44	44/F0 44
49	P	19/99	4D/F0 4D	4D/F0 4D
50	[1A/9A	54/F0 54	54/F0 54
51]	1B/9B	5B/F0 5B	5B/F0 5B
52	Delete	E0 53/E0 D3 E0 AA E0 53/E0 D3 E0 2A [4] E0 2A E0 53/E0 D3 E0 AA [6]	E0 71/E0 F0 71 E0 F0 12 E0 71/E0 F0 71 E0 12 [5] E0 12 E0 71/E0 F0 71 E0 F0 12 [6]	64/F0 64
53	End	E0 4F/E0 CF E0 AA E0 4F/E0 CF E0 2A [4] E0 2A E0 4F/E0 CF E0 AA [6]	E0 69/E0 F0 69 E0 F0 12 E0 69/E0 F0 69 E0 12 [5] E0 12 E0 69/E0 F0 69 E0 F0 12 [6]	65/F0 65
54	Page Down	E0 51/E0 D1 E0 AA E0 51/E0 D1 E0 2A [4] E0 @a E0 51/E0 D1 E0 AA [6]	E0 7A/E0 F0 7A E0 F0 12 E0 7A/E0 F0 7A E0 12 [5] E0 12 E0 7A/E0 F0 7A E0 F0 12 [6]	6D/F0 6D
55	7	47/C7 [6]	6C/F0 6C [6]	6C/na [6]
56	8	48/C8 [6]	75/F0 75 [6]	75/na [6]
57	9	49/C9 [6]	7D/F0 7D [6]	7D/na [6]
58	+	4E/CE [6]	79/F0 79 [6]	7C/F0 7C
59	Caps Lock	3A/BA	58/F0 58	14/F0 14
60	A	1E/9E	1C/F0 1C	1C/F0 1C
61	S	1F/9F	1B/F0 1B	1B/F0 1B
62	D	20/A0	23/F0 23	23/F0 23
63	F	21/A1	2B/F0 2B	2B/F0 2B
64	G	22/A2	34/F0 34	34/F0 34
65	H	23/A3	33/F0 33	33/F0 33
66	J	24/A4	3B/F0 3B	3B/F0 3B
67	K	25/A5	42/F0 42	42/F0 42
68	L	26/A6	4B/F0 4B	4B/F0 4B
69	;	27/A7	4C/F0 4C	4C/F0 4C
70	'	28/A8	52/F0 52	52/F0 52
71	Enter	1C/9C	5A/F0 5A	5A/F0 5A
72	4	4B/CB [6]	6B/F0 6B [6]	6B/na [6]
73	5	4C/CC [6]	73/F0 73 [6]	73/na [6]
74	6	4D/CD [6]	74/F0 74 [6]	74/na [6]
75	Shift (left)	2A/AA	12/F0 12	12/F0 12
76	Z	2C/AC	1A/F0 1A	1A/F0 1A
77	X	2D/AD	22/F0 22	22/F0 22
78	C	2E/AE	21/F0 21	21/F0 21
79	V	2F/AF	2A/F0 2A	2A/F0 2A
80	B	30/B0	32/F0 32	32/F0 32

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes (Continued)

Key Pos.	Legend	Make / Break Codes (Hex)		
		Mode 1	Mode 2	Mode 3
81	N	31/B1	31/F0 31	31/F0 31
82	M	32/B2	3A/F0 3A	3A/F0 3A
83	,	33/B3	41/F0 41	41/F0 41
84	.	34/B4	49/F0 49	49/F0 49
85	/	35/B5	4A/F0 4A	4A/F0 4A
86	Shift (right)	36/B6	59/F0 59	59/F0 59
87	▲	E0 48/E0 C8 E0 AA E0 48/E0 C8 E0 2A [4] E0 2A E0 48/E0 C8 E0 AA [6]	E0 75/E0 F0 75 E0 F0 12 E0 75/E0 F0 75 E0 12 [5] E0 12 E0 75/E0 F0 75 E0 F0 12 [6]	63/F0 63
88	1	4F/CF [6]	69/F0 69 [6]	69/na [6]
89	2	50/D0 [6]	72/F0 72 [6]	72/na [6]
90	3	51/D1 [6]	7A/F0 7A [6]	7A/na [6]
91	Enter	E0 1C/E0 9C	E0 5A/F0 E0 5A	79/F0 79[6]
92	Ctrl (left)	1D/9D	14/F0 14	11/F0 11
93	Alt (left)	38/B8	11/F0 11	19/F0 19
94	(Space)	39/B9	29/F0 29	29/F0 29
95	Alt (right)	E0 38/E0 B8	E0 11/F0 E0 11	39/na
96	Ctrl (right)	E0 1D/E0 9D	E0 14/F0 E0 14	58/na
97	◀	E0 4B/E0 CB E0 AA E0 4B/E0 CB E0 2A [4] E0 2A E0 4B/E0 CB E0 AA [6]	E0 6B/E0 F0 6B E0 F0 12 E0 6B/E0 F0 6B E0 12[5] E0 12 E0 6B/E0 F0 6B E0 F0 12[6]	61/F0 61
98	▼	E0 50/E0 D0 E0 AA E0 50/E0 D0 E0 2A [4] E0 2A E0 50/E0 D0 E0 AA [6]	E0 72/E0 F0 72 E0 F0 12 E0 72/E0 F0 72 E0 12[5] E0 12 E0 72/E0 F0 72 E0 F0 12[6]	60/F0 60
99	▶	E0 4D/E0 CD E0 AA E0 4D/E0 CD E0 2A [4] E0 2A E0 4D/E0 CD E0 AA [6]	E0 74/E0 F0 74 E0 F0 12 E0 74/E0 F0 74 E0 12[5] E0 12 E0 74/E0 F0 74 E0 F0 12[6]	6A/F0 6A
100	0	52/D2 [6]	70/F0 70 [6]	70/na [6]
101	.	53/D3 [6]	71/F0 71 [6]	71/na [6]
102	na	7E/FE	6D/F0 6D	7B/F0 7B
103	na	2B/AB	5D/F0 5D	53/F0 53
104	na	36/D6	61/F0 61	13/F0 13
110	(Win95) [7]	E0 5B/E0 DB E0 AA E0 5B/E0 DB E0 2A [4] E0 2A E0 5B/E0 DB E0 AA [6]	E0 1F/E0 F0 1F E0 F0 12 E0 1F/E0 F0 1F E0 12 [5] E0 12 E0 1F/E0 F0 1F E0 F0 12 [6]	8B/F0 8B
111	(Win95) [7]	E0 5C/E0 DC E0 AA E0 5C/E0 DC E0 2A [4] E0 2A E0 5C/E0 DC E0 AA [6]	E0 2F/E0 F0 27 E0 F0 12 E0 27/E0 F0 27 E0 12 [5] E0 12 E0 27/E0 F0 27 E0 F0 12 [6]	8C/F0 8C
112	(Win Apps) [7]	E0 5D/E0 DD E0 AA E0 5D/E0 DD E0 2A [4] E0 2A E0 5D E0 DD E0 AA [6]	E0 2F/E0 F0 2F E0 F0 12 E0 2F/E0 F0 2F E0 12 [5] E0 12 E0 2F/E0 F0 2F E0 F0 12 [6]	8D/F0 8D

NOTES:

All codes assume Shift, Ctrl, and Alt keys inactive unless otherwise noted.

NA = Not applicable

[1] Shift (left) key active.

[2] Ctrl key active.

[3] Alt key active.

[4] Left Shift key active. For active right Shift key, substitute AA/2A make/break codes for B6/36 codes.

[5] Left Shift key active. For active right Shift key, substitute F0 12/12 make/break codes for F0 59/59 codes.

[6] Num Lock key active.

[7] Windows keyboards only

Appendix D

MATROX MILLENNIUM G400

AGP GRAPHICS CARD / G400 DVI Card

D.1 INTRODUCTION

This appendix describes Matrox Millennium G400-SD Graphics Card used in some models and available as an option. This card (layout shown in the following figure) installs in a system's AGP slot. The Matrox Millennium G400 graphics card provides high 2D performance as well as 3D capabilities. With the optional Matrox G400 DVI daughter card installed, a digital flat panel can be used for even higher quality imaging.

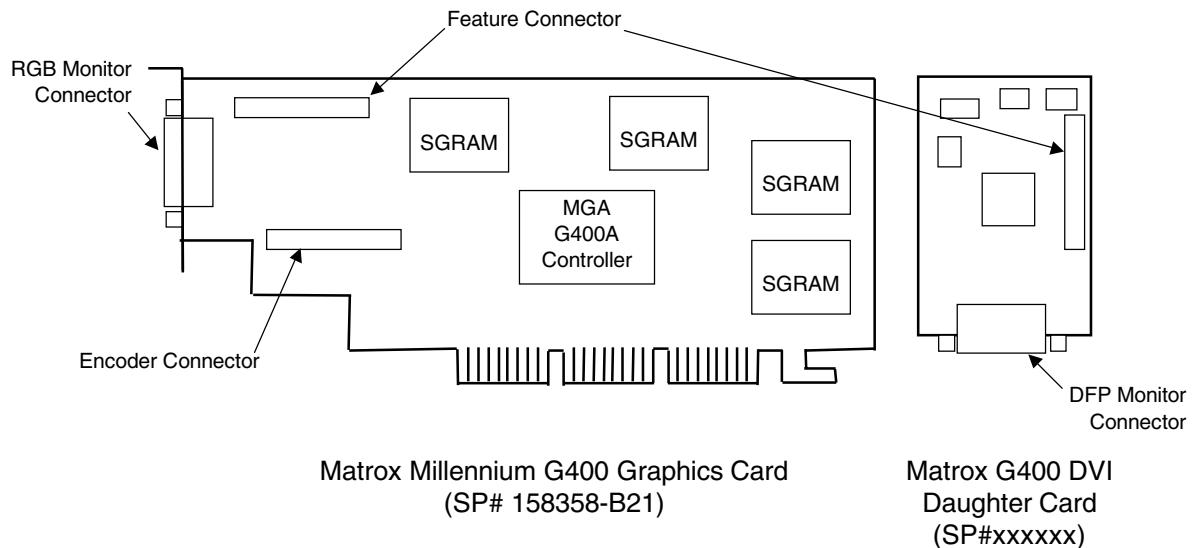


Figure D-1. Matrox Millennium G400 Graphics Card and G400 DVI Card Layouts

This appendix covers the following subjects:

- ◆ Functional description (D.2) page D-2
- ◆ Display modes (D.3) page D-3
- ◆ Software support information (D.4) page D-4
- ◆ Monitor power management (D.5) page D-4
- ◆ Connectors (D.6) page D-5

D.2 FUNCTIONAL DESCRIPTION

The Matrox Millennium G400-SD Graphics Card provides high performance 2D and 3D display imaging. The card's AGP design provides an economical approach to 3D processing by off-loading 3D effects such as texturing, z-buffering and alpha blending to the system memory while the on-board SGRAM stores the main display image. This card includes an encoder connector for attaching a video (TV) encoder option and a feature connector for attaching the optional Matrox G400 DVI daughter card that can drive a digital flat panel (DFP) display. By by-passing the RAMDAC and using a digital interface and a DFP, image quality is enhanced and free from degradation sometimes suffered by RGB interfaces.

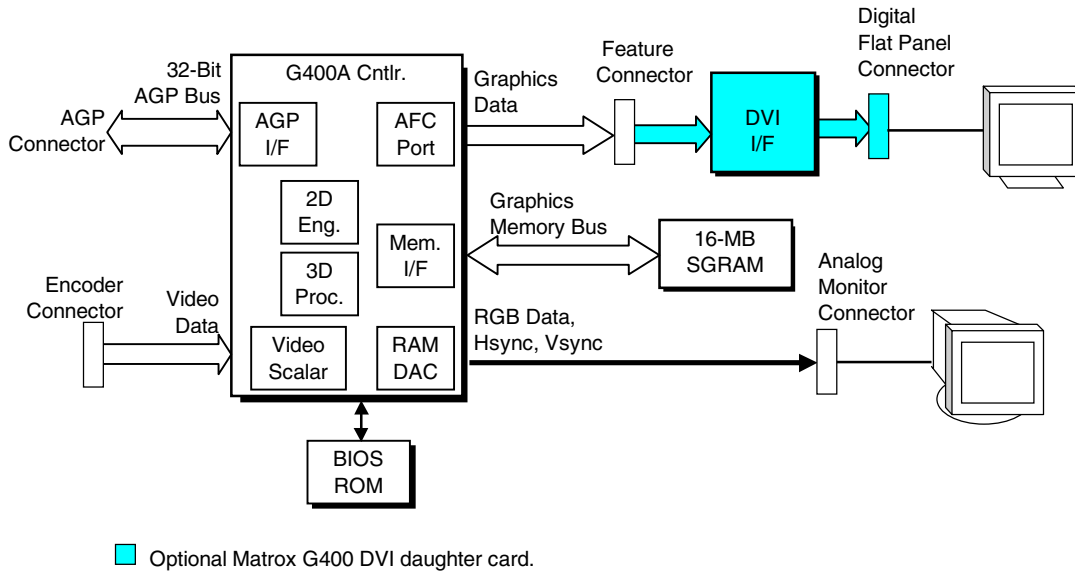


Figure D-2. Matrox Millennium G400 Graphics Card Block diagram

The Matrox Millennium G400-SD Graphics Card includes the following features:

- ◆ 256-bit (dual 128-bit bus) internal processing
- ◆ AGP 4X transfers with sideband addressing
- ◆ 2D drawing engine
- ◆ 3D rendering engine
- ◆ 300-MHz RAMDAC
- ◆ 16 megabytes of SGRAM using 128-bit access
- ◆ Color space conversion
- ◆ Texture mapping
- ◆ Flat and Gouraud shading
- ◆ Specular highlighting
- ◆ Dithering
- ◆ Vertex fogging
- ◆ Environment bump mapping

D.3 DISPLAY MODES

The graphics display modes supported by the Matrox Millennium G400-SD Graphics are listed in Table D-1. To expand display mode support will require memory expansion and may also require a video BIOS upgrade.

Table D-1.
2D Graphics Display Modes

Resolution	Color Depth	Vertical Refresh Freq. [1]	Amount of Memory Used
640 x 480	256	200 Hz	512 KB
640 x 480	65K	200 Hz	1 MB
640 x 480	16.7M	200 Hz	1 MB
800 x 600	256	200 Hz	512 KB
800 x 600	65K	200 Hz	1 MB
800 x 600	16.7M	200 Hz	1.5 MB
1024 x 768	256	160 Hz	1 MB
1024 x 768	65K	160 Hz	1.5 MB
1024 x 768	16.7M	160 Hz	2.5 MB
1152 x 864	256	140 Hz	3 MB
1152 x 864	65K	140 Hz	3.5 MB
1152 x 864	16.7M	140 Hz	4 MB
1280 x 1024	256	120 Hz	1.5 MB
1280 x 1024	65K	120 Hz	2.5 MB
1280 x 1024	16.7M	120 Hz	4 MB
1600 x 1200	256	100 Hz	2 MB
1600 x 1200	65K	100 Hz	4 MB
1600 x 1200	16.7M	100 Hz	8 MB
1800 x 1440	256	80 Hz	3 MB
1800 x 1440	65K	80 Hz	6 MB
1800 x 1440	16.7M	80 Hz	8 MB
1920 x 1080	256	80 Hz	2 MB
1920 x 1080	65K	80 Hz	4 MB
1920 x 1080	16.7	60 Hz	8 MB
1920 x 1440	256	75 Hz	3 MB
1920 x 1440	65K	75 Hz	6 MB
1920 x 1440	16.7M	75 Hz	8 MB
2048 x 1536	356	75 Hz	4 MB
2048 x 1536	65K	75 Hz	8 MB
2048 x 1536	16.7M	75 Hz	12 MB

NOTE:

[1] Drivers may restrict refresh frequency to a maximum of 85 Hz in Windows environment.

The optional Matrox G400 DVI daughter card provides a maximum resolution of 1280 x 1024 @ 24 bpp (16.7 million colors) for a digital flat panel.

D.4 SOFTWARE SUPPORT INFORMATION

The Matrox Millennium G400-SD graphics card is fully compatible with software written for legacy video modes (VGA, EGA, CGA) and needs no driver support for those modes.

Drivers are provided with or available for the card to provide extended mode support for the current operating systems and programming environments such as:

- ◆ Windows 98, 95
- ◆ Windows NT 4.0, 3.51
- ◆ Windows 3.11, 3.1
- ◆ OS/2
- ◆ Quick Draw
- ◆ MS Direct Draw
- ◆ Direct 3D
- ◆ OpenGL

D.5 POWER MANAGEMENT AND CONSUMPTION

This controller provides monitor power control for monitors that conform to the VESA display power management signaling (DPMS) protocol. This protocol defines different power consumption conditions and uses the HSYNC and VSYNC signals to select a monitor's power condition. Table I-2 lists the monitor power conditions.

Table D-2.
Monitor Power Management Conditions

HSYNC	VSYNC	Power Mode	Description
Active	Active	On	Monitor is completely powered up. If activated, the inactivity counter counts down during system inactivity and if allowed to timeout, generates an SMI to initiate the Suspend mode.
Active	Inactive	Suspend	Monitor's high voltage section is turned off and CRT heater (filament) voltage is reduced from 6.6 to 4.4 VDC. The Off mode inactivity timer counts down from the preset value and if allowed to timeout, another SMI is generated and serviced, resulting in the monitor being placed into the Off mode. Wake up from Suspend mode is typically a few seconds.
Inactive	Inactive	Off	Monitor's high voltage section and heater circuitry is turned off. Wake up from Off mode is a little longer than from Suspend.

The graphics card's maximum power consumption on the AGP bus is listed below:

Maximum current @ 3.3 VDC: 3.1 A
Maximum current @ 5.0 VDC: 100 mA
Maximum current @ 1.5 VDC: 50 mA
Maximum power consumption: 10.8 watts

D.6 CONNECTORS

There are three connectors associated with the graphics subsystem; the display/monitor connector, the Feature connector, and the Encoder port.

NOTE: The graphic card's edge connector mates with the AGP connector on the system board. This interface is described in chapter 4 of the product's technical reference guide.

The DB-15 display/monitor connector is provided for connection of a compatible RGB/analog monitor. The Encoder port connector allows the attachment of a video peripheral for displaying motion picture text. The Feature connector allows the attachment of the optional Matrox G400 DVI daughter card, which provides a DVI interface for a compliant digital flat panel display.

D.6.1 MONITOR CONNECTOR

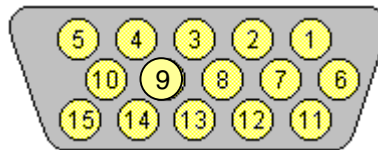


Figure D-3. VGA Monitor Connector, (Female DB-15, as viewed from rear).

Table D-3.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	PWR	+5 VDC (fused) [1]
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	NC	Not Connected
4	NC	Not Connected	12	SDA	DDC2-B Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSynC	Vertical Sync
7	G GND	Green Analog Ground	15	SCL	DDC2-B Clock
8	B GND	Blue Analog Ground	--	--	--

NOTES:

[1] Fuse automatically resets when excessive load is removed.

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Appendix E

ELSA SYNERGY II GRAPHICS CARD

E.1 INTRODUCTION

This appendix describes the ELSA Synergy II Graphics Card. The ELSA Synergy II graphics card installs in the AGP slot on the system board and is included in the standard configuration of some models. This card provides high 2D performance and entry-level 3D performance for CAD, DCC, and GIS applications. Multiple-monitor support can be obtained by the installation of additional Synergy II graphics cards (using PCI-bus type cards).

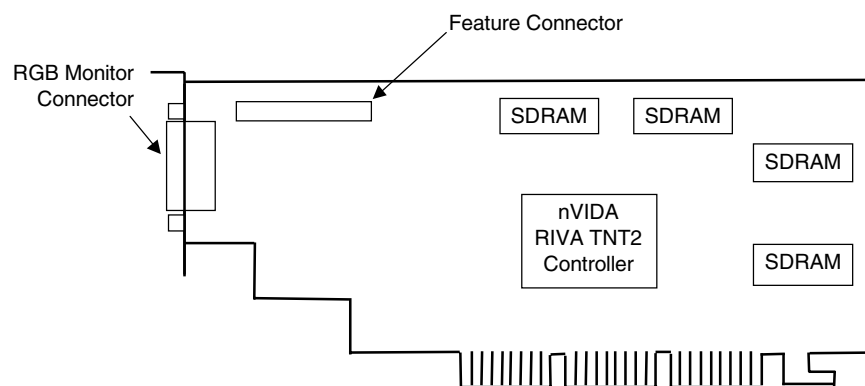


Figure E-1. ELSA Synergy II AGP Graphics Card Layout (Compaq SP# 103382-B21)

This appendix covers the following subjects:

- ◆ Functional description (E.2) page E-2
- ◆ Display configurations (E.3) page E-4
- ◆ Programming (E.4) page E-5
- ◆ Power management (E.5) page E-6
- ◆ Connectors (E.6) page E-7

E.2 FUNCTIONAL DESCRIPTION

The ELSA Synergy II AGP Graphics Card is based on the nVIDIA RIVA TNT2 graphics controller. This card supports 3D effects such as texturing, z-buffering and alpha blending. This card includes 32 megabytes of 143-MHz SDRAM. The graphics BIOS code is contained on-board in flash ROM that is upgradeable..

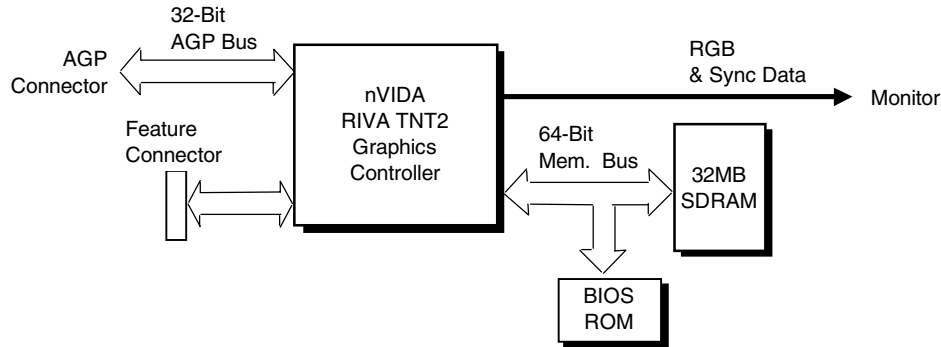


Figure E-2. ELSA Synergy II AGP Graphics Card Block diagram

The ELSA Synergy II AGP Graphics Card includes the following features:

- ◆ AGP 4X interface
- ◆ 128-bit 2D/3D processor
- ◆ 32 megabytes of 143-MHz SDRAM
- ◆ 300 MHz RAMDAC
- ◆ 24-bit double-buffered color planes
- ◆ 8-bit stencil planes
- ◆ 24-bit Z-buffer

Utilizing a variety of software tools, the nVIDIA TNT2 provides powerful 2D/3D processing for demanding graphical environments. Hardware-accelerated MPEG2 decode is supported for DVD at resolutions up to 720 x 480, and HDTV formats (720I-1080I, 720p-1080p) are also supported.

The 300-MHz pixel clock of the RAMDAC operates at full speed for all resolutions. The feature connector allows the addition of a PanelLink adapter for driving a digital flat panel (DFP) for maximum image sharpness.

E.3 DISPLAY CONFIGURATIONS

The graphics modes supported by both the ELSA Synergy II and its video BIOS are listed in Table E-1. All modes utilize double-buffering.

Table E-1.
Graphics Display Modes

Resolution	Color Depth	Vertical Refresh Freq. [1]	Z-Buffer	Texture Memory Size (KB)
640 x 480 @ 8 bpp	256	723 Hz	16-bit	31,568
640 x 480 @ 16 bpp	65K	723 Hz	16-bit	30,968
640 x 480 @ 32 bpp	16.7M	723 Hz	24-bit	29,168
800 x 600 @ 8 bpp	256	463 Hz	16-bit	30,893
800 x 600 @ 16 bpp	65K	463 Hz	16-bit	29,956
800 x 600 @ 32 bpp	16.7M	463 Hz	24-bit	27,143
1024 x 768 @ 8 bpp	256	283 Hz	16-bit	29,696
1024 x 768 @ 16 bpp	65K	283 Hz	16-bit	28,160
1024 x 768 @ 32 bpp	16.7M	283 Hz	24-bit	23,552
1152 x 864 @ 8 bpp	256	223 Hz	16-bit	28,880
1152 x 864 @ 16 bpp	65K	223 Hz	16-bit	26,936
1152 x 864 @ 32 bpp	16.7M	223 Hz	24-bit	21,104
1280 x 1024 @ 8 bpp	256	170 Hz	16-bit	27,648
1280 x 1024 @ 16 bpp	65K	170 Hz	16-bit	25,088
1280 x 1024 @ 32 bpp	16.7M	170 Hz	24-bit	17,408
1536 x 960 @ 8 bpp	256	151 Hz	16-bit	27,008
1536 x 960 @ 16 bpp	65K	151 Hz	16-bit	24,128
1536 x 960 @ 32 bpp	16.7M	151 Hz	24-bit	15,488
1600 x 1000 @ 8 bpp	256	139 Hz	16-bit	26,518
1600 x 1000 @ 16 bpp	65K	139 Hz	16-bit	23,393
1600 x 1000 @ 32 bpp	16.7M	139 Hz	24-bit	14,018
1600 x 1200 @ 8 bpp	256	116 Hz	16-bit	25,268
1600 x 1200 @ 16 bpp	65K	116 Hz	16-bit	21,518
1600 x 1200 @ 32 bpp	16.7M	116 Hz	24-bit	10,268
1600 x 1280 @ 8 bpp	256	109 Hz	16-bit	24,768
1600 x 1280 @ 16 bpp	65K	109 Hz	16-bit	20,768
1600 x 1280 @ 32 bpp	16.7M	109 Hz	24-bit	8,768
1792 x 1120 @ 8 bpp	256	111 Hz	16-bit	24,928
1792 x 1120 @ 16 bpp	65K	111 Hz	16-bit	21,008
1792 x 1120 @ 32 bpp	16.7M	111 Hz	24-bit	9,248
1920 x 1080 @ 8 bpp	256	107 Hz	16-bit	24,668
1920 x 1080 @ 16 bpp	65K	107 Hz	16-bit	20,618
1920 x 1080 @ 32 bpp	16.7M	107 Hz	24-bit	8,468
1920 x 1200 @ 8 bpp	256	96 Hz	16-bit	23,768
1920 x 1200 @ 16 bpp	65K	96 Hz	16-bit	19,268
1920 x 1200 @ 32 bpp	16.7M	96 Hz	24-bit	5,768

NOTE:

[1] Refresh frequency limited to a maximum of 85 Hz in Windows 95/NT environments.

E.4 SOFTWARE SUPPORT

Then ELSA Synergy II graphics controller includes a VGA core that is compatible with software written for the legacy display modes (CGA, EGA, and VGA). Driver and/or application accelerator support is available for the following operating systems and environments:

- ◆ MS Windows 95, 98, NT 3.51/4.0, 2000
- ◆ Autodesk AutoCAD
- ◆ Kinetix 3D Studio MAX
- ◆ 2D GSI
- ◆ OpenGL 1.1/1.2
- ◆ OpenGL extensions for AutoCAD, 3D Viewer for AutoCAD, Discreet MAX
- ◆ DirectX, Direct3D, Direct Draw DX6/DX7, ActiveX
- ◆ Fahrenheit
- ◆ Heidi
- ◆ POWERdraft, ELSAview, MAXtreme
- ◆ Discreet MAX, Discreet Edit, NewTek Lightwave 3D

E.5 POWER CONSUMPTION

The ELSA Synergy II Graphics Card consumes the following amounts of power:

At initialization: 1.7 A
Average load: 2.2 A
Maximum load: 2.6 A

E.6 MONITOR CONTROL

This controller provides monitor power control for monitors that conform to the VESA display power management signaling (DPMS) protocol. This protocol defines different power consumption conditions and uses the HSYNC and VSYNC signals to select a monitor's power condition. Table E-5 lists the monitor power conditions.

Table E-5.
Monitor Power Management Conditions

HSYNC	VSYNC	Power Mode	Description
Active	Active	On	Monitor is completely powered up. If activated, the inactivity counter counts down during system inactivity and if allowed to timeout, generates an SMI to initiate the Suspend mode.
Active	Inactive	Suspend	Monitor's high voltage section is turned off and CRT heater (filament) voltage is reduced from 6.6 to 4.4 VDC. The Off mode inactivity timer counts down from the preset value and if allowed to timeout, another SMI is generated and serviced, resulting in the monitor being placed into the Off mode. Wake up from Suspend mode is typically a few seconds.
Inactive	Inactive	Off	Monitor's high voltage section and heater circuitry is turned off. Wake up from Off mode is a little longer than from Suspend.

E.7 CONNECTORS

The ELSA SYNERGY II graphics card contains two connectors: the monitor (display) connector for attaching a CRT display and a feature connector for attaching peripherals. The monitor connector is illustrated below with the pin-out.

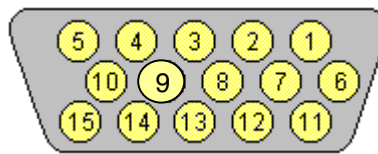


Figure E-3. VGA Monitor Connector, (Female DB-15, as viewed from rear).

Table E-6.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog [1]	9	+5 VDC	+5 volts (fused) [4]
2	G	Blue Analog [1]	10	GND	Ground
3	B	Green Analog [1]	11	Mon. ID	Monitor Identification
4	Mon ID	Monitor Identification	12	SDA	DDC2-B Data [2]
5	GND	Ground	13	HSync	Horizontal Sync [3]
6	R GND	Red Analog Ground	14	VSynC	Vertical Sync [3]
7	G GND	Blue Analog Ground	15	SCL	DDC2-B Clock [2]
8	B GND	Green Analog Ground	--	--	--

NOTES:

- [1] RS343A signal levels:
Full on condition = 0.700 VDC
Rise Fall Time @ max pixel rate = 4 ns
Output impedance = 75 ohms
- [2] TTL signal levels:
Max Rise Time = 100 ns
Max Fall Time = 15 ns
- [3] TTL signal levels:
Max Rise Time = 15 ns
Max Fall Time = 10 ns
- [4] Fuse automatically resets when excessive load is removed.

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Appendix F

3DLABS OXYGEN GVX1 AGP GRAPHICS CARD

F.1 INTRODUCTION

This appendix describes the 3Dlabs Oxygen GVX1 AGP Graphics Card (Figure F-1), which is the standard graphics controller on select workstation models. This card installs in the AGP slot of the system board. This controller represents an optimum price/performance solution for professional 3D environments such as CAD/CAM, DCC, GIS, solids modeling, and visual data analysis applications.

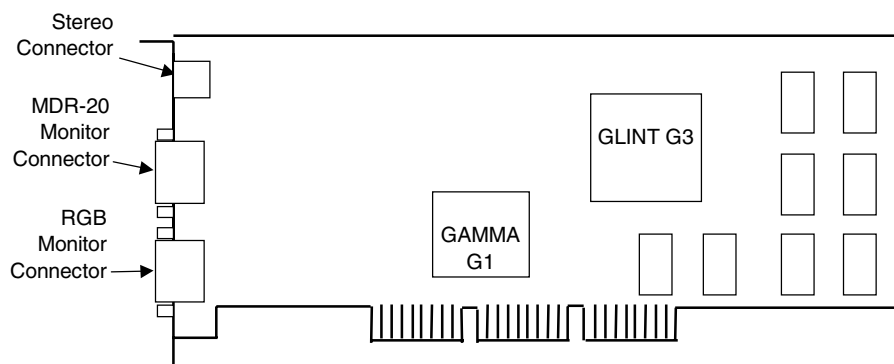


Figure F-1. 3Dlabs Oxygen GVX1 AGP Graphics Card Layout (SP# 136398-B21)

This appendix covers the following subjects:

- ◆ Functional description (F.2) page F-2
- ◆ Display modes (F.3) page F-4
- ◆ Programming (F.4) page F-5
- ◆ Monitor power management (F.5) page F-6
- ◆ Connectors (F.6) page F-6

F.2 FUNCTIONAL DESCRIPTION

The 3Dlabs Oxygen GVX1 graphics card is based on two main components: the GLINT R3 Rasterization Processor and the GLINT Gamma G1 Geometry Processor. The GLINT G3 uses a quality graphics pipeline and display management subsystem that is highly efficient and economical. Memory management is handled directly by the GLINT G3. The GLINT Gamma G1 is a dedicated 3D lighting and geometry component providing a complete OpenGL pipeline reducing the bottleneck found on other systems.

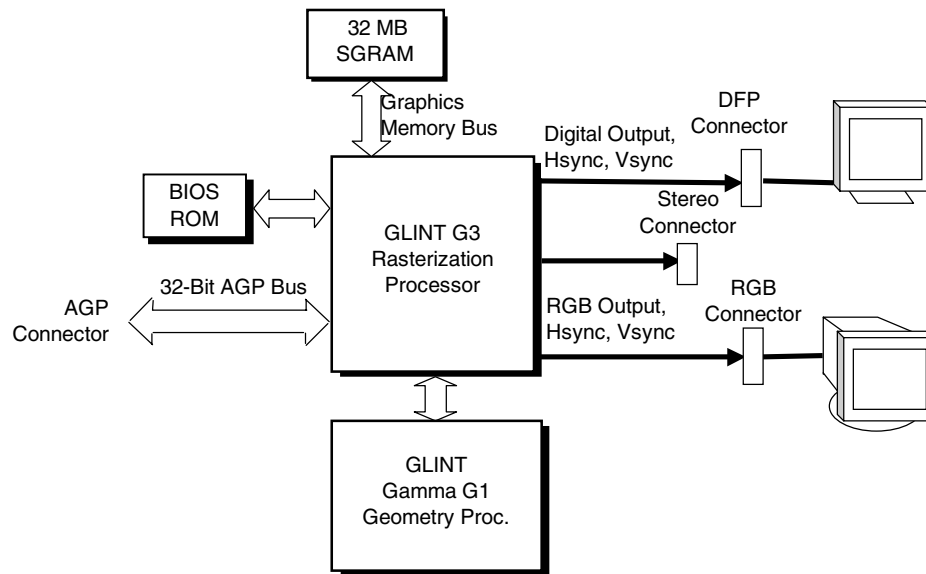


Figure F-2. 3Dlabs Oxygen GVX1 Graphics Card Block diagram

The Oxygen GVX1 graphics card includes 32 megabytes of SGRAM used as the local frame buffer as well as texture storage. The card features a process called Virtual Textual Mapping that uses on-demand loading of textures into local memory on a page-by-page basis (using a 4-KB page granularity). The 3DLABS Oxygen GVX1 AGP Graphics Card includes the following features:

- ◆ AGP 4X transfer support
- ◆ Maximum resolution of 1920 x 1200 w/24-bit color @ 76Hz vertical refresh
- ◆ Bi-linear fill rate of 230M texels per second
- ◆ Tri-linear fill rate of 115M texels per second
- ◆ Can display up to 4.75 M fully transformed and lit polygons per second
- ◆ 300-MHz RAMDAC
- ◆ 125-MHz memory speed
- ◆ 24-bit double buffered color planes
- ◆ 8-bit overlay planes (shared with Alpha planes)
- ◆ 8-bit stencil planes with 24-bit Z-buffer
- ◆ 32-bit Z-buffer (w/o stencil plane, 24-bit w/stencil plane)
- ◆ Digital Flat Panel support (up to 1280 x 1024 @ 60 Hz)
- ◆ Stereographics support
- ◆ Dual display mode using an additional Oxygen GVX1 (PCI) card (SP# 136397-B21) for increased viewing area

F.3 DISPLAY MODES

The graphics modes supported by the 3DLabs Oxygen GVX1 card are listed in Table F-1.

Table F-1.
Graphics Display Modes

Resolution	Color Depth	Horizontal Refresh Freq.	Amount Memory Used [2]
640 x 480	256	100 Hz	512 KB
640 x 480	65K	100 Hz	1 MB
640 x 480	16.7M	100 Hz	1 MB
800 x 600	256	100 Hz	512 KB
800 x 600	65K	100 Hz	1 MB
800 x 600	16.7M	100 Hz	1.5 MB
1024 x 768	256	100 Hz	1 MB
1024 x 768	65K	100 Hz	1.5 MB
1024 x 768	16.7M	100 Hz	2.5 MB
1152 x 864	256	100 Hz	3 MB
1152 x 864	65K	100 Hz	3.5 MB
1152 x 864	16.7M	100 Hz	4 MB
1280 x 800	256	100 Hz	1 MB
1280 x 800	65K	100 Hz	2 MB
1280 x 800	16.7M	100 Hz	4 MB
1280 x 960	256	100 Hz	1.3 MB
1280 x 960	65K	100 Hz	2.5 MB
1280 x 960	16.7M	100 Hz	5 MB
1280 x 1024	256	100 Hz	1.5 MB
1280 x 1024	65K	100 Hz	3 MB
1280 x 1024	16.7M	100 Hz [1]	6 MB
1600 x 1024	256	85 Hz	1.6 MB
1600 x 1024	65K	85 Hz	3.5 MB
1600 x 1024	16.7M	85 Hz	7 MB
1600 x 1200	256	100 Hz	2 MB
1600 x 1200	65K	100 Hz	4 MB
1600 x 1200	16.7M	100 Hz	8 MB
1920 x 1080	256	100 Hz	2 MB
1920 x 1080	65K	100 Hz	4 MB
1920 x 1080	16.7M	100 Hz	8 MB
1920 x 1200	256	76 Hz	2.3 MB
1920 x 1200	65K	76 Hz	4.6 MB
1920 x 1200	16.7M	76 Hz	9.2 MB

NOTES:

■ Resolutions supported for Stereographics functionality .

■ RGB analog output only

[1] 60 Hz refresh rate for DFP.

[2] Value represents amount required by resolution/color depth for frame buffer memory.
Remainder (of 32 MB) available for texture mapping.

F.4 SOFTWARE SUPPORT

The 3Dlabs Oxygen GVX1 graphics card is fully compatible with software written for legacy video modes (CGA, EGA, VGA). Use of extended modes, current operating systems, and the Pentium III's SSEs is supported through software drivers. The following operating systems and programming environments are supported and are either supplied or available from Compaq:

- ◆ Window NT4.0 w/Service Pack 4
- ◆ Powerthreads SSE OpenGL ICD
- ◆ OpenGL 1.1 ICD (1.2 ready)
- ◆ Soft Engine 4 AutoCAD display list

Suggested graphics applications that take advantage of the card's capabilities include:

- ◆ Discreet MAX
- ◆ Lightwave
- ◆ Softimage
- ◆ PRO/E
- ◆ UG
- ◆ Solidworks
- ◆ AutoCAD

F.5 MONITOR POWER MANAGEMENT CONTROL

This controller provides monitor power control for monitors that conform to the VESA display power management signaling (DPMS) protocol. This protocol defines different power consumption conditions and uses the HSYNC and VSYNC signals to select a monitor's power condition. Table F-5 lists the monitor power conditions.

Table F-5.
Monitor Power Management Conditions

HSYNC	VSYNC	Power Mode	Description
Active	Active	On	Monitor is completely powered up. If activated, the inactivity counter counts down during system inactivity and if allowed to timeout, generates an SMI to initiate the Suspend mode.
Active	Inactive	Suspend	Monitor's high voltage section is turned off and CRT heater (filament) voltage is reduced from 6.6 to 4.4 VDC. The Off mode inactivity timer counts down from the preset value and if allowed to timeout, another SMI is generated and serviced, resulting in the monitor being placed into the Off mode. Wake up from Suspend mode is typically a few seconds.
Inactive	Inactive	Off	Monitor's high voltage section and heater circuitry is turned off. Wake up from Off mode is a little longer than from Suspend.

F.6 CONNECTORS

There are three connectors associated with the graphics subsystem; the display/monitor connector, the standard VGA-type (RGB analog) connector, a MDR-20 digital flat panel (DFP) connector, and a stereographics connector.

NOTE: The graphic card's edge connector mates with the AGP connector on the system board. This interface is described in chapter 4.

F.6.1 ANALOG MONITOR CONNECTOR

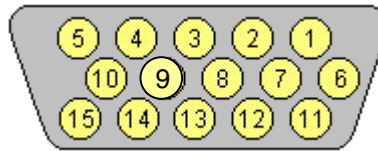


Figure F-3. Analog Monitor Connector, (Female DB-15, as viewed from rear).

Table F-6.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	PWR	+5 VDC (fused) [1]
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	NC	Not Connected
4	NC	Not Connected	12	SDA	DDC2-B Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSynC	Vertical Sync
7	G GND	Blue Analog Ground	15	SCL	DDC2-B Clock
8	B GND	Green Analog Ground	--	--	--

NOTES:

[1] Fuse automatically resets when excessive load is removed.

F.6.2 DFP MONITOR CONNECTOR

A MDR-20 connector is provided to attach a digital flat panel monitor.

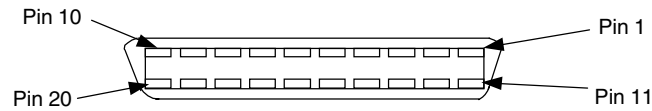


Figure F-4. DFP Monitor Connector, (Female 20-pin, as viewed from rear).

F.6.3 STEREOGRAPHICS CONNECTOR

A three-pin mini-DIN connector is provided to attach stereographics monitor.

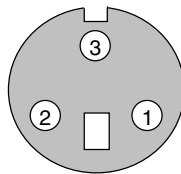


Figure F-5. Stereographics Connector, (as viewed from rear).

F.7 POWER CONSUMPTION

The 3Dlabs Oxygen GVX1 Graphics Card uses 3.3 and 5 VDC power off the AGP bus to the extent listed below:

<u>Volts</u>	<u>Consumption</u>
3.3	14.40 watts
5	6.46 watts

Total Consumption: 20.86 watts

Appendix G

INTEL PRO/100+ MANAGEMENT ADAPTER

G.1 INTRODUCTION

This appendix describes the Intel PRO/100+ Management Adapter, a high-performance Ethernet adapter (Figure G-1) that installs in a PCI slot and is standard on some models covered in this guide. The adapter is based in the Intel 82559 Ethernet Controller and supports ACPI, AOL, and WfM manageability standards.

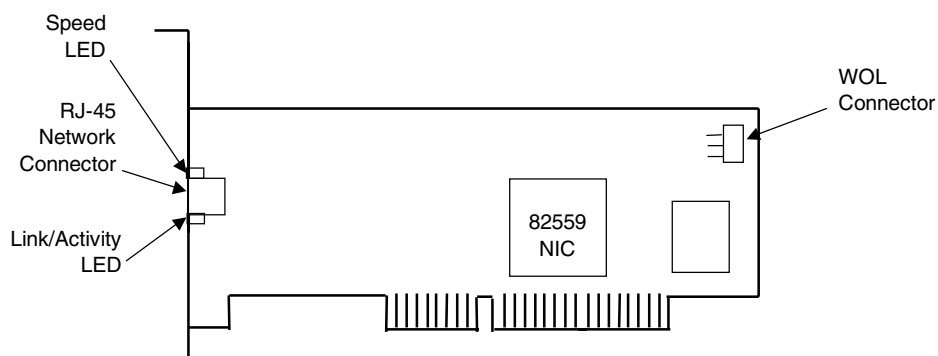


Figure G-1. Intel PRO/100+ Management Adapter Card Layout

This appendix covers the following subjects:

- | | |
|--------------------------------|----------|
| ◆ Functional description (G.2) | page G-2 |
| ◆ Power management (G.3) | page G-4 |
| ◆ Adapter programming (G.4) | page G-5 |
| ◆ Network connector (G.5) | page G-6 |
| ◆ Adapter specifications (G.6) | page G-6 |

G.2 FUNCTIONAL DESCRIPTION

The Intel PRO/100+ Management Adapter is based on the Intel 82559 Ethernet Controller supported by firmware in flash ROM (Figure G-2). The adapter provides a physical interface with a network through an RJ-45 network connector and includes two status (speed and link/activity) LEDs. The adapter can operate in half- or full-duplex modes and provides auto-negotiation of both mode and speed. Half-duplex operation features an Intel-proprietary collision reduction mechanism while full-duplex operation follows the IEEE 802.3x flow control specification. Transmit and receive FIFOs of three kilobytes each reduce the chance of overrun while waiting for bus access. The card includes an on-board 5/3.3 VDC regulator circuit and WOL connector in support of Wake-On-LAN functionality.

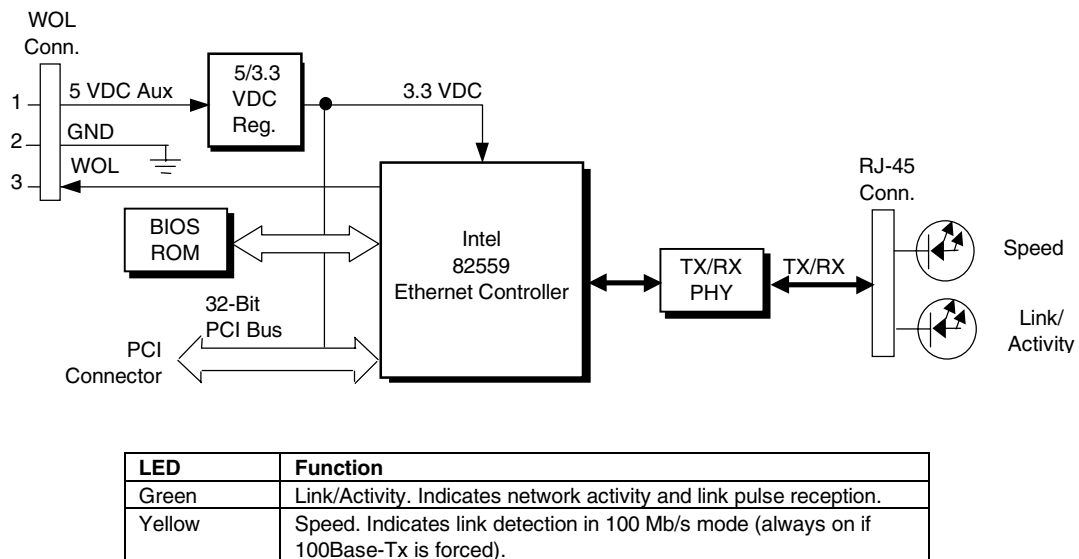


Figure G-2. Intel PRP/100+ Management Adapter, Block diagram

Key features of the adapter include:

- ◆ 32-bit architecture and separate 3-KB transmit and receive buffers.
- ◆ PCI ver. 2.2 compliant
- ◆ Dual-mode support with auto-switching between 10BASE-T and 100BASE-TX
- ◆ Both APM and ACPI power management support
- ◆ AOL ver. 1.0 and WOL support

The 82559 controller features high and low priority queues and provides priority-packet processing for networks that support that feature. The controller's micro-machine processes transmit and receive frames independently and concurrently. Receive runt (undersized) frames are not passed on as faulty data but discarded by the controller, which also directly handles such errors as collision detection or data under-run. An EEPROM is used to store identification, configuration, and connection parameters.

G.2.1 AOL FUNCTION

The adapter's Alert-On-LAN (AOL) function provides a AOL-compliant system unit with the ability to communicate system status to a management console, even while the system is powered down. When installed in an AOL-compliant system, the adapter receives alert messages from the system's I/O Controller Hub (ICH) over the PCI bus. Each alert message is decoded by the adapter and a resulting pre-constructed status message is then transmitted over the network to a management console.

Alert-On-LAN functionality occurs independent of software, driver, or even processor intervention. The adapter can report following conditions:

- ◆ System tampering – Removal of the chassis cover
- ◆ BIOS failure – System fails to boot successfully
- ◆ OS problem – System fails to load operating system after boot
- ◆ Missing/faulty processor – Processor fails to fetch first instruction
- ◆ Thermal condition – High temperature detected in system
- ◆ Heartbeat – Indication of system's presence on the network (sent approximately every 30 seconds)

NOTE: The system unit must be plugged into a live AC outlet for the AOL function to be operative. **Controlling a system unit's power through an AC outlet strip will, when the strip is turned off, disable AOL functionality.**

The AOL implementation requirements are as follows:

1. System unit featuring the 810, 810e, or 820 (or later) chipset.
2. Intel PRO/100+ Management Adapter Driver 3.1 or later (available from Compaq).
3. Client-side utility agent software (available from Compaq).
4. Management console running one of the following:
 - a. HP OpenView Network Node Manager 6.x.
 - b. Intel LANDesk Client Manager.
 - c. Compaq Insight Manager.

G.2.2 WAKE UP FUNCTIONS

The adapter provides two types of wake-up signaling: the PME- signal and the WOL signal.

The adapter provides PME- signal support for systems compliant with PCI ver. 2.2. The detection of any wake event results in the adapter's assertion of the PME- signal, which can be used by the system unit to initiate the power-up sequence. System software is responsible for the clearing the PME- signal.

The adapter also includes a WOL interface for systems supporting that method of wake-up. The adapter asserts the WOL signal for 50 milliseconds upon detection of a Magic Packet. The WOL signal is routed to the system unit (through a three-conductor cable connection) for initializing a power-up sequence.

G.3 POWER MANAGEMENT SUPPORT

The NIC adapter supports APM and ACPI power management environments as well as the Wired-for-Management (WfM) and Wake-On-LAN (WOL) standards. The adapter is designed to be powered up as long as the system unit is plugged into a live AC outlet to provide system “wake-up” functionality. Power is provided by either the auxiliary 3.3 VDC power rail of the PCI bus (when installed in systems compliant with PCI ver. 2.2) or by auxiliary 5 VDC through the WOL connector.

NOTE: Controlling a system unit’s power through an AC outlet strip will, **with the strip turned off, disable wake-up functionality.**

G.3.1 APM ENVIRONMENT

The Advanced Power Management (APM) functionality of system wake up is implemented through the system’s APM-compliant BIOS and Magic Packet-compliant hardware. This environment is not dependent on operating system (OS) intervention allowing a unit plugged into a live AC outlet to be turned on remotely over the network (i.e., “remote wake-up”) even if the OS has not been installed. In APM mode the controller will respond upon receiving a Magic Packet, which is a packet where the node’s address is repeated 16 times. Upon Magic Packet reception, the adapter asserts the PME- signal (on the PCI bus) resulting in the system unit’s power control logic turning on the system and initiating the boot sequence. After the boot sequence the BIOS clears the PME- signal so that subsequent wake up events will be detected.

G.3.2 ACPI ENVIRONMENT

The Advanced Configuration and Power Interface (ACPI) functionality of system wake up is implemented through an ACPI-compliant OS (such as Windows NT 5.0) and is the default power management mode. The following wake up events may be individually enabled/disabled through the software driver supplied with the adapter:

- ◆ Magic Packet – Packet with node address repeated 16 times in data portion.
- ◆ Individual address match – Directed acket with matching user-defined byte mask.
- ◆ Multicast address match – Directed packet with matching user-defined sample frame.
- ◆ ARP (address resolution protocol) packet
- ◆ Flexible packet filtering – Packets that match defined CRC signature.
- ◆ NBT query (under Ipv4)
- ◆ IPX Diagnostic
- ◆ TCO packet
- ◆ VLAN Type

When an enabled event is received the controller asserts the PME- signal that is used to initiate the wakeup sequence.

G.4 ADAPTER PROGRAMMING

Programming the adapter consists of configuration, which occurs during POST, and control, which occurs at runtime.

G.4.1 CONFIGURATION

The adapter's 82559 NIC controller is a PCI device and configured through PCI configuration space registers using PCI protocol described in chapter 4 of this guide. The PCI configuration registers are listed in the following table:

Table G-1.
PCI Configuration Registers

PCI Conf. Addr.	Register	Value on Reset	PCI Conf. Addr.	Register	Value on Reset
00-01h	Vender ID	8086h	10-13h	Cntrl. Reg. Base Addr. (Mem)	0000h
02-03h	Device ID	1229h	14-17h	Cntrl. Reg. Base Addr. (I/O)	00h
04-05h	PCI Command	0000h	18-1Bh	Flash Mem. Base Addr.	00h
06-07h	PCI Status	0280h	2C-2Dh	Subsystem Vender ID	
08h	Revision ID	xxh	2E-2Fh	Subsystem ID	
09-0Bh	Class Code	01h	30-33h	Expansion ROM Base Addr.	
0Ch	Cache Line Size	01h	34h	Cap-Ptr	
0Dh	Latency Timer	04h	3C-3D	Interrupt Line/Pin	
0Eh	Header Type	00h	3E-3Fh	Min Gnt/Max Lat	
0Fh	BIST	00h	DC-E3h	Power Mgmt. Functions	

NOTE:

Assume unmarked gaps are reserved and/or not used.

G.4.2 CONTROL

The adapter's 82559 controller is controlled through registers that may be mapped in system memory space or variable I/O space. The registers are listed in the following table:

Table G-2.
Control Registers

Offset Addr. / Register	No. of Bytes	Offset Addr. / Register	No. of Bytes
00h SCB Status	2	19h Flow Control Register	2
02h SCB Command	2	1Bh PMDR	1
04h SCB General Pointer	4	1Ch General Control	1
08h PORT	4	1Dh General Status	1
0Ch Flash Control Reg.	2	1E-2Fh Reserved	10
0Eh EEPROM Control Reg.	2	30h Function Event Register	4
10h Mgmt. Data I/F Cntrl. Reg.	4	34h Function Event Mask Register	4
14h Rx Direct Mem. Access Byte Cnt.	4	38h Function Present State Register	4
18h Early Receive Interrupt	1	20h Force Event Register	4

Not implemented in these systems (CardBus registers).

G.5 NETWORK CONNECTOR

Figure G-3 shows the RJ-45 connector used for the NIC interface. This connector includes the two status LEDs as part of the connector assembly.

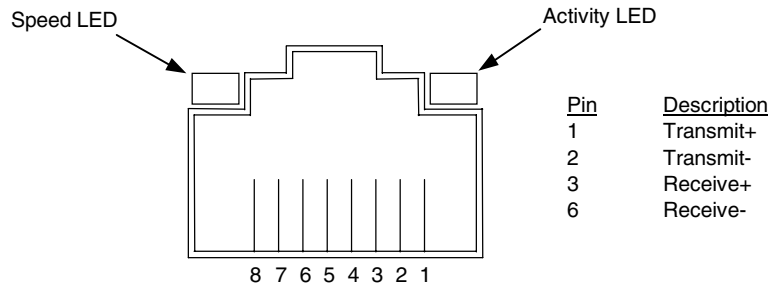


Figure G-3. Ethernet TPE Connector (RJ-45, viewed from card edge)

G.6 ADAPTER SPECIFICATIONS

Table G-3.
Adapter Specifications

Parameter	
Modes Supported	10BASE-T half duplex @ 10 MB/s 10Base-T full duplex @ 20 MB/s 100BASE-TX half duplex @ 100 MB/s 100Base-TX full duplex @ 200 MB/s
Standards Compliance	IEEE VLAN (802.1A) IEEE 802.2 IEEE 802.3 & 802.3u IEEE Intel priority packet (801.1p)
OS Driver Support	MS Windows 95,98, and 2000 beta MS Windows NT 3.51 & 4.0 Novell Netware 3.11, 3.12, & 4.1x; 5 Server Sunsoft Solaris SCO UnixWare Open Desktop OpenServer
Boot ROM Support	Intel PRO/100 Boot Agent (PXE 2.0, RPL)
F12 BIOS Support	Yes
Bus Interface	PCI 2.2
Power Management Support	APM, ACPI, PCI Power Management Spec.
Power Consumption	0.750 mW (max)

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