
Technical Reference Manual Hardware and BIOS

HP Vectra VL

6/xxx Series 6 PC

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Preface

This manual is a technical reference and BIOS document for engineers and technicians providing system level support. It is assumed that the reader possesses a detailed understanding of AT-compatible microprocessor functions and digital addressing techniques.

Technical information that is readily available from other sources, such as manufacturer's proprietary publications, has not been reproduced.

This manual contains summary information only. For additional reference material, refer to the bibliography, on the next page.

Conventions

The following conventions are used throughout this manual to identify specific numeric elements:

- Hexadecimal numbers are identified by a lower case h.
For example, 0FFFFFFFh or 32F5h
- Binary numbers and bit patterns are identified by a lower case b.
For example, 1101b or 10011011b

Bibliography

- ❑ HP Vectra VL 6/xxx Series 6 *User's Guide* manual (D5040-90001).
- ❑ HP Vectra VL 6/xxx MT Series 6 *User's Guide* manual (D5050-90001).
- ❑ HP Vectra VL 6/xxx Series 6 *Familiarization Guide* (D5040-90901).
- ❑ *HP Network Administrator's Guide* (online).
- ❑ *HP Vectra Accessories Service Handbook - 7th edition* (5965-4074).
- ❑ *HP Vectra PC Service Handbook (Volume 1) - 12th edition* (to be announced).
- ❑ *HP Support Assistant* CD-ROM (by subscription).

The following Intel® publications provide more detailed information:

- ❑ *Pentium Pro Family Developer's Manual*, Volume 1: *Specifications*, Intel, 1996, ISBN 1-55512-259-0
- ❑ *Pentium Pro Family Developer's Manual*, Volume 2: *Programmer's reference manual*, Intel, 1996, ISBN 1-55512-260-4
- ❑ *Pentium Pro Family Developer's Manual*, Volume 3: *Operating System Writer's Manual*, Intel, 1996, ISBN 1-55512-261-2

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System Overview

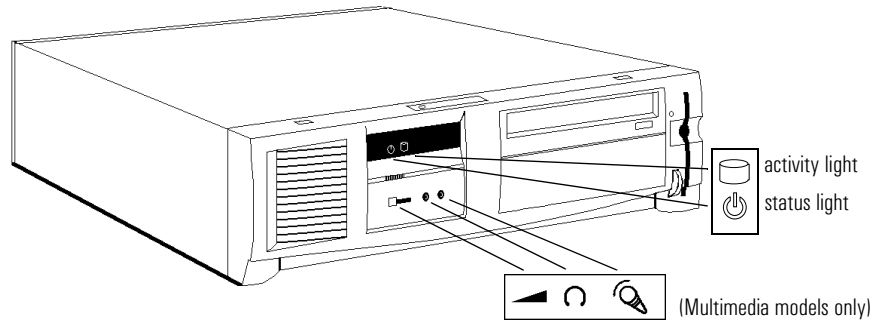
This manual describes the *HP Vectra VL 6/xxx Series 6 PC*, and provides detailed system specifications.

This chapter introduces the external features, and lists the specifications and characteristic data of the system. It also summarizes the documentation which is available.

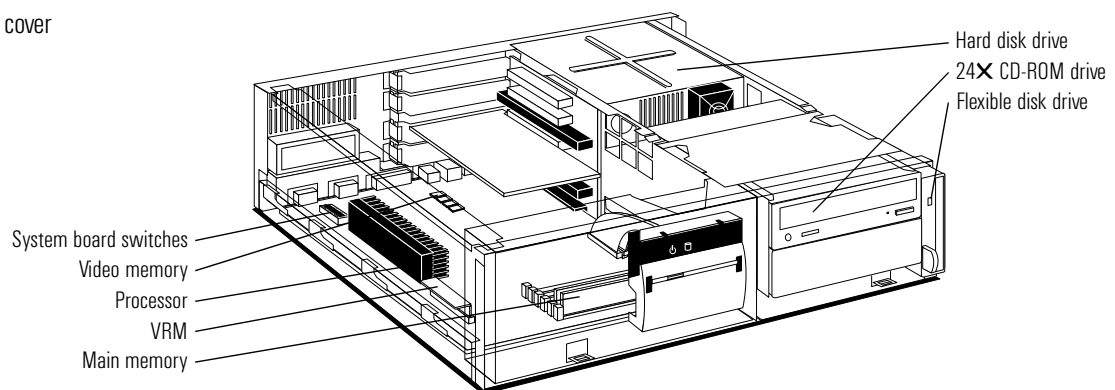
1 System Overview

Package

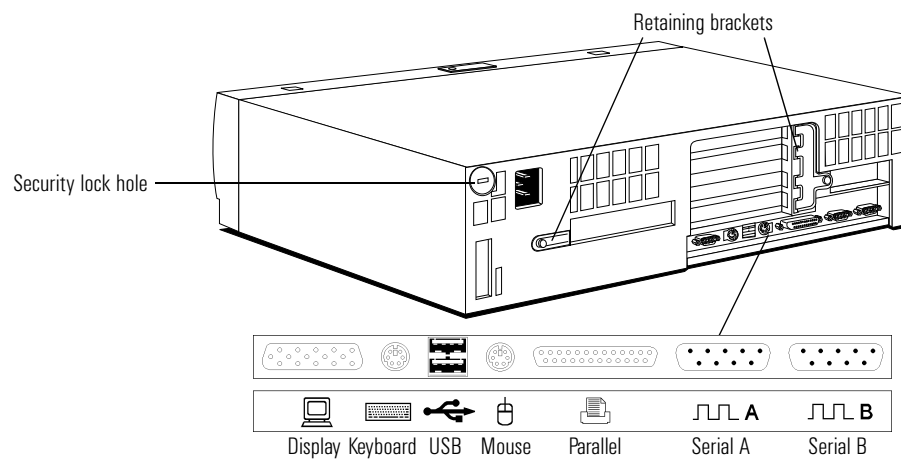
Front view



Front view with cover removed



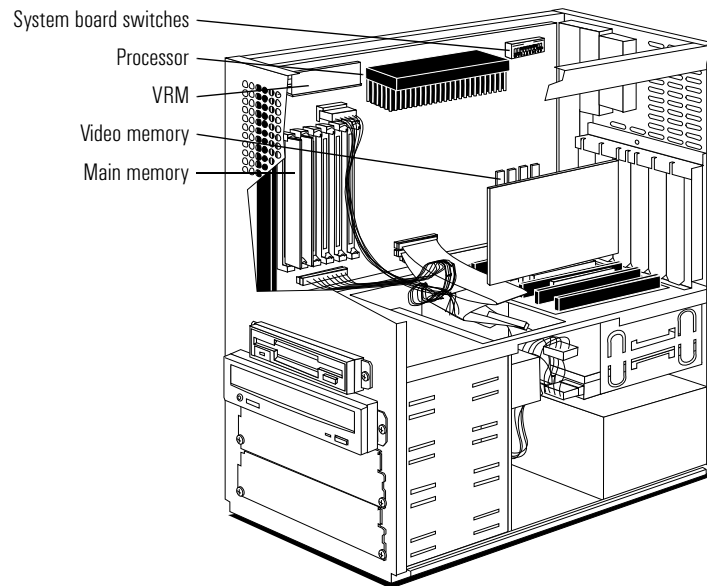
Rear view



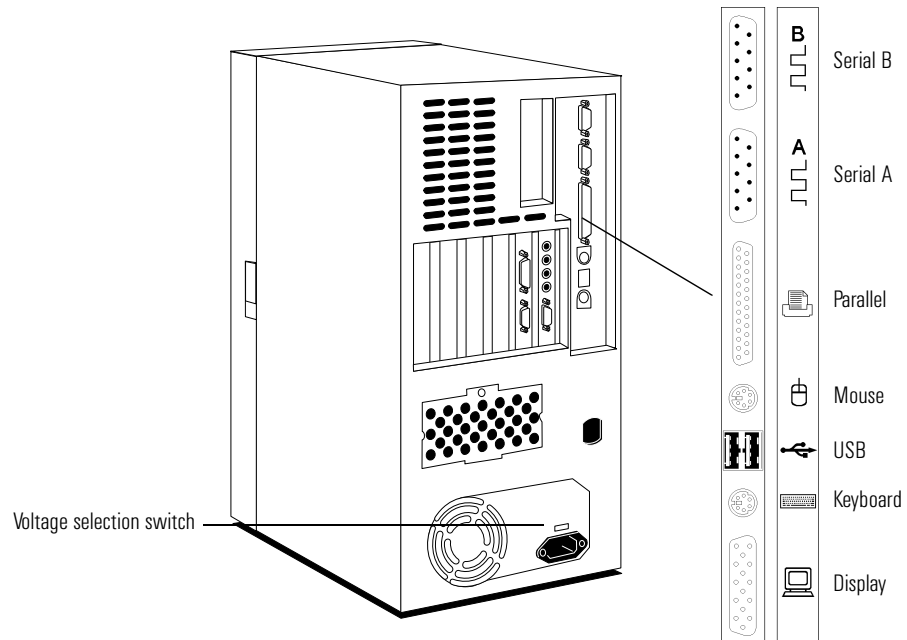
(All icons shown here are for information, and do not necessarily appear on the PC).

Minitower Package

Front view with cover removed



Rear view



(All icons shown here are for information, and do not necessarily appear on the PC).

1 System Overview

Specifications and Characteristic Data

Specifications and Characteristic Data

Physical Characteristics

System Processing Unit		
	Desktop	Minitower
Weight	9 kg (20 lbs)	15 kg (33 lbs)
Dimensions	44.6 cm (D) by 43.5 cm (W) by 13.2 cm (H) 17.5 inches by 17.1 inches by 5.2 inches	44 cm (D) by 19.2 cm (W) by 43.8 cm (H) 17.3 inches by 7.6 inches by 17.2 inches
Footprint	0.194 m ² (2.08 sq ft)	0.085 m ² (0.91 sq ft)
Keyboard		
Flat	464 mm (W) by 178 mm (D) by 33 mm (H) (18.3 inches by 7 inches by 1.3 inches)	
Standing	464 mm (W) by 178 mm (D) by 51 mm (H) (18.3 inches by 7 inches by 2 inches)	

Environmental Specification

System Processing Unit with a Hard Disk		
Acoustic noise emission (operating)	LwA < 40 dB	LpA < 35 dB
Acoustic noise emission (operating with hard disk drive access)	LwA < 41 dB	LpA < 35 dB
Acoustic noise emission (operating with flexible disk drive access)	LwA < 43 dB	LpA < 38 dB
Operating temperature	+ 10°C to +40°C	(+ 50°F to 104° F)
Recommended operating temperature	+ 15°C to +40°C	(+ 59°F to + 104°F)
Storage temperature	-40°C to +70°C	(-40°F to +158°F)
Over temperature shutdown	+ 50°C	(+ 122°F)
Operating humidity	15% to 80% (relative)	
Storage humidity	8% to 80% (relative), non-condensing at 40°C (104°F)	
Operating altitude	3100 m max	(10000 ft max)
Storage altitude	4600 m max	(15000 ft max)

Operating temperature and humidity ranges may vary depending upon the mass storage devices installed. High humidity levels can cause improper operation of disk drives. Low humidity levels can aggravate static electricity problems and cause excessive wear of the disk surface.

Electrical Specification

For the desktop models:

Parameter	Limit for the Power Supply		Notes	Limit per PCI Accessory Slot	Limit per ISA Accessory Slot
Input voltage	100-127 Vac	200-240 Vac	Auto-ranging		
Input voltage range	90-264 Vac				
Input current (max)	3 A				
Input power (max)	150 W				
Input power (typical ¹)	< 63 W < 31 W < 30 W < 24 W < 1.2 W	< 65 W < 34 W < 30 W < 24 W < 2.8 W	Fully-on mode (with input/output) Fully-on mode (without input/output) Standby mode Suspend mode Off (but plugged in)		
Input frequency	45 Hz to 66 Hz				
Available power	120 W (continuous)			25 W (max)	7 W (max)
Max current at +5 V	13.5 A			4.5 A	4.5 A
Max current at +3.3 V	6 A			—	—
Max current at -5 V	0.1 A			—	0.1 A
Max current at +12 V	4.5 A			0.5 A	1.5 A
Max current at -12 V	0.3 A			0.1 A	0.3 A

¹Dependant on operating system and PC configuration

1 System Overview

Specifications and Characteristic Data

For the minitower models:

Parameter	Limit for the Power Supply		Notes	Limit per PCI Accessory Slot	Limit per ISA Accessory Slot
Input voltage	100-127 Vac	200-240 Vac	Switch selectable		
Input voltage range	90-140 Vac	180-264 Vac			
Input current (max)	5 A	3 A			
Input power (max)	200 W				
Input power (typical ¹)	< 59 W < 35 W < 30 W < 24 W < 1.3 W	< 58 W < 35 W < 30 W < 24 W < 1.3 W	Fully-on mode (with input/output) Fully-on mode (without input/output) Standby mode Suspend mode Off (but plugged in)		
Input frequency	45 Hz to 66 Hz				
Available power	160 W (continuous)			25 W (max)	7 W (max)
Max current at +5 V	20 A			4.5 A	4.5 A
Max current at +3.3 V	12 A			—	—
Max current at -5 V	0.2 A			—	0.1 A
Max current at +12 V	4.4 A			1.5 A	0.5 A
Max current at -12 V	0.5 A			0.1 A	0.3 A
Max current at +5 Vst	0.05 A			—	—

¹-Dependant on operating system and PC configuration

When the computer is turned off, but left plugged in at the mains, the power consumption falls below 5 watts, but is not zero. If the computer is completely unplugged from the mains, the real time clock continues to operate from the charge stored in the battery. If the computer is left plugged in, but not turned on, it continues to supply power to the real time clock, and also keeps the battery recharged. The life-time of rechargeable batteries is considerably extended by keeping them in a fully charged state.

The battery can be recharged by plugging the computer back in for at least an hour. It is not necessary to start the computer.

Documentation

The table below summarizes the availability of documentation that is appropriate to the *HP Vectra VL 6/xxx Series 6 PCs*. Only selected publications are available on paper. Most are available as viewable files (which can also be printed) from the HP division support servers, and on the *HP Support Assistant CD-ROM*.

	Division Support Server	Support Assistant CD-ROM	Paper-based
HP Vectra VL 6/xxx Series 6 User's Guide	PDF file	PDF file	<i>DT</i> : D5040A <i>MT</i> : D5050A
HP Vectra VL 6/xxx Series 6 Familiarization Guide	PDF file	PDF file	D5040-90901
HP Vectra VL 6/xxx Series 6 Technical Reference Manual	PDF file	PDF file	no
HP Vectra PC Service Handbook (Vol 1, 12th Edition)	PDF file	PDF file	To be announced
HP Vectra Accessory Service Handbook (7th Edition)	PDF file	PDF file	5965-4074

Each PDF file (portable document format) can be viewed on the screen by opening the file with Acrobat Reader. To print the document, press Ctrl+P whilst you have the document on the screen. You can use the page-up, page-down, goto page, search string functions to read the document on the screen. (Note, though, that for some documents, there is difference between the page number that is printed on the page, and the page number that Acrobat Reader indicates, because of the presence of the front matter pages).

1 System Overview

Documentation

Where to Find the Information

The following table summarizes the availability of information within the *HP Vectra VL 6/xxx Series 6 PC* documentation set.

	User Guide	User Online	Familiarization Guide	Service Handbook	Technical Reference Manual
Introducing the computer					
Product features	Key features	Exploring	New features	Exploded view Parts list	Key features
Product model numbers				Product range CPL dates	
Using the computer					
Connecting cables and turning on	Keyboard, mouse, display, network, printer, power				
Finding on-line information	Finding READ.MEs and on-line documentation				
Environmental		Working in comfort			System overview
Formal documents	Software license agreement Warranty information	S/w license agreement			
Upgrading the computer					
Opening the computer	Full details				
Supported accessories	Some part number details			Full PN details	
Replacing accessories	How to install		New procedures		
Configuring devices		Configuring peripherals			Problem fixes
Fields and their options within <i>Setup</i>					Key fields
Repairing the computer					
Troubleshooting	Basic		New symptoms	Service notes	Advanced
Technical information	Basic	Detailed			Advanced
System board	Jumpers, switches and connectors		Jumpers, switches and connectors How to replace	Jumpers, switches and connectors	Jumpers, switches and connectors Chip-set details
BIOS	Basic details		Upgrading		Technical details Memory maps
Power-On Self-Test routines (POST)	Key error codes and suggestions for corrective action				Order of tests Complete list

System Board

The next chapter describes the graphics, disk and audio devices which are supplied with the computer.

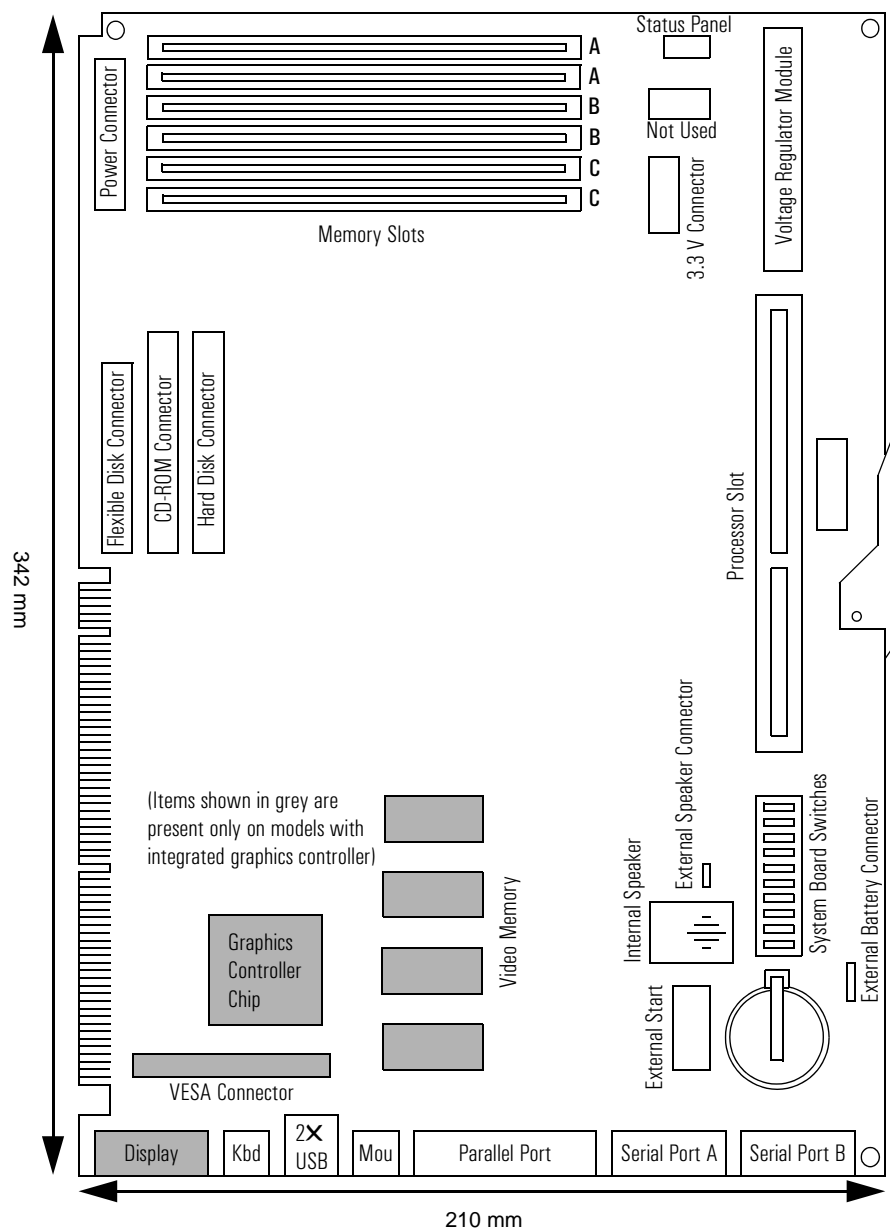
This chapter describes the components of the system board, taking in turn the components of the Processor-Local Bus, the Peripheral Component Interconnect (PCI) bus and the Industry Standard Architecture (ISA) bus.

2 System Board

System Board and Backplane Boards

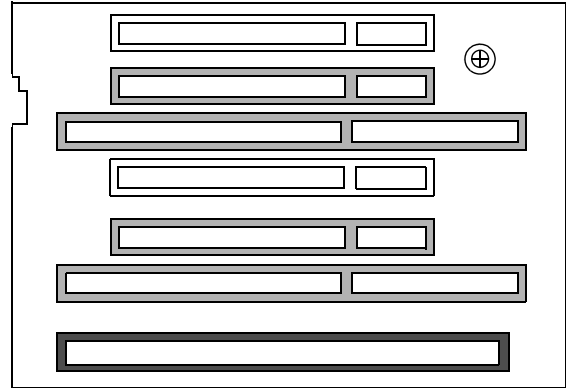
System Board and Backplane Boards

Most desktop and minitower models are supplied with a Matrox graphics controller on a PCI board, and do not have the integrated graphics controller loaded on the system board.



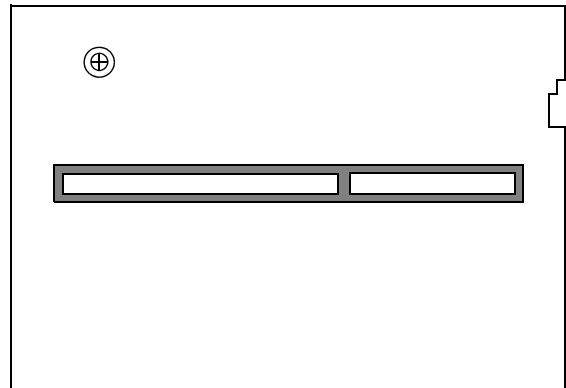
Desktop (front view)

- 2 X PCI slot (shown in white)
 - 2 X ISA/PCI combination slot (shown in light grey)
 - 1 X system board slot (shown in dark grey)
- PCI Slot #4 (J12)
- PCI Slot #3 (J5)
- PCI Slot #2 (J11)
- PCI Slot #1 (J6)



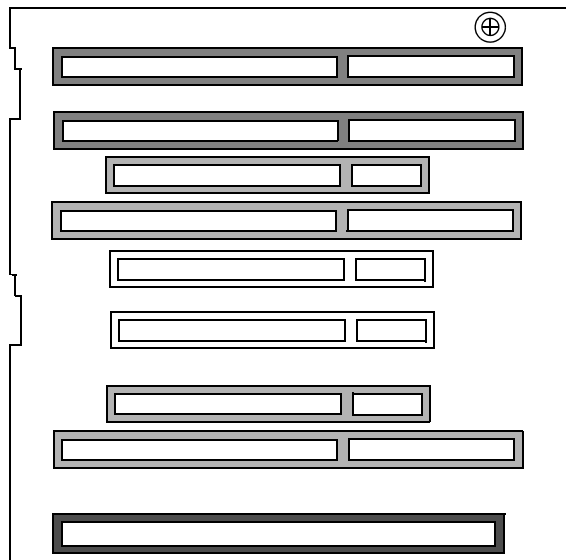
Desktop (rear view)

- 1 X ISA slot (shown in grey)



Minitower (top view)

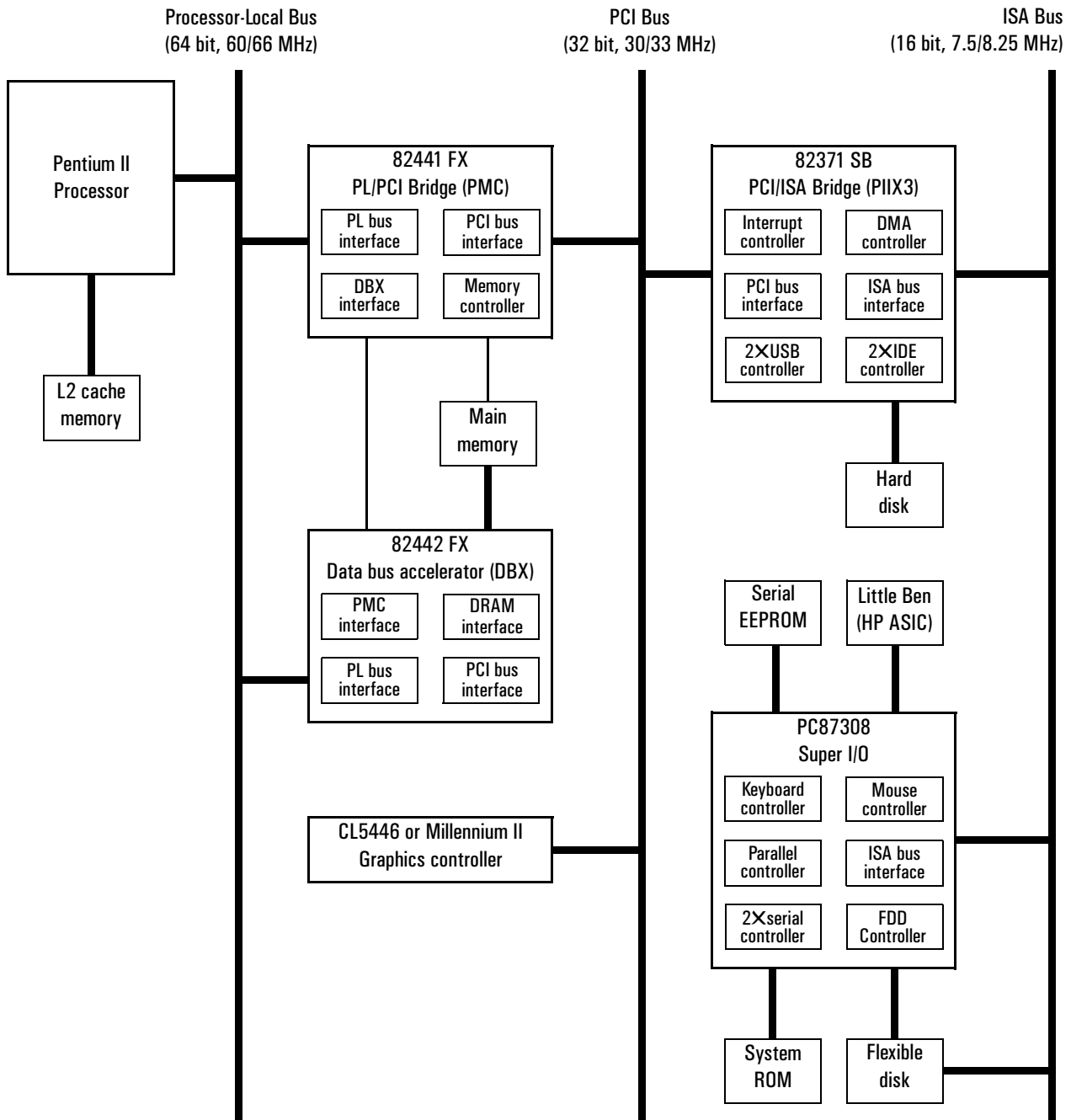
- 2 X ISA slot (shown in grey)
 - 2 X PCI slot (shown in white)
 - 2 X ISA/PCI combination slot (shown in light grey)
 - 1 X system board slot (shown in dark grey)
- PCI Slot #4 (J12)
- PCI Slot #3 (J5)
- PCI Slot #2 (J11)
- PCI Slot #1 (J6)



2 System Board

Architectural View

Architectural View



Chip-Set

The chip-set comprises four chips. These interface between the three main buses (the Processor-Local bus, the PCI bus and the ISA bus).

- The PMC chip (82441FX) is a combined *PL/PCI bridge* and *main memory controller*.
- The DBX chip (82442FX) is the *data bus accelerator*, implementing the datapath between the processor local bus and main memory.
- The PIIX3 chip (82371SB) is a combined *PCI/ISA bridge* and *IDE controller* and *USB controller*.
- The Super I/O chip (37C932) is a combined *serial interface* and *parallel interface* and *keyboard controller* and *mouse controller* and *flexible disk drive controller*.

The PMC, PL/PCI Bridge Chip (82441 FX)

This forms the bridge between the Processor Local Bus (PL Bus) and the PCI Bus.

PL Bus Interface

The PMC chip monitors each cycle that is initiated by the processor, and forwards those to the PCI bus that are not targeted at the local memory. It translates PL bus cycles into PCI bus cycles.

The chip supports the SMM mode of the Pentium processor, the CPU stop clock hardware function, and the keyboard lock function. These are used by the LittleBen chip, as described on page 34.

PCI Bus Interface

Sequential PL-to-PCI memory write cycles are translated into PCI zero wait state burst cycles. The maximum PCI burst transfer can be between 256 bytes and 4 KB. The chip supports advanced snooping for PCI master bursting, and provides a pre-fetch mechanism dedicated for IDE read.

The PCI arbiter supports PCI bus arbitration for up to four masters using a rotating priority mechanism. Its hidden arbitration scheme minimizes arbitration overhead.

Main Memory Controller The main memory controller supports up to 512 MB of dynamic random access memory (DRAM), arranged in banks of any mixture of memory capacities, provided that each bank contains a pair of identical single interline memory modules (SIMMs). With the 32 MB module from HP, the three banks on these PCs gives a total capacity of 192 MB. With a 64 MB module from HP, it will give a total capacity of 384 MB.

DBX Interface The DBX chip, described next, is controlled by the PMC chip.

The DBX, Data Bus Accelerator Chip (82442 FX)

PMC Interface The DBX chip implements a 64-bit data path (not interleaved) between the Processor-Local bus and main memory modules.

PL Bus Interface This unit takes the data from the Processor Local bus that is to be written to the memory, and takes the data out to the Processor Local bus that has been read from the memory.

Data Path Storage elements are provided for bidirectional data buffering among the 64-bit PL data bus, the 64/32-bit memory data bus, and the 32-bit PCI address/data bus.

There are three FIFO (first-in first-out) queues, and one read buffer for the paths between the PL, PCI, and Memory buses. This buffering is used, partly, to smooth the differences in bandwidths between the three buses, thereby improving the overall system performance. During bus operations between the PL, PCI and Memory buses, the chip receives control signals from the PMC, performs functions such as data latching, data forwarding to the destination bus, and data assemble and disassemble.

Whilst accesses to the local memory are in progress, whether it be from the PL or PCI bus, the PMC maintains control of the secondary cache, DRAMs, and the datapath.

DRAM Interface In the case of 66 MHz PL bus operation, memory accesses have a timing pattern of 5-2-2-2 for a page-hit. This degrades to 8-2-2-2 for a row-miss, and to 11-2-2-2 for a page-miss. When the banks have been filled in an arbitrary order, back-to-back burst reads keep to the 5-2-2-2,5-2-2-2 timing

pattern. When the banks have been filled contiguously (bank A, then bank B, then bank C), back-to-back burst reads are improved to a 5-2-2-2,3-2-2-2 timing pattern.

The controller supports relocation of system management memory. It supports a read cycle power saving mode, and a CAS before RAS *Intelligent Refresh* mode of operation, with a CAS# driving current that is programmable.

The controller is fully configurable for the characteristics of the shadow RAM (640 KB to 1 MB). It supports concurrent write back.

The PIIX3, PCI/ISA Bridge Chip (82371SB)

This chip is encapsulated in a 208 pin plastic quad flat pack (PQFP) package.

PCI Bus Interface

This part of the chip is responsible for transferring data between the PCI bus and the ISA expansion bus. It performs PCI-to-ISA, and ISA-to-PCI bus cycle translation. It supports the Plug-and-Play mechanism. Data buffers are provided, to isolate the PCI and ISA buses.

ISA Bus Interface

As well as accepting cycles from the PCI bus interface, and translating them for the ISA bus, the ISA bus interface also requests the PCI master bridge to generate PCI cycles on behalf of a DMA or ISA master. The ISA bus interface contains a standard ISA bus controller and data buffering logic. It can directly support six ISA slots without external data or address buffering.

IDE Controller

The PCI master/slave IDE controller, supporting four devices, two on each of two channels, is described on page 29.

USB Controller

The PCI USB controller, supporting two connectors, is described on page 30.

DMA Controller

The seven channel DMA controller incorporates the functionality of two 82C37 DMA controllers. Channels 0 to 3 are for 8-bit DMA devices, while channels 5 to 7 are for 16-bit devices (see page 67). The channels can be programmed for any of the four transfer modes: the three active modes (single, demand, block), can perform three different types of transfer: read, write and verify. The address generation circuitry supports a 24-bit address for DMA devices.

2 System Board

Chip-Set

Interrupt Controller

The sixteen channel interrupt controller incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded, giving 14 external and two internal interrupt sources (see page 67).

Counter / Timer

The chip contains a three-channel 82C54 counter/timer. The counters use a division of the 14.318 MHz OSC input as the clock source.

The SIO, Super I/O Controller (NS 87308)

The *Super I/O* chip (NS 87308) provides the control for two FDC devices, two serial ports and one bidirectional multi-mode parallel port.

Function	Logical device number
Flexible disk controller	0 ??
Parallel port controller	3 ??
UART1 controller	4 ??
UART2 controller	5 ??
RTC	6 ??
Keyboard controller	7 ??
Mouse controller	7 ??
General purpose I/O (GPIO)	8 ??

Serial / parallel communications ports

The two 9-pin serial ports (whose pin layouts are depicted on page 55) support RS-232-C and are buffered by 16550 UARTs, with 16 Byte FIFOs. They can be programmed as COM1, COM2, COM3, COM4, or disabled.

The 25-pin parallel port (also depicted on page 55) is Centronics compatible, supporting IEEE 1284. It can be programmed as LPT1, LPT2, or disabled. It can operate in the following four modes:

- ☐ Standard mode (PC/XT, PC/AT, and PS/2 compatible).
- ☐ Bidirectional mode (PC/XT, PC/AT, and PS/2 compatible).
- ☐ Enhanced mode (enhanced parallel port, EPP, compatible).
- ☐ High speed mode (MS/HP extended capabilities port, ECP, compatible).

FDC	The integrated <i>flexible disk controller</i> (FDC) supports any combination of two of the following: tape drives, 3.5-inch flexible disk drives, 5.25-inch flexible disk drives. It is software and register compatible with the 82077AA, and 100% IBM compatible. It has an A and B drive-swapping capability and a non-burst DMA option.
RTC	The real-time clock (RTC) is 146818A-compatible. With an accuracy of 20 ppm (parts per million). The configuration RAM is implemented as 256 bytes of CMOS memory.
Keyboard and Mouse Controller	The computer has an 8042-based keyboard and mouse controller. The connector pin layouts are shown on page 55. The Power-On keyboard is described on page 31.
Serial EEPROM	This is the non-volatile memory which holds the values for the <i>Setup</i> program (they are no longer stored in the CMOS memory).

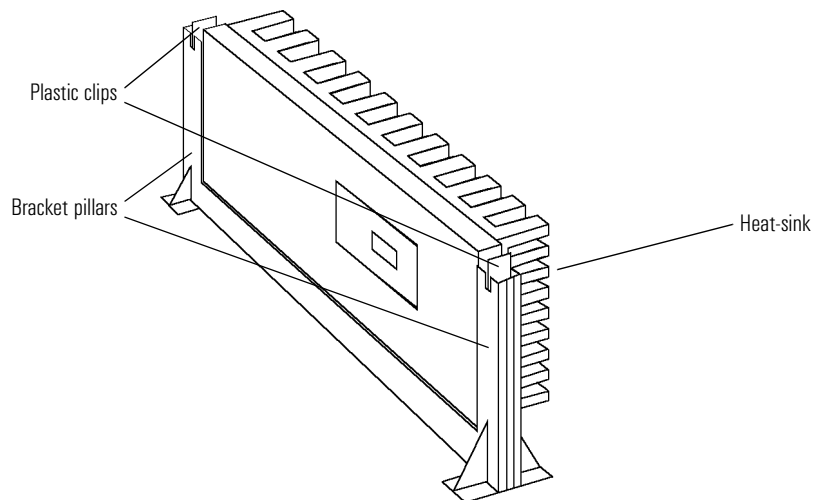
2 System Board

Devices on the Processor-Local Bus

Devices on the Processor-Local Bus

Intel Pentium II Microprocessor

The Pentium II processor and level-2 cache memory are packaged in a self-contained, pre-sealed module, installed in a socket on the system board. The heat-sink is supplied with the processor, and is bolted to it by the manufacturer. The module is held in place by a bracket. There are two plastic clips, one on the top of each pillar of the bracket, to hold the processor module in place.



To remove the old processor module:

- 1 Press the two plastic clips towards each other.
- 2 Carefully pull the processor module away from its connector on the system board.

Only upgrades, pin compatible with the original processor, manufactured by Intel, are supported.

Every processor that is installed, or replaced, must be accompanied by the voltage regulator module (VRM) that is supplied with it. Each VRM is specific to the processor with which it is supplied, and should be used only with that processor.

Bus Frequencies

There is a 14.318 MHz crystal oscillator on the system board. This frequency is multiplied to 60 or 66 MHz by a phase locked loop. This is further scaled by an internal clock multiplier within the processor. For example, the Pentium II 233 MHz processor multiplies the 66 MHz system clock by 3.5. Switches 1 and 2, on the system board switches, set the frequency of the Processor-Local bus. Switches 3, 4 and 5 set the clock multiplier ratio.

Switch		Processor Local Bus Frequency	PCI Bus Frequency	ISA Bus Frequency	Switch			Frequency Ratio Processor: Local Bus	Processor Frequency
1	2				3	4	5		
Closed	Open	60 MHz	30 MHz	7.5 MHz	Open	Open	Closed	2.5 : 1	150 MHz ¹
Open	Open	66 MHz	33 MHz	8.25 MHz	Open	Open	Closed	2.5 : 1	166 MHz ¹
Closed	Open	60 MHz	30 MHz	7.5 MHz	Open	Closed	Open	3 : 1	180 MHz ¹
Open	Open	66 MHz	33 MHz	8.25 MHz	Open	Closed	Open	3 : 1	200 MHz ¹
Open	Open	66 MHz	33 MHz	8.25 MHz	Open	Closed	Closed	3.5 : 1	233 MHz
Open	Open	66 MHz	33 MHz	8.25 MHz	Closed	Open	Open	4 : 1	266 MHz

- ¹. These processors are not available for these models of HP Vectra PC at the time of printing. This information is provided for completeness only.

The computer may execute erratically, if at all, or may overheat, if it is configured to operate at a higher processor speed than the processor is capable of supporting. This can cause damage to the computer.

Setting the switches to operate at a slower speed, than the processor is capable of supporting, can still cause erratic behavior in some cases, and would reduce the instruction throughput in others.

Cache Memory

The level-2 cache memory is pre-packaged in the processor module. The level-1 cache memory is fabricated on the Pentium II processor chip. Each bank of level-1 cache memory (I-cache and D-cache) has a capacity of 16 KB. The level-2 cache memory has a capacity of 256 KB or 512 KB. The amount of both types of cache memory is set at the time of manufacture, so cannot be changed.

Data is stored in lines of 32-bytes (256 bits). Thus four consecutive 64-bit transfers with the main memory are involved for each transaction.

2 System Board

Devices on the Processor-Local Bus

Main Memory

There are six main memory module sockets, arranged in three banks (A to C). One bank is already occupied by the pair of *single interline memory modules* (SIMMs) that contain the 16 MB or 32 MB of memory that is supplied with the computer.

Different banks can have different capacities (8, 16, 32 or 64 MB), but must be composed of identical pairs of modules (2×4, 2×8, 2×16 or 2×32 MB). By installing a pair of 32 MB SIMMs in every bank, first removing the memory modules that were supplied with the computer, the maximum capacity of 192 MB of main memory can be attained.

The banks can be filled, or left empty, in any order. However, there is a performance advantage to filling the banks in the order A, B, C.

Each bank that is used must contain a pair of identical modules: the same speed (60 or 70 ns), the same width (32-bit or 36-bit), and the same technology (*extended data out*, EDO, or *fast page mode*, FPM). Different banks can contain different speed modules (but the computer will work at the speed of the slowest bank). Different banks can contain different technology modules.

The following table indicates the recommended capacities of main memory.

Operating System	Minimum Memory Capacity	Recommended Memory Capacity
Windows 3.11	4 to 8 MB	12 to 16 MB
Windows 95	8 MB	16 to 24 MB
Windows NT	12 MB	24 to 32 MB
OS/2	4 to 8 MB	16 MB

The *Setup* program automatically detects which memory module capacity, speed, and type is installed in each bank. Individual pages of memory can be configured as cacheable or non-cacheable by software or hardware. They can also be enabled and disabled by hardware or software.

Devices on the PCI Bus

PCI Device	Device Name	Device Number	Function	AD[xx]	Chip-set Interrupt Connection			
					INTA	INTB	INTC	INTD
PL/PCI bridge	PMC	0 (00h)	0	11	—	—	—	—
PCI/ISA bridge	PIIX3	4 (04h)	0	15	—	—	—	—
IDE controller			1		—	—	—	—
USB controller			2		—	—	—	—
Integrated graphics controller	CL 5446	13 (0Dh)	0	24	A	—	—	—
PCI slot #1	J6	7 (07h)	—	18	A	B	C	D
PCI slot #2	J11	10 (0Ah)	—	21	D	A	B	C
PCI slot #3	J5	6 (06h)	—	17	C	D	A	B
PCI slot #4	J12	12 (0Ch)	—	23	B	C	D	A

The distribution of the interrupt lines is described more fully on page 68.

Integrated Drive Electronics (IDE)

The IDE controller is implemented as part of the PIIX3 chip (the PCI/ISA bridge). It is driven from the PCI bus, and has PCI-Master capability. It supports Enhanced IDE (EIDE) and Standard IDE. To use the Enhanced IDE features the drives must be compliant with Enhanced IDE.

Up to four IDE devices are supported: two (one master and one slave) connected to the primary channel, and two (one master and one slave) to the secondary channel. The primary channel is fitted with an IDE cable with two connectors. The secondary channel is fitted with an IDE cable with one or two connectors. If a single drive is attached to a channel, it should be in the master position (this is the connector that is closest to the system board, unless the markings on the cables state otherwise).

It is possible to mix a fast and a slow device, such as a hard disk drive and a CD-ROM, on the same channel without affecting the performance of the fast device. The BIOS sends a command to each drive to determine, automatically, the fastest configuration that it supports. However, in general, the primary channel cable is recommended for hard disk drives, and the secondary channel cable for CD-ROM drives.

2 System Board

Devices on the PCI Bus

Transfer Rates Versus Modes of Operation

The controller supports 32-bit Windows I/O transfers. Five PIO modes, and three DMA modes are supported. The five supported PIO modes allow the following transfer rates.

Mode	0	1	2	3	4
Cycle time (ns)	600	383	240	180	120
Transfer rate (MB/s)	3.33	5.22	8.33	11.1	16.7

The three DMA modes allow the following transfer rates:

Mode	0	1	2
Cycle time (ns)	480	150	120
Transfer rate (MB/s)	4.2	13.3	16.7

Disk Capacity Versus Modes of Addressing

The amount of addressable space on a hard disk is limited by three factors: the physical size of the hard disk, the addressing limit of the IDE hardware, and the addressing limit of the BIOS. The Extended-CHS addressing scheme allows larger disk capacities to be addressed than under CHS, by performing a translation. If the *Setup* field has been set to **extended**, the logical block addressing (LBA) mode will be selected for each device that supports it.

	Cylinders per Device	Heads per Cylinder	Sectors per Track	Bytes per Sector	Bytes per Device
CHS	64	16	1024	512	528 M
ECHS	64	256	1024	512	8.4 G
LBA	-	-	256 M (= 2 ²⁸)	512	137 G

Universal Serial Bus (USB) Controller

The OpenHCI (for USB release 1.0) USB controller is implemented as part of the PIIX3 chip (the PCI/ISA bridge). It is driven from the PCI bus, and provides support for the two stacked USB connectors on the back panel. Over-current detection and protection is provided, but shared between the two ports.

USB works only if the USB interface has been enabled within the HP *Setup* program. Currently, only the Microsoft Windows 95 operating system provides support for the USB.

The Microsoft Supplement 2.1 software, which provides support of the Universal Serial Bus, can be obtained from the Hewlett-Packard World Wide Web site: <http://www.hp.com/go/vectrasupport/>



Devices on the ISA Bus

ISA Device	Index	Data
Super I/O	15Ch	15Dh
Little Ben (HP ASIC)	496h	497h

Super I/O Controller

The *Super I/O* chip (NS 87308) is part of the chip set, and is described on page 24.

The computer is supplied with a Logitech 2-button mouse, and a C3758A keyboard with the following features:

- ☐ Space bar power on, to start the computer from the *Off* state (if **power on from keyboard** is enabled in the *Setup* program).
- ☐ Windows key (next to the  keys), which has the same effect as clicking the “Start” button on the Windows 95 task bar.
- ☐ Pull-down key (next to the right  key), which has the same effect as clicking the right mouse button.

Serial EEPROM

The computer uses 4 Kbit of Serial EEPROM implemented within a single 512 K \times 8-bit ROM chip. Serial EEPROM is ROM in which one byte at a time can be returned to its unprogrammed state by the application of appropriate electrical signals. In effect, it can be made to behave like very slow, non-volatile RAM. It is used for storing the tatoo string, the serial number, and the parameter settings for the *Setup* program.

When installing a new system board, the Serial EEPROM will have a blank serial number field. This will be detected automatically by the BIOS, which will then prompt the user to enter the serial number which is printed on the identification label on the back of the computer.

Flash EEPROM (the System ROM)

The computer uses 256 KB of Flash EEPROM implemented within a single 256 K \times 8-bit ROM chip (or in two 128 K \times 8-bit chips). Flash EEPROM is ROM in which the whole memory can be returned to its unprogrammed state by the application of appropriate electrical signals to its pins. It can then be reprogrammed with the latest firmware.

The System ROM contains: 64 KB of system BIOS (including the boot code, the ISA and PCI initialization, DMI, the *Setup* program and the Power-On Self-Test routines, plus their error messages); 32 KB of video BIOS; 32 KB of Plug-and-Play code; and 32 KB of power management code. The functions of these are summarized in Chapters 4 and 5.

Updating the System ROM

The System ROM can be updated with the latest BIOS. This can be downloaded, as a compressed file, from the *HP Electronic Services*. You must specify the model of the computer since the utility which is supplied for a different model cannot be used with this one. (More information is given in the “Hewlett-Packard Support and Information Services” chapter in the *User's Guide* that was supplied with the computer).

The compressed file, once downloaded, can be executed. This causes it to be expanded out into a number of files, including:

- the Flash EEPROM reprogramming utility program, **phlash.exe**
- the BIOS upgrade file, **HD0700xx.FUL**
- the binary file, **PFMHD106.bin**
- the batch file, **flash.bat**
- a number of ***.txt** files, giving information about the new version of the BIOS, and instructions on how to install it.

The *Phlash* utility must be run from a diskette.

Do not switch off the computer until the system BIOS update procedure has completed, successfully or not, otherwise irrecoverable damage to the ROM may be caused. The control panel switches are automatically disabled to prevent accidental interruption of the flash programming process.

System Board Switches

Five of the *system board switches* (whose location is shown on page 18) set the working frequencies for the computer, as summarized on page 27. The others set the configuration for the computer, as summarized in the following table.

Switch	Functions of the System Board Switches
1-5	Bus frequencies (see the table on page 27)
6	Clear CMOS: Open = normal operation Closed = clear CMOS (to reload the <i>Setup</i> program defaults)
7	Password: Open = normal operation Closed = disabled / clear User and Administrator passwords
8	Keyboard space-bar power-on: Open = disabled Closed = normal operation
9	For test purposes only, do not use: Open = normal operation
10	Product identification: Open = normal operation Closed = clear the product identification field in the CMOS memory

By setting switch SW6 in the **Closed** position, not only is the configuration data cleared (in the CMOS memory and the Serial EEPROM), but also all the Plug-and-Play data that had been saved in the Serial EEPROM. However, the serial number, the tattooing string, the date and the time are each retained.

By setting switch SW8 in the **Closed** position, the Power-On Space-Bar function is enabled. Note, though, that it must *also* be enabled in the **Power-On Space-Bar** field of the Power Menu in the *Setup* program.

Turning the computer on, with switch SW10 in the **Closed** position, clears the product identification field in the BIOS, and causes the computer to prompt for the new information. By identifying the product correctly (after replacing a defective system board by a new one), the BIOS is able to tailor itself for the particular product, and to enable the appropriate features.

2 System Board

Devices on the ISA Bus

Updating the BIOS Before Considering Replacing the System Board

If the computer is faulty, but it starts up correctly, and the fault is not clearly due to the system board hardware, then it is advisable to check the BIOS version number. The BIOS version number can be found from the summary screen, or the *Setup* program, obtained by pressing **[Esc]** or **[F2]**, respectively, when the computer has just been restarted, as described in Chapter 4.

If it is not the current version of the BIOS, the System ROM should be flashed with the new version, as described on the previous page. The computer should then be re-run to see if this has cleared the problem.

Little Ben

Little Ben is an HP application specific integrated circuit (ASIC), designed to be a companion to the Super I/O chip. It interfaces between the chip-set and the processor, and contains the following:

- BIOS timer
 - ☐ hardware wired 50 ms long 880 Hz beep module.
 - ☐ automatic blinker that feeds the LEDs module with a 1 Hz oscillator signal.
- security protection (access, flash and anti-virus protection)
 - ☐ For 128, 256 or 512 KB Flash EEPROMs.
 - ☐ For the Super I/O space: the Serial EEPROM, serial ports, parallel port and mass storage drives (disable write on Flexible Disk Drive, disable boot on any drive, disable use of any embedded drive)
- hard and soft control for the power supply (available with Windows NT and Windows 95, but not with OS/2)
- Advanced power management (APM) version 1.2 (available with Windows 95 and OS/2, but not with Windows NT)
- glue logic (such as programmable chip selects)

The computer can be turned on by typing the space-bar on the keyboard, or when it receives an external signal from a network board. When *VccState* and *PowerGood* pins are both low, all output pins are in tri-state mode, except for *RemoteOnBen* which continues to be driven. The power consumption has been kept as low as possible. This allows the computer to be powered from the standby power supply, and to be restarted even after a power loss has occurred.

When the user requests a ShutDown from the operating system, the environment is first cleared. Any request to turn off the computer, from the control panel, or from the operating system, can only be granted if the computer is not locked by Little Ben's lock bit (otherwise the power remains on, a red light is illuminated, and the buzzer is sounded).

Other PCI and ISA Accessory Devices Under Plug and Play

Plug and Play is an industry standard for automatically configuring the computer's hardware. When you start the computer, the Plug and Play system BIOS can detect automatically which hardware resources (IRQs, DMAs, memory ranges, and I/O addresses) are used by the system-based components.

All PCI accessory boards are Plug and Play, although not all ISA boards are. Check the accessory board's documentation if you are unsure.

The computer is PCI 2.1 compliant, and PnP 1.1 compliant. Accessory boards which are Plug and Play are automatically configured by the BIOS.

In general, in a Plug and Play configuration, resources for an ISA board have to be reserved first, and then you can plug in your board. If you want to install an ISA board when running a non Plug-and-Play operating system, such as Windows for Workgroups, you have to reserve the resources for the board using the ICU (ISA configuration utility). Failure to do so may lead to resource conflicts.

2 System Board

Devices on the ISA Bus

Interface Devices and Mass-Storage Drives

This chapter describes the graphics, mass storage and audio devices which are supplied with the computer. It also summarizes the pin connections on the internal and external connectors.

Cirrus 5446 Graphics Controller Chip

Some models are supplied with a graphics controller chip integrated on the system board (all other models are supplied with a Matrox Millennium II PCI graphics controller on a board fitted in a PCI accessory slot, as described in the next section of this chapter). The Cirrus Logic CL-GD5446, can be characterized as follows:

- 100% hardware- and BIOS-compatible with IBM[®] VGA display standard
- 64-bit video memory access with 2 MB, 50 ns, EDO, video DRAM (this is not upgradeable since it is already fitted to capacity).
- Hardware acceleration of graphical user interface (GUI) operations through a bit-block transfer mechanism
- Support for up to 4 MB, 50 ns EDO video DRAM (though space is only provided on the system board for 2 MB)
- Integrated 24-bit, 135 MHz RAMDAC
- Integrated programmable, dual-clock synthesizer
- Green power saving features
- Standard and Enhanced Video Graphics Array (VGA) modes
- Acceleration for playback, continuous interpolation on X, continuous interpolation on Y
- DDC 2B compliant.
- Superior TV-like quality video performance: hardware video window; YUV video support; color key, chroma key; X & Y interpolated zooming.

Connectors

The Video Electronics Standards Association (VESA) defines a standard video connector, variously known as the VESA *feature* connector, *auxiliary* connector, or *pass-through* connector. The graphics controller supports an input/output VESA *feature* connector. This connector (whose pin names are listed in a table on page 51) is integrated on the system board, and is connected directly to the pixel data bus and the synchronization signals.

Video Memory

The video RAM (also known as the frame buffer) is a local block of 50 ns EDO DRAM for holding both the on-screen surface (reflecting what is currently displayed on the screen), and the off-screen surface (video frame, fonts, double buffer).

Video Modes

The following table details the standard VGA modes which are currently implemented in the video BIOS. These modes are supported by standard BIOS functions; that is, the video BIOS (which is mapped contiguously in the address range C0000h to C7FFFh) contains all the routines required to configure and access the graphics subsystem.

Standard VGA Modes

Mode No.	Standard	Interface Type	Resolution	No. of Colors	Vertical Refresh	Horizontal Refresh	Notes
00h, 01h 02h, 03h	CGA CGA	text text	360 x 400 720 x 400	16/256K 16/256K	70 Hz 70 Hz	31.5 kHz 31.5 kHz	
04h, 05h 06h	CGA CGA	graphics graphics	320 x 200 640 x 200	4/256K 2/256K	70 Hz 70 Hz	31.5 kHz 31.5 kHz	
07h	MDA	text	720 x 400	monochrome	70 Hz	31.5 kHz	
0Dh 0Eh 0Fh 10h	EGA EGA EGA EGA	graphics graphics graphics graphics	320 x 200 640 x 200 640 x 350 640 x 350	16/256K 16/256K monochrome 16/256K	70 Hz 70 Hz 70 Hz 70 Hz	31.5 kHz 31.5 kHz 31.5 kHz 31.5 kHz	
11h 11h + 11h + 12h 12h + 12h + 12h + 12h + 13h	VGA VGA VGA VGA VGA VGA VGA VGA VGA	graphics graphics graphics graphics graphics graphics graphics graphics graphics	640 x 480 640 x 480 640 x 480 640 x 480 640 x 480 640 x 480 640 x 480 640 x 480 320 x 200	2/256K 2/256K 2/256K 16/256K 16/256K 16/256K 16/256K 16/256K 256/256K	60 Hz 72 Hz 75 Hz 60 Hz 72 Hz 75 Hz 85 Hz 70 Hz	31.5 kHz 37.9 kHz 37.5 kHz 31.5 kHz 37.9 kHz 37.5 kHz 43.3 kHz 31.5 kHz	

3 Interface Devices and Mass-Storage Drives

Cirrus 5446 Graphics Controller Chip

Extended Video Modes

Extended Mode No.	VESA Mode No.	Interface Type	Resolution	No. of Colors	Vertical Refresh	Horizontal Refresh	Notes
58h, 6Ah 58h, 6Ah 58h, 6Ah 58h, 6Ah	102h 102h 102h ergo 102h ergo	graphics graphics graphics graphics	800 x 600 800 x 600 800 x 600 800 x 600	16/256K 16/256K 16/256K 16/256K	56 Hz 60 Hz 72 Hz 75 Hz	35.2 kHz 37.8 kHz 48.1 kHz 46.9 kHz	
5Ch 5Ch 5Ch 5Ch 5Ch	103h 103h 103h ergo 103h ergo 103h ergo	graphics graphics graphics graphics graphics	800 x 600 800 x 600 800 x 600 800 x 600 800 x 600	256/256K 256/256K 256/256K 256/256K 256/256K	56 Hz 60 Hz 72 Hz 75 Hz 85 Hz	35.2 kHz 37.9 kHz 48.1 kHz 46.9 kHz 53.7 kHz	
5Dh i 5Dh 5Dh 5Dh 5Dh	104h 104h 104h 104h 104h ergo	graphics graphics graphics graphics graphics	1024 x 768 1024 x 768 1024 x 768 1024 x 768 1024 x 768	16/256K 16/256K 16/256K 16/256K 16/256K	43 Hz i 60 Hz 70 Hz 72 Hz 75 Hz	35.5 kHz 48.3 Hz 56 kHz 58 kHz 60 kHz	interlaced
5Eh	100h	graphics	640 x 400	256/256K	70 Hz	31.5 kHz	
5Fh 5Fh 5Fh 5Fh	101h 101h ergo 101h ergo 101h ergo	graphics graphics graphics graphics	640 x 480 640 x 480 640 x 480 640 x 480	256/256K 256/256K 256/256K 256/256K	60 Hz 72 Hz 75 Hz 85 Hz	31.5 kHz 37.9 kHz 37.5 kHz 43.3 kHz	
60h i 60h 60h 60h 60h 60h d	105h 105h 105h 105h 105h ergo 105h ergo	graphics graphics graphics graphics graphics graphics	1024 x 768 1024 x 768 1024 x 768 1024 x 768 1024 x 768 1024 x 768	256/256K 256/256K 256/256K 256/256K 256/256K 256/256K	43 Hz i 60 Hz 70 Hz 72 Hz 75 Hz 85 Hz	35.5 kHz 48.3 kHz 56 kHz 58 kHz 60 kHz 68.3 kHz	interlaced clock-doubled 8 bpp
64h 64h 64h 64h	111h 111h ergo 111h ergo 111h ergo	graphics graphics graphics graphics	640 x 480 640 x 480 640 x 480 640 x 480	65,536 65,536 65,536 65,536	60 Hz 72 Hz 75 Hz 85 Hz	31.5 kHz 37.9 kHz 37.5 kHz 43.3 kHz	
65h 65h 65h 65h 65h	114h 114h 114h ergo 114h ergo 114h ergo	graphics graphics graphics graphics graphics	800 x 600 800 x 600 800 x 600 800 x 600 800 x 600	65,536 65,536 65,536 65,536 65,536	56 Hz 60 Hz 72 Hz 75 Hz 85 Hz	35.2 kHz 37.8 kHz 48.1 kHz 46.9 kHz 53.7 kHz	
66h 66h 66h 66h	110h 110h ergo 110h ergo 110h ergo	graphics graphics graphics graphics	640 x 480 640 x 480 640 x 480 640 x 480	32,768 32,768 32,768 32,768	60 Hz 72 Hz 75 Hz 85 Hz	31.5 kHz 37.8 kHz 37.5 kHz 43.3 kHz	
67h 67h 67h 67h 67h	113h 113h 113h ergo 113h ergo 113h ergo	graphics graphics graphics graphics graphics	800 x 600 800 x 600 800 x 600 800 x 600 800 x 600	32,768 32,768 32,768 32,768 32,768	56 Hz 60 Hz 72 Hz 75 Hz 85 Hz	35.2 kHz 37.8 kHz 48.1 kHz 46.9 kHz 53.7 kHz	

3 Interface Devices and Mass-Storage Drives

Cirrus 5446 Graphics Controller Chip

Extended Mode No.	VESA Mode No.	Interface Type	Resolution	No. of Colors	Vertical Refresh	Horizontal Refresh	Notes
68h i 68h 68h 68h 68h	116h 116h 116h ergo 116h ergo 116h ergo	graphics graphics graphics graphics graphics	1024 x 768 1024 x 768 1024 x 768 1024 x 768 1024 x 768	32,768 32,768 32,768 32,768 32,768	43 Hz i 60 Hz 70 Hz 75 Hz 85 Hz	35.5 kHz 48.3 kHz 56 kHz 60 kHz 68.3 kHz	interlaced non Vesa timing
69h i	119h	graphics	1280 x 1024	32,768	43 Hz i	48 kHz	interlaced
6Ch i	106h	graphics	1280 x 1024	16/256K	43 Hz i	48 kHz	interlaced
6Dh i 6Dh d 6Dh d 6Dh d	107h 107h 107h ergo 107h ergo	graphics graphics graphics graphics	1280 x 1024 1280 x 1024 1280 x 1024 1280 x 1024	256/256K 256/256K 256/256K 256/256K	43 Hz i 60 Hz 71.2 Hz 75 Hz	48 kHz 65 kHz 76 kHz 80 kHz	interlaced clock-doubled clock-doubled clock-doubled
71h 71h 71h 71h	112h 112h 112h 112h	graphics graphics graphics graphics	640 x 480 640 x 480 640 x 480 640 x 480	16.7 M 16.7 M 16.7 M 16.7 M	60 Hz 72 Hz 75 Hz 85 Hz	31.5 kHz 37.8 kHz 37.5kHz 43.3 kHz	
74h i 74h 74h 74h 74h	117h 117h 117h ergo 117h ergo 117h ergo	graphics graphics graphics graphics graphics	1024 x 768 1024 x 768 1024 x 768 1024 x 768 1024 x 768	65,536 65,536 65,536 65,536 65,536	43 Hz i 60 Hz 70 Hz 75 Hz 85 Hz	35.5 kHz 48.3 kHz 56 kHz 60 kHz 68.3 kHz	interlaced non Vesa timing
75h i	11Ah	graphics	1280 x 1024	65,536	43 Hz i	48 kHz	interlaced
78h 78h 78h 78h 78h	115h 115h 115h 115h 115h	graphics graphics graphics graphics graphics	800 x 600 800 x 600 800 x 600 800 x 600 800 x 600	16.7 M 16.7 M 16.7 M 16.7 M 16.7 M	56 Hz 60 Hz 72 Hz 75 Hz 85 Hz	35.2 kHz 37.8 kHz 48.1 kHz 46.9 kHz 53.7 kHz	
79h i 79h 79h 79h 79h	118h 118h 118h ergo 118h ergo 118h ergo	graphics graphics graphics graphics graphics	1024 x 768 1024 x 768 1024 x 768 1024 x 768 1024 x 768	16.7 M 16.7 M 16.7 M 16.7 M 16.7 M	43 Hz i 60 Hz 70 Hz 75 Hz 85 Hz	35.5 kHz 48.3 kHz 56 kHz 60 kHz 68.3 kHz	interlaced non Vesa timing
7Ch d 7Ch d	- -	graphics graphics	1152 x 864 1152 x 864	256/256K 256/256K	70 Hz 75 Hz	63.9 kHz 67.5 kHz	clock-doubled clock-doubled 8 bpp

The “non Vesa timing”, on modes 68h, 74h and 79h, arises because the VESA pixel frequency on the 5446 is 87.7 MHz, as opposed to 94.5 MHz. This should not present major problems; most of the displays that can support such video modes are high end displays that use micro-controller based electronics.

3 Interface Devices and Mass-Storage Drives

Cirrus 5446 Graphics Controller Chip

Available Video Resolutions

The number of colors supported is limited by the graphics device and the video memory. The resolution/color/refresh-rate combination is limited by a combination of the display driver, the graphics device, and the video memory. If the resolution/refresh-rate combination is set higher than the display can support, you risk damaging the display.

The following table lists the video resolutions that are available from the BIOS:

Resolution	Number of colors	Refresh Rate (Hz)	Memory
640 x 480	16, 256, 32K, 64K, 16M	60, 72, 75, 85	1 MB
800 x 600	16	56, 60, 72, 75	
	256, 32K, 64K	56, 60, 72, 75, 85	
1024 x 768	16	i87 ¹ , 60, 70, 75	
	256	i87 ¹ , 60, 70, 75, 85	
1280 x 1024	16	i87 ¹	
800 x 600	16M	56, 60, 72, 75, 85	2 MB (additional modes available)
1024 x 768	64K	i87 ¹ , 60, 70, 75, 85	
1280 x 1024	256	i87 ¹ , 60, 72, 75	

¹. Interlaced.

The table, on the following page, lists the available video resolutions using the current drivers. The available resolutions may be different with later versions of each of these drivers.

	Resolution	Number of colors	Refresh Rate (Hz)	Memory
Windows NT	640 x 480	16, 256, 32K, 64K, 16M	60, 75, 85	1 MB
	800 x 600	16	56, 60, 72, 75	
		256, 64K	56, 60, 72, 75, 85	
	1024 x 768	16	i87 ¹ , 60, 70, 75	
		256	i87 ¹ , 60, 70, 75, 85	
	1280 x 1024	16	i87 ¹	
	800 x 600	16M	60, 72, 75, 85	2 MB
	1024 x 768	64K	i87 ¹ , 60, 70, 75, 85	
	1280 x 1024	256	i87 ¹ , 60, 72, 75	

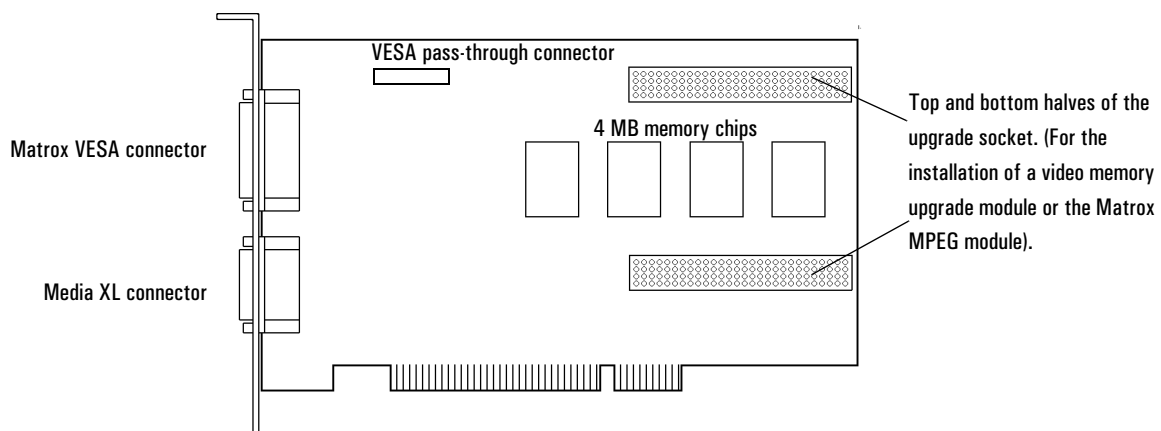
	Resolution	Number of colors	Refresh Rate (Hz)	Memory
Windows 95	640 x 480	16, 256, 64K, 16M	60, 72, 75, 85	1 MB
	800 x 600	16	56, 60, 72, 75	
		256, 64K	56, 60, 72, 75, 85	
	1024 x 768	256	i87 ¹ , 60, 70, 75, 85	2 MB (additional modes available)
	800 x 600	16M	56, 60, 72, 75, 85	
	1024 x 768	64K	i87 ¹ , 60, 70, 75, 85	
OS/2	1280 x 1024	256	i87 ¹ , 60, 72, 75	2 MB (additional modes available)
	640 x 480	256, 64K	60, 72, 75, 85	
	800 x 600	256, 64K	56, 60, 72, 75, 85	
	1024 x 768	256	i87 ¹ , 60, 70, 75, 85	
	1024 x 768	64K	i87 ¹ , 60, 70, 75, 85	
	1280 x 1024	256	i87 ¹ , 60, 72, 75	

¹. Interlaced.

Matrox MGA Millennium II Graphics Controller Board

Some models are supplied with a Matrox MGA Millennium PCI graphics controller on a board fitted in a PCI accessory slot. The on-board MGA-2064W processor communicates with the Pentium II processor along the PCI bus. The controller can be characterized as follows:

- 100% hardware- and BIOS-compatible with IBM[®] VGA display standard
- 64-bit video memory access
- Hardware acceleration of graphical user interface (GUI) operations
- Support for up to 8 MB Window RAM (WRAM) at 50 ns
- Integrated 24-bit, 220 MHz RAMDAC
- Pixel clock maximum frequency of 135 MHz
- Green power saving features
- Standard and Enhanced Video Graphics Array (VGA) modes
- Acceleration for 3D, playback, MPEG (when an optional upgrade module from Matrox is fitted), continuous interpolation on X, replication on Y
- DDC 2B compliant.



Connectors

The Video Electronics Standards Association (VESA) defines a standard video connector, variously known as the VESA *feature* connector, *auxiliary* connector, or *pass-through* connector. The video controller supports an output-only VESA *feature* connector in VGA mode. This connector (whose pin names are listed in a table on page 51) is integrated on the PCI board, is connected directly to the pixel data bus and the synchronization signals, and is automatically enabled all of the time.

There are two connectors on the back panel: the normal DB15 VGA connector, for connecting to HP displays, and a Media XL connector (used by the MPEG accessory, not supported by HP). The layout of the pins for the DB15 VGA connector are shown on page 55.

If you install a VESA-standard video accessory board that uses the MGA video adapter, connect the accessory board's cable to the VESA pass-through connector on the board.

Video Memory

The video memory (also known as window RAM, or WRAM) is a local block of RAM for holding two major data structures: the double buffer (to hold one frame steady on the screen whilst the next one is being processed), and the Z-buffer (for storing depth information for each pixel). It is dual ported, so that it can be inputting and outputting simultaneously. There is also hardware support for Gouraud shading, Phong shading and texture mapping.

The Matrox MGA Millennium graphics controller board is supplied with 4 MB of video memory. This can be upgraded with an HP upgrade module. The upgrade socket can alternatively be used for the installation of the Matrox MGA Media XL upgrade module (also ordered from Matrox) to support MPEG.

Available Video Resolutions

The number of colors supported is limited by the graphics device and the video memory. The resolution/color/refresh-rate combination is limited by a combination of the display driver, the graphics device, and the video memory. If the resolution/refresh-rate combination is set higher than the display can support, you risk damaging the display.

3 Interface Devices and Mass-Storage Drives

Matrox MGA Millennium II Graphics Controller Board

Resolution	Number of colors	Maximum Refresh Rate (Hz)	Memory
640 x 480	256, 64K, 16M	200	2 MB
800 x 600	256, 64K, 16M		
1024 x 768	256, 64K	120	
1280 x 1024	256	110	
1600 x 1200	256	85	
640 x 480	256, 64K, 16M	200	4 MB
800 x 600	256, 64K, 16M		
1024 x 768	256, 64K, 16M	120	
1280 x 1024	256, 64K, 16M (24 bpp)	110	
1600 x 1200	256, 64K	85	
640 x 480	256, 64K, 16M	200	8 MB
800 x 600	256, 64K, 16M		
1024 x 768	256, 64K, 16M	120	
1280 x 1024	256, 64K, 16M	110	
1600 x 1200	256, 64K, 16M (24 bpp)	85	

The table below summarizes the 2D video resolutions which are supported. Note, though, SCO Unix only supports 15 bpp (bits per pixel), instead of 16 bpp, and does not support 32 bpp; OS/2 does not support 24 bpp.

Number of Colors	256	64 K Hi-Color	16.7 M True-Color	16.7 M True-Color
Bits per Pixel	8	16	24	32
640 × 480	2 MB, 200 Hz			
800 × 600	2 MB, 200 Hz			
1024 × 768	2 MB, 120 Hz		4 MB, 120Hz	
1152 × 882 ¹	2 MB, 120 Hz		4 MB, 120 Hz	
1280 × 1024	2 MB, 110 Hz	4 MB, 110 Hz		8 MB, 110 Hz
1600 × 120	2 MB, 85 Hz	4 MB, 85 Hz	8 MB, 85 Hz	Not supported

¹.1152 × 882 is not preset on HP displays

The maximum 2D resolutions for any given video memory capacity and color scale can be found from the following table:

Number of Colors	256	64 K Hi-Color	16.7 M True-Color	16.7 M True-Color
Bits per Pixel	8	16	24	32
2 MB	1600 X 1200	1024 X 768	800 X 600	800 X 600
4 MB	1600 X 1200	1600 X 1200	1280 X 1024	1152 X 882 ¹
8 MB	1600 X 1200	1600 X 1200	1600 X 1200	Not supported

¹. 1152 X 882 is not preset on HP displays

Video BIOS

The board has a flash video BIOS that can be updated like a system BIOS, using a flash utility. This is achieved as follows:

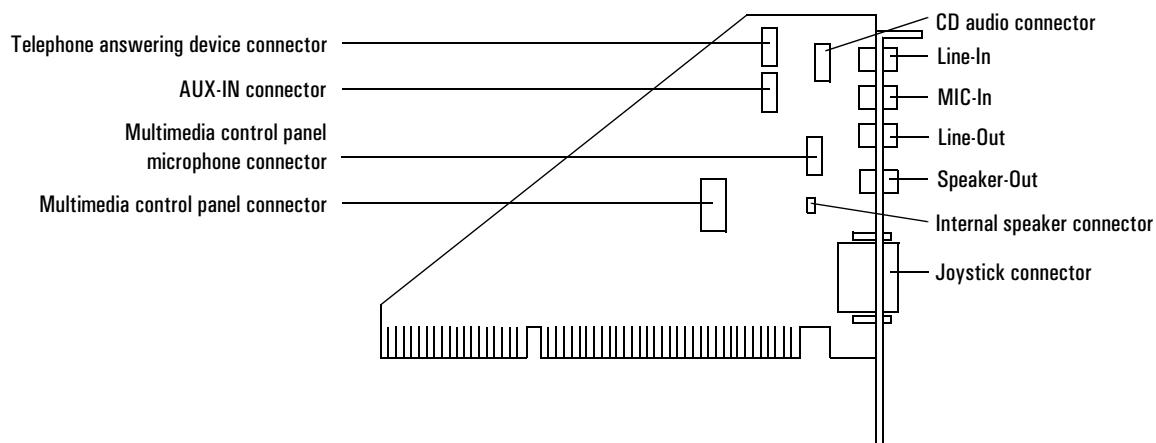
- 1 Create a DOS boot diskette, and copy the following files to it:
 - xxxxxxxx.bin (a binary file whose name depends on the version)
 - dos4gw.exe
 - progbios.exe
 - updbios.bat
- 2 Switch off the PC, insert the boot diskette, and switch on the PC.
- 3 Run the **updbios.bat** command file or **progbios.exe -i *.bin**.
- 4 Switch off the PC, and take out the boot diskette, and switch on the PC.

Executing **progbios.exe -d** allows the BIOS revision date to be checked. The video BIOS revision number can be checked by clicking on the MGA control panel.

Audio Controller

The Creative Labs CT2970 SoundBlaster 16 audio interface, supplied on some models in an ISA slot, can be summarized as follows:

- line-out (stereo) jack: 20 Hz to 20 kHz frequency response, 83 dB signal to noise ratio, 0.2% total harmonic distortion
- headphones jack: 2 W PMPO per channel, 32 Ω load
- speaker connector: 0.2% total harmonic distortion
- line-in (stereo) jack: 15 k Ω , 0 V to 2 V peak-to-peak
- CD audio-in connector: 15 k Ω , 0 V to 2 V peak-to-peak
- microphone input: 600 Ω , dynamic, 30 mV to 200 mV peak-to-peak
- MIDI /joystick interface connector: MPU-401 UART compatible
- 8-bit and 16-bit stereo sampling: 5 kHz to 44.1 kHz
- Creative OPL3 synthesizer: 20 polyphonic voices
- typical electrical current: +5 V (250 mA), +12 V (250 mA), -12 V (50 mA)



The board is compliant with Microsoft PC 95 revised / PC 96. It has a full duplex codec, and supports a volume control on the front panel.

Drivers

Drivers for the audio board, working with the Windows NT operating system, are supplied with the computer. These are required since the board is Plug-and-Play, but the operating system is not. It is the user's responsibility to avoid conflicts with other devices using the same resources (such as IRQ, DMA and I/O lines). The user can use the configuration manager to change the board settings, choosing either the default configuration, or changes to any of the parameters.

Mass-Storage Drives

The IDE controller is described on page 29. The flexible disk controller is described on page 20.

Hard Disk Drives

A 3.5-inch hard disk drive is supplied on an internal shelf in some models.

	4.0 GB IDE	2.5 GB IDE
HP product number	D2687-69001	D2786-69001
Manufacturer	Quantum	Quantum
Product name		Fireball TM 2550

Flexible Disk Drives

A 3.5-inch, 1.44 MB flexible disk drive (D2035B) is supplied on the top front-access shelf of all minitower models. Desktop models are supplied with the new bezelless version of the drive (D2035-63162) mounted vertically on the right hand side of the front panel.

CD-ROM Drives

Most models have a 24× Max IDE CD-ROM drive (D4383A) supplied in a 5.25-inch front-access shelf.

	24× Max IDE
HP product number	D4383A
Manufacturer	Hitachi
Product name	
Formatted storage capacity	650 MB

If a disk is still in the drive after power failure or drive failure, the disk can be reclaimed by inserting a stout wire, such as the end of a straightened paper-clip, into the small hole at the bottom of the door.

In order to allow correct CD-ROM drive detection by the *Setup* program, leave the device configuration jumper on the rear connector in the cable select (CS) or master (MA) positions.

Connectors and Sockets

IDE Hard Disk Drive Data Connector			
Pin	Signal	Pin	Signal
1	Reset#	2	Ground
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	Ground	20	orientation key
21	DMARQ	22	Ground
23	DIOW#	24	Ground
25	DIOR#	26	Ground
27	IORDY	28	SPSYNC:CSEL
29	DMACK#	30	Ground
31	INTRQ	32	IOCS16#
33	DA1	34	PDIAG#
35	DA0	36	DA2
37	CS0#	38	CS1#
39	DASP#	40	Ground

Flexible Disk Drive Data Connector			
Pin	Signal	Pin	Signal
1	Ground	2	LDENSEL#
3	Ground	4	Microfloppy
5	Ground	6	EDENSEL
7	Ground	8	INDX#
9	Ground	10	MTEN1#
11	Ground	12	DRSEL0#
13	Ground	14	DRSEL1#
15	Ground	16	DTEN0#
17	Ground	18	DIR#
19	Ground	20	STP#
21	Ground	22	WRDATA#
23	Ground	24	WREN#
25	Ground	26	TRK0#
27	Ground	28	WRPRDT#
29	Ground	30	RDDATA#
31	Ground	32	HDSEL1#
33	Ground	34	DSKCHG#

Status Panel Connector			
Pin	Signal	Pin	Signal
1	LCK_LED_K	2	LCK_LED_A
3	PWR_LED_K	4	PWR_LED_A
5	not connected	6	common
7	Push_On	8	RED_LED_A
9	HDD_LED_K	10	HDD_LED_A
11	_Reset	12	Ground
13	LCK_PUSH2	14	LCK_PUSH2

External Start and Remote Start Connectors			
Pin	Signal	Pin	Signal
1	ExternalStart	2	Ground
3	Wake1#	4	Wake2#
5	not connected	6	Wake3#
7	PowerGood	8	not connected
9	Vstandby	10	orientation key

3 Interface Devices and Mass-Storage Drives

Connectors and Sockets

Audio Board Connectors

Wavetable Connector			
Pin	Signal	Pin	Signal
1	Ground	2	not connected
3	Ground	4	MIDI input
5	Ground	6	Vcc
7	Ground	8	MIDI output
9	Ground	10	Vcc
11	Ground	12	not connected
13	not connected	14	Vcc
15	Ground	16	not connected
17	Ground	18	+12 V
19	Ground	20	Line-in (right)
21	Ground	22	-12 V
23	Ground	24	Line-in (left)
25	Ground	26	Reset B

Int. Speaker Connector	
Pin	Signal
1	Power signal out
2	Analog ground

Modem Connector			
Pin	Signal	Pin	Signal
1	Analog ground	2	orientation key
3	Line-in	4	Analog ground
5	Line-out (left)	6	Analog ground
7	Line-out (right)	8	Modem speaker
9	Analog ground	10	Microphone in

Goldfinch Connector			
Pin	Signal	Pin	Signal
1	Line-in (right)	2	Analog ground
3	Line-in (left)	4	Analog ground
5	orientation key	6	Analog ground
7	Analog ground	8	Analog ground

Aux2 MPEG Connector	
Pin	Signal
1	Left channel
2	Ground
3	Ground
4	Right channel

CD Audio Connector	
Pin	Signal
1	Ground
2	Left channel
3	Ground
4	Right channel

Front Panel Connector			
Pin	Signal	Pin	Signal
1	Ground	2	orientation key
3	Headphones left	4	Head return left
5	Headphones right	6	Head return right
7	Volume low limit	8	Volume DC cntl
9	Volume high limit	10	not used

Microphone Connector	
Pin	Signal
3	Signal and power
2	Ground
1	Signal and power

2nd ring:
3rd ring:
1st ring:

3 Interface Devices and Mass-Storage Drives

Connectors and Sockets

PCI Connector							
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	-12 V	A1	TRST#	B47	AD[12]	A47	AD[11]
B2	TCK	A2	+12 V	B48	AD[10]	A48	Ground
B3	Ground	A3	TMS	B49	+3.3 V	A49	AD[09]
B4	TDO	A4	TDI	B50	AD[08]	A50	C/BE#[0]
B5	+5 V	A5	+5 V	B51	AD[07]	A51	+3.3 V
B6	+5 V	A6	INTA#	B52	Ground	A52	AD[06]
B7	INTB#	A7	INTC#	B53	AD[05]	A53	AD[04]
B8	INTD#	A8	+5 V	B54	AD[03]	A54	Ground
B9	Ground	A9	reserved	B55	Ground	A55	AD[02]
B10	reserved	A10	PRSENT#	B56	AD[01]	A56	AD[00]
B11	+3.3 V	A11	reserved	B57	+5 V	A57	+5 V
	orientation key		orientation key	B58	+5 V	A58	+5 V
B12	reserved	A12	reserved	B59	+5 V	A59	+5 V
B13	Ground	A13	RESET#	B60	ACK64#	A60	REQ64#
B14	CLK	A14	+3.3 V		orientation key		orientation key
B15	Ground	A15	GNT#	B61	reserved	A61	Ground
B16	REQ#	A16	Ground	B62	Ground	A62	C/BE#[7]
B17	+3.3 V	A17	reserved	B63	C/BE#[5]	A63	C/BE#[6]
B18	AD[31]	A18	AD[30]	B64	C/BE#[4]	A64	+3.3 V
B19	AD[29]	A19	Ground	B65	Ground	A65	PAR64
B20	Ground	A20	AD[28]	B66	AD[63]	A66	AD[62]
B21	AD[27]	A21	AD[26]	B67	AD[61]	A67	Ground
B22	AD[25]	A22	+3.3 V	B68	+3.3 V	A68	AD[60]
B23	Ground	A23	AD[24]	B69	AD[59]	A69	AD[58]
B24	C/BE#[3]	A24	IDSEL	B70	AD[57]	A70	Ground
B25	AD[23]	A25	Ground	B71	Ground	A71	AD[56]
B26	+3.3 V	A26	AD[22]	B72	AD[55]	A72	AD[54]
B27	AD[21]	A27	AD[20]	B73	AD[53]	A73	+3.3 V
B28	AD[19]	A28	Ground	B74	Ground	A74	AD[52]
B29	Ground	A29	AD[18]	B75	AD[51]	A75	AD[50]
B30	AD[17]	A30	AD[16]	B76	AD[49]	A76	Ground
B31	C/BE#[2]	A31	+3.3 V	B77	+3.3 V	A77	AD[48]
B32	Ground	A32	FRAME#	B78	AD[47]	A78	AD[46]
B33	IRDY#	A33	Ground	B79	AD[45]	A79	Ground
B34	+3.3 V	A34	TRDY#	B80	Ground	A80	AD[44]
B35	DEVSEL#	A35	Ground	B81	AD[43]	A81	AD[42]
B36	Ground	A36	STOP#	B82	AD[41]	A82	+3.3 V
B37	LOCK#	A37	+3.3 V	B83	Ground	A83	AD[40]
B38	PERR#	A38	SDONE	B84	AD[39]	A84	AD[38]
B39	Ground	A39	SB0#	B85	AD[37]	A85	Ground
B40	SERR#	A40	Ground	B86	+3.3 V	A86	AD[36]
B41	+3.3 V	A41	C/BE#[1]	B87	AD[35]	A87	AD[34]
B42	AD[15]	A42	PAR	B88	AD[33]	A88	Ground
B43	+3.3 V	A43	+3.3 V	B89	Ground	A89	AD[32]
B44	+3.3 V	A44	+3.3 V	B90	reserved	A90	reserved
B45	AD[14]	A45	+3.3 V	B91	reserved	A91	Ground
B46	Ground	A46	AD[13]	B92	Ground	A92	reserved

3 Interface Devices and Mass-Storage Drives

Connectors and Sockets

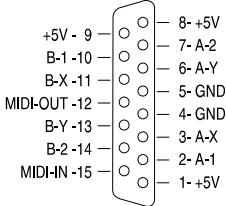
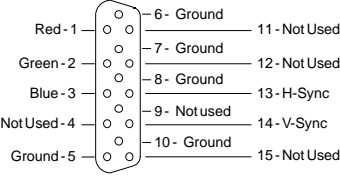
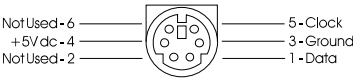
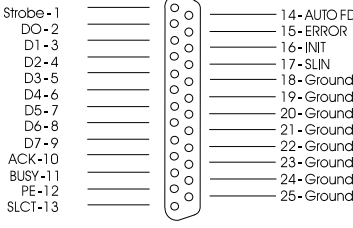
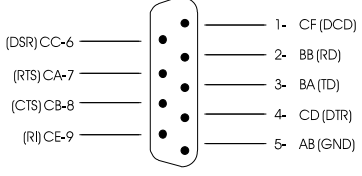
16-bit ISA Connector (8-bit ISA uses the A and B connectors)			
Pin	Signal	Pin	Signal
B1	Ground	A1	CHCHK#
B2	RESDRV	A2	SD7
B3	+5 V	A3	SD6
B4	IRQ9	A4	SD5
B5	-5 V	A5	SD4
B6	DRQ2	A6	SD3
B7	-12 V	A7	SD2
B8	NOWS#	A8	SD1
B9	+ 12 V	A9	SD0
B10	Ground	A10	CHRDY
B11	SMWTC#	A11	AENx
B12	SMRDC#	A12	SA19
B13	IOWC#	A13	SA18
B14	IORC#	A14	SA17
B15	DEK3#	A15	SA16
B16	DRQ3	A16	SA15
B17	DAK1#	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH#	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DAK2#	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	+5 V	A29	SA2
B30	OSC	A30	SA1
B31	Ground	A31	SA0
D1	M16#	C1	SBHE#
D2	IO16#	C2	LA23
D3	IRQ10	C3	LA22
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DAK0#	C8	LA17
D9	DRQ0	C9	MRDC#
D10	DAK5#	C10	MWTC#
D11	DRQ5	C11	SD8
D12	DAK6#	C12	SD9
D13	DRQ6	C13	SD10
D14	DAK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5 V	C16	SD13
D17	MASTER16#	C17	SD14
D18	Ground	C18	SD15

Power Supply Connector for System Board			
Pin	Signal	Pin	Signal
1	PwrGood	13	Remote_On
2	VSTDBY	14	-5 V supply
3	+5 V supply	15	-12 V supply
4	+5 V supply	16	+12 V supply
5	+5 V supply	17	Ground
6	+5 V supply	18	Ground
7	+5 V supply	19	Ground
8	+3.3 V supply	20	Ground
9	+3.3 V supply	21	Ground
10	+3.3 V supply	22	Ground
11	+3.3 V supply	23	Ground
12	+3.3 V supply	24	Ground

Battery Pack Connector	
Pin	Signal
1	VBATT
2	orientation key
3	not connected
4	Ground

USB Connector	
Pin	Signal
1	Vcc
2	Data —
3	Data +
4	Ground

Socket Pin Layouts

<div><h3>MIDI Connector</h3></div>	<div><h3>VGA Connector</h3></div>
<div><h3>Keyboard and Mouse Connector</h3></div>	<div><h3>Parallel Port Connector</h3></div>
<div><h3>Serial Port Connector</h3></div>	

3 Interface Devices and Mass-Storage Drives

Connectors and Sockets

Summary of the HP/Phoenix BIOS

The *Setup* program and HP/Phoenix BIOS are summarized in this chapter. The POST routines are described in the next chapter.

HP/Phoenix BIOS Summary

The System ROM contains the POST (power-on self-test) routines, and the BIOS: the System BIOS, video BIOS (for models with an integrated video controller), and low option ROM. This chapter, and the following one, give an overview of the following aspects:

- menu-driven *Setup* with context-sensitive help (in US English only), described next in this chapter.
- The address space, with details of the interrupts used, described at the end of this chapter.
- The Power-On-Self-Test or POST, which is the sequence of tests the computer performs to ensure that the system is functioning correctly, described in the next chapter.

The system BIOS is identified by the version number **HD.07.xx**. The procedure for updating the System ROM firmware is described on page 32.

Press **(F2)**, to run the *Setup* program, while the initial “Vectra” logo is being displayed immediately after restarting the PC. Alternatively, press **(Esc)** to view the summary configuration screen, an example of which is depicted on the next page. By default, this remains on the screen for 20 seconds, but by pressing **(F5)** once, it can be held on the screen indefinitely until **(F1)** is pressed again. Pressing **(F10)** will cause the computer to be turned off.

VL6/266 — Copyright 1997 Hewlett-Packard — HD.07.xx			
Any line of text can be entered here as a 'tattoo' for the computer			
BIOS version	HD.07.xx	PC Serial Number	FR54011111
CPU Date Code	N/A	LAN MAC address	not available
System RAM	: 32 MB	Processor type	: Pentium II
Bank A	: 32 MB (EDO)	COM1	: 3F8H (Serial A)
Bank B	: None	COM2	: 2F8H (Serial B)
Bank C	: None	COM3	: None
Video RAM	: Not available	COM4	: None
System Cache	: 512KB (Synchronous)	LPT1	: 378H
Video Device	: Matrox (External)	LPT2	: None
1st IDE Device	: HDD 2500 MB	LPT3	: None
2nd IDE Device	: None	Flexible Disk A	: 1.44 MB
3rd IDE Device	: CD-ROM	Flexible Disk B	: None
4th IDE Device	: None	Display type	: Not Available
ISA PnP	: Not Installed	PCI Slot #1	: Not Installed
ISA PnP	: Not Installed	PCI Slot #2	: Not Installed
ISA PnP	: Not Installed	PCI Slot #3	: Not Installed
		PCI Slot #4	: Not Installed
<F1> to continue, <F2> to run Setup, <F10> to power off, <F5> to retain			

Setup Program

To run the *Setup* program, interrupt the POST by pressing **(F2)** when the **F2=Setup** message appears on the initial “Vectra” logo screen.

The band along the top of the screen offers five menus: Main, Configuration, Security, Power, and Exit. These are selected using the left and right arrow keys. Each menu is discussed in the following sub-sections. For a more complete description, see the *User's Guide* that was supplied with the PC.

Main Menu

The Main Menu presents the user with a list of fields, such as “System Time” and “Key auto-repeat speed”. These can be selected using the up and down arrow keys, and can have their values changed using the **(F7)** and **(F8)** keys.

The “Item-Specific Help” field changes automatically as the user moves the cursor between the fields. It tells the user what the presently highlighted field is for, and what the options are.

Some fields are not changeable. Examples include fields that are for information only, and fields whose contents become “frozen” by the setting of a value in some other field. Such fields are displayed in a different color, without the “[” and “]” brackets. When the user moves the cursor with the up and down arrow keys, these fields are skipped.

Some fields disappear completely when a choice in another field makes their appearance inappropriate.

Configuration Menu

The Configuration Menu does not have the same structure as the Main Menu and Power Menu. Instead of presenting a list of fields, it offers the user a list of sub-menus. Again, the user steps between the options using the up and down arrow keys, but presses the **(Enter)** key to enter the chosen sub-menu (and the **(Esc)** key to go back again when finished).

If access to devices has been disabled in the Security Menu, then the configuration of those devices on the Configuration Menu becomes frozen, as shown in the diagram below for Serial port A. The field becomes starred, appears in a different color, and cannot be changed.

Phoenix BIOS Setup — Copyright 1985-95 Phoenix Technologies Ltd. Copyright 1997 Hewlett-Packard Rev. HD.07.xx							
		Configuration					
Integrated I/O Ports						Item-Specific Help	
<div>Parallel port<div>[378h IRQ7]</div></div> <div>Parallel port mode<div>[Centronix TM]</div></div> <div>Serial port A<div>* 3F8h IRQ4</div></div> <div>Serial port B<div>[Disabled]</div></div> <div><div>[*] = The device is disabled for security reasons. To enable it, use the Security/Hardware Protection menu.</div></div>						<div>Enables or disables the on-board parallel port at the specific address. 'Disabled' frees resources used by the port.</div>	
F1 ESC	Help Exit	↕ ↔	Select Item Select Menu	F7/F8 Enter	Change Values Select > Sub-Menu	F9 F10	Setup Defaults Previous Values

Disabling a device in the Configuration Menu (for example, Serial port B in the diagram above) has the advantage of freeing the resources (such as IRQs and peripheral addresses). Disabling a device in the Security Menu disables the access, not the device. It does not have the advantage of freeing the resources, but has the advantage of temporarily disabling the device without losing the configuration settings.

The **Modem IRQ** field, in the Modem sub-menu, is used when a modem accessory has been installed. It does not enable the IRQ on the modem. It is used to indicate, to the System BIOS, which of the IRQ lines should wake up the PC when the modem receives a ringing tone. It is only applicable with an APM 1.2 compatible operating system, such as Windows 95.

Security Menu

Sub-menus are presented for changing the characteristics and values of the User Password, the System Administrator Password, the amount of protection against use of the system's drives (using the Hardware Protection sub-menu), and the amount of protection against being able to boot from the system's drives (using the Start-Up Center sub-menu).

The minimum lengths of either type of password can be set to a specific number of characters, or to **none**. The maximum length of each is 32 characters. A limit can be set for the maximum number of retries that are permitted if the password is mistyped, and whether a delay should be imposed (of successively increasing lengths: 4 seconds, 8 seconds, 16 seconds, and finally 32 seconds) before successive retries are accepted (using the **exponential** setting for the "Lock Time Between Attempts" field).

The "User Password" sub-menu grants access to the keyboard lock timer option. Once this password has been set, the menu gives access to the main sub-menu of user preferences.

Under the "Hardware Protection" sub-menu, the following devices can have their access **enabled/disabled**: flexible disk controller, IDE controllers, serial and parallel ports. Writes to the flexible disk can be **disabled**, so as to prevent the exporting of data. Writes to the hard disk drive boot sector can be **disabled**, for instance as a protection against viruses.

Under the "Start-Up Center" sub-menu, the *Setup* program not only allows the user to select which devices are **enabled** or **disabled** for booting up the system, but also indicates their order of precedence when more than one is enabled.

Power Menu

The "Power" menu allows the user to set the standby delay. It also allows the system administrator to decide whether the serial ports, mouse, or space bar are enabled as a means of reactivating the system from *Standby* or *Suspend*.

Power Saving and Ergonometry

Power-On from Space-Bar

The *power-on from the space-bar* function is enabled, provided that:

- The computer is connected to a Power-On keyboard (recognizable by the Power-On icon on the space bar).
- The computer is running a Windows operating system.
- The function has not been disabled by setting SW-8 to **open** on the system board switches.
- The function has not been disabled in the “Power” menu of the *Setup* program.

Soft Power Down

When the user requests the operating system to shutdown, the environment is cleared, and the computer is powered off. *Soft Power Down* is available with the Windows NT and Windows 95 operating systems, but not with the OS/2 operating system.

The hardware to do this is contained within the HP ASIC chip, LittleBen. This chip is described on page 34.

BIOS Addresses

This section provides a summary of the main features of the HP system BIOS. This is software that provides an interface between the computer hardware and the operating system.

System Memory Map

Reserved memory used by accessory boards must be located in the area from C8000h to EFFFFh.

0 - 3Fh	Interrupt vector table	640 KB: The addresses 0-9FFFFh are collectively known as the Base memory area
400h - 4Fh	BIOS data area	
500h - 9EFFFh		
9F000h - 9FFFFh	Extended BIOS data area	
A0000h - BFFFFh	128 KB: Video memory area	
C0000h - C7FFFh	32 KB: Video BIOS area	
C8000h - D7FFFh	64 KB: available for accessory boards (used by the boot ROM, if configured in the <i>Setup</i> program)	
D8000h - EFFFFh	96 KB: available after the POST (for upper memory block, UMB, for example)	
F0000h - FFFFFh	64 KB: System BIOS area	
100000h - FFFFFFFFh	1 MB plus: Extended memory	

Product Identification

The reserved addresses in the 64 KB BIOS ROM data area, which contain various product identification and BIOS identification strings, are no longer accessed directly. Instead, the information is obtained from utilities in the Desk Management Interface (DMI).

HP I/O Port Map (I/O Addresses Used by the System¹)

Peripheral devices, accessory devices and system controllers are accessed via the system I/O space, which is not located in system memory space. The 64 KB of addressable I/O space comprises 8-bit and 16-bit registers (called I/O ports) located in the various system components. When installing an accessory board, ensure that the I/O address space selected is in the free area of the space reserved for accessory boards (100h to 3FFh).

Although the *Setup* program can be used to change some of the settings, the following address map is not completely BIOS dependent, but is determined partly by the operating system. Beware that some of the I/O addresses are allocated dynamically.

I/O Address Ports	Function
0000h - 000Fh	DMA controller 1
0020h - 0021h	Interrupt controller 1
0040h - 0043h	Interval timer 1
0060h, 0064h	Keyboard controller
0061h	System speaker, or NMI status and control
0070h	NMI mask register, RTC and CMOS address
0071h	RTC and CMOS data
0081h - 0083h, 008Fh	DMA low page register
0092h	Alternate reset and A20 Function
0096h - 009Fh	Internal ports (Little Ben ASIC)
00A0h - 00A1h	Interrupt controller 2
00C0h - 00DFh	DMA controller 2
00EAh - 00EBh	Internal port
00F0h - 00FFh	Co-processor error
0102h	Graphics controller (Matrox MGA)
0170h - 0177h	IDE hard disk drive controller secondary channel
01F0h - 01F7h	IDE hard disk drive controller primary channel

1. If configured (legacy resources only).

4 Summary of the HP/Phoenix BIOS

BIOS Addresses

I/O Address Ports	Function
0200h - 0207h	Joystick port (Soundblaster)
0220h - 022Fh	Audio interface 1 (Soundblaster)
0240h - 024Fh	Audio interface 2 (Soundblaster)
0260h - 026Fh	Audio interface 3 (Soundblaster)
0270h - 0273h	IO read data port for ISA Plug and Play enumerator
0278h - 027Fh	Parallel port 2
0280h - 028Fh	Audio interface 4 (Soundblaster)
02E8h - 02EFh	Serial port 4
02F8h - 02FFh	Serial port 2
0300h - 0301h	MPU-401 MIDI interface 2 (Soundblaster)
0330h - 0331h	MPU-401 MIDI interface 1 (Soundblaster)
0370h - 0371h	Super I/O controller
0372h - 0375h	Secondary flexible disk drive controller
0376h	IDE hard disk drive controller secondary channel
0377h	Secondary flexible disk drive controller
0378h - 037Ah	Parallel port 1
0388h - 038Bh	Ad-lib / FM synthesized music (Soundblaster)
03B0h - 03DFh	Graphics controller (Matrox MGA)
03E8h - 03EFh	Serial port 3
03F0h - 03F5h	Primary flexible disk drive controller
03F6h	IDE hard disk drive controller primary channel
03F7h	Primary flexible disk drive controller
03F8h - 03FFh	Serial port 1
0496h - 049Fh	Internal ports (Little Ben ASIC)
0678h - 067Bh	Parallel port 2 if ECP mode is selected
0778h - 077Bh	Parallel port 1 if ECP mode is selected
0CF8h - 0CFFh	Configuration registers for PCI devices

DMA Channel Controllers

Only “I/O-to-memory” and “memory-to-I/O” transfers are allowed. “I/O-to-I/O” and “memory-to-memory” transfers are disallowed by the hardware configuration.

The system controller supports seven DMA channels, each with a page register used to extend the addressing range of the channel to 16 MB. The following table summarizes how the DMA channels are allocated.

First DMA controller (used for 8-bit transfers)	
Channel	Function
0	Available
1	SoundBlaster or ECP mode for parallel port
2	Flexible disk I/O
3	ECP mode for parallel port or SoundBlaster
Second DMA controller (used for 16-bit transfers)	
Channel	Function
4	Cascade from first DMA controller
5	SoundBlaster or Available
6	Available
7	Available or SoundBlaster

Interrupt Controllers

The system has two 8259A compatible interrupt controllers. They are arranged as a master interrupt controller and a slave that is cascaded through the master.

The following table shows how the master and slave controllers are connected. The Interrupt Requests (IRQ) are numbered sequentially, starting with the master controller, and followed by the slave.

4 Summary of the HP/Phoenix BIOS

BIOS Addresses

IRQ (Interrupt Vector)		Interrupt Request Description
IRQ0(08h)		System Timer
IRQ1(09h)		Keyboard Controller
IRQ2(0Ah)	Slave IRQ	Cascade connection from INTC2 (Interrupt Controller 2)
	IRQ8(70h)	Real Time Clock
	IRQ9(71h)	Available for accessory board (ISA/PCI)
	IRQ10(72h)	SoundBlaster 3, or Available for accessory board (ISA/PCI)
	IRQ11(73h)	Available for accessory board (ISA/PCI)
	IRQ12(74h)	Mouse, or ISA accessory board
	IRQ13(75h)	Co-processor
	IRQ14(76h)	IDE, or ISA accessory board
	IRQ15(77h)	Secondary IDE or ISA/PCI accessory board
IRQ3(0Bh)		Serial Port 2, Serial Port 4, or ISA accessory board
IRQ4(0Ch)		Serial Port 1, Serial Port 3, or ISA accessory board
IRQ5(0Dh)		SoundBlaster 1, Parallel Port 2, or ISA accessory board
IRQ6(0Eh)		Flexible Disk Controller
IRQ7(0Fh)		SoundBlaster 2, Parallel Port 1, or ISA accessory board

Using the *Setup* program:

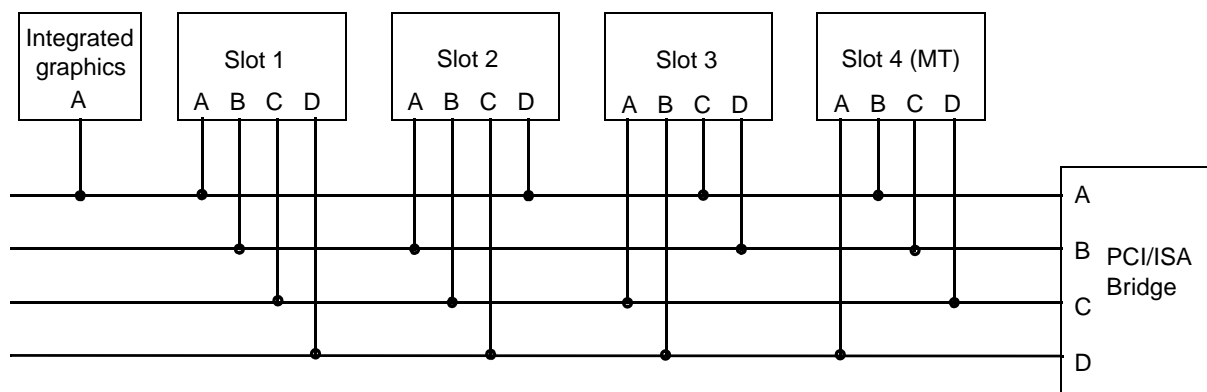
- IRQ3 can be made available by disabling serial ports 2 and 4.
- IRQ4 can be made available by disabling serial ports 1 and 3.
- IRQ5 can be made available by disabling the parallel port 2.
- IRQ7 can be made available by disabling parallel ports 1 and 2.

PCI Interrupt Request Lines

PCI devices generate interrupt requests using up to four PCI interrupt request lines (INTA#, INTB#, INTC#, and INTD#).

When a PCI device makes an interrupt request, the request is re-directed to the system interrupt controller. The interrupt request will be re-directed to one of the IRQ lines made available for PCI devices.

The PCI interrupt lines A, B, C and D are spread across the four inputs of the interrupt router (which is part of the PCI/ISA bridge, in the PIIX3 chip). Since most PCI devices are single-function, this allows for an even distribution of the lines. The distribution is shown in the following diagram. In this, Slot 4 is present only on minitower models (and is omitted on desktop models).



PCI interrupts are then mapped into ISA interrupts inside the PCI/ISA Bridge (in the PIIX3 chip), by configuring registers 60h through 63h.

Bit	Description
7	Routing of interrupts: when enabled, this bit routes the PCI interrupt signal to the PC-compatible interrupt signal specified in bits[3:0]. At reset, this bit is disabled (set to 1)
6:4	Reserved: read as 000
3:0	IRQx# Routing Bits: these bits specify which IRQ signal to generate. Possible values are: 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15.

The possible choices given by the *Setup* program are 9, 10, 11, 15. If some of these are unavailable due to ISA cards, some interrupts will have to be shared.

The IDE controller (device 04h, function 01h) is configured in *legacy mode*, and uses IRQ 14 (IRQ 15 for the secondary channel).

4 Summary of the HP/Phoenix BIOS BIOS Addresses

Power-On Self-Test and Error Messages

This chapter describes the Power-On Self-Test (POST) routines, which are contained in the computer's ROM BIOS, the error messages which can result, and the suggestions for corrective action.

Order in Which the Tests are Performed

Each time the system is powered on, or a reset is performed, the POST is executed. The POST process verifies the basic functionality of the system components and initializes certain system parameters.

The POST starts by displaying a graphic screen with the initial “Vectra” logo when the PC is restarted. If the POST detects an error, the error message is displayed inside a *view system errors* screen, in which the *error message utility* (EMU) not only displays the error diagnosis, but the suggestions for corrective action (see page 75 for a brief summary). Error codes are no longer displayed.

Devices, such as memory and newly installed hard disks, are configured automatically. The user is not requested to confirm the change. Newly removed hard disks are detected, and the user is prompted to confirm the new configuration by pressing **[F4]**. Note, though, that the POST does not detect when a hard disk drive has been otherwise changed.

During the POST, the BIOS and other ROM data is copied into high-speed shadow RAM. The shadow RAM is addressed at the same physical location as the original ROM in a manner which is completely transparent to applications. It therefore appears to behave as very fast ROM. This technique provides faster access to the system BIOS firmware.

The following table lists the POST routines in the order in which they are executed (from the shadow RAM). If the POST is initiated by a soft reset **[Ctrl]** **[Alt]** and **[Delete]**, the RAM tests are not executed and shadow RAM is not cleared. In all other respects, the POST executes in the same way following power-on or a soft reset.

Test	Description
System BIOS Tests	
LED Test	Tests the LEDs on the control panel.
System (BIOS) ROM Test	Calculates an 8-bit checksum. Test failure causes the boot process to abort.
RAM Refresh Timer Test	Tests the RAM refresh timer circuitry. Test failure causes the boot process to abort.
Interrupt RAM Test	Checks the first 64 KB of system RAM used to store data corresponding to various system interrupt vector addresses. Test failures cause the boot process to abort.

5 Power-On Self-Test and Error Messages

Order in Which the Tests are Performed

Shadow the System ROM BIOS	Tests the system ROM BIOS and shadows it. Failure to shadow the ROM BIOS will cause an error code to display. The boot process will continue, but the system will execute from ROM. This test is not performed after a soft reset (using Ctrl , Alt , and Delete).
Load CMOS Memory	Checks the serial EEPROM and returns an error code if it has been corrupted. Copies the contents of the EEPROM into CMOS RAM.
CMOS RAM Test	Checks the CMOS RAM for start-up power loss, verifies the CMOS RAM checksums. Test failure causes error codes to display.
CPU Cache Memory Test	Tests the processor's internal level-one cache RAM. Test failure causes an error code to display and the boot process to abort.
Video Tests	
Initialize the Video	Initializes the video subsystem, tests the video shadow RAM, and, if required, shadows the video BIOS. A failure causes an error code to display, but the boot process continues.
System Board Tests	
8042 Self-Test	Downloads the 8042 and invokes the 8042 internal self-test. A failure causes an error code to display.
Timer 0/Timer 2 Test	Tests Timer 0 and Timer 2. Test failure causes an error code to display.
DMA Subsystem Test	Checks the DMA controller registers. Test failure causes an error code to display.
Interrupt Controller Test	Tests the Interrupt masks, the master controller interrupt path (by forcing an IRQ0), and the industry-standard slave controller (by forcing an IRQ8). Test failure causes an error code to display.
Real-Time Clock Test	Checks the real-time clock registers and performs a test that ensures that the clock is running. Test failure causes an error code to display.
Audio Test	If the audio board is present, invokes a built-in self-test. Test failure causes an error code to display.
Memory Tests	
RAM Address Line Independence Test	Verifies the address independence of real-mode RAM (no address lines stuck together). Test failure causes an error code to display.
Size Extended Memory	Sizes and clears the protected mode (extended) memory and writes the value into CMOS bytes 30h and 31h. If the system fails to switch to protected mode, an error code is displayed.
Real-Mode Memory Test (First 640KB)	Read/write test on real-mode RAM. (This test is <i>not</i> done during a reset using Ctrl , Alt , and Delete). The test checks each block of system RAM to determine how much is present. Test failure of a 64 KB block of memory causes an error code to display, and the test is aborted.
Shadow RAM Test	Tests shadow RAM in 64 KB segments (except for segments beginning at A000h, B000h, and F000h). If they are <i>not</i> being used, segments C000h, D000h and E000h are tested. Test failure causes an error code to display.

5 Power-On Self-Test and Error Messages

Order in Which the Tests are Performed

Protected Mode RAM Test (Extended RAM)	Tests protected RAM in 64 KB segments above 1 MB. (This test is <i>not</i> done during a reset using <input type="button" value="Ctrl"/> <input type="button" value="Alt"/> and <input type="button" value="Delete"/>). Test failure causes an error code to display.
Keyboard / Mouse Tests	
Keyboard Test	Invokes a built-in keyboard self-test of the keyboard's microprocessor and tests for the presence of a keyboard and for stuck keyboard keys. Test failure causes an error code to display.
Mouse Test	If a mouse is present, invokes a built-in mouse self-test of the mouse's microprocessor and for stuck mouse buttons. Test failure causes an error code to display.
Tests of Flexible Disk Drive A	
Flexible Disk Controller Subsystem Test	Tests for proper operation of the flexible disk controller. Test failure causes an error code to display.
Coprocessor Tests	
Internal Numeric Coprocessor Test	Checks for proper operation of the numeric coprocessor part of the processor. Test failure causes an error code to display.
Communication Port Tests	
Parallel Port Test	Tests the integrated parallel port registers, as well as any other parallel ports. Test failure causes an error code to display.
Serial Port Test	Tests the integrated serial port registers, as well as any other serial ports. Test failure causes an error code to display.
Hard Disk Drive Tests	
Hard Disk Controller Subsystem Test	Tests for proper operation of the hard disk controller. Test failure causes an error code to display. The test does not detect hard disk replacement or changes in the size of the hard disk.
System Configuration Tests	
System Generation	Initiation of the system generation (SYSGEN) process, which compares the configuration information stored in the CMOS memory with the actual system. If a discrepancy is found, an error code will be displayed.
Plug and Play Configuration	Configures any Plug and Play device detected (either PCI or ISA): <ul style="list-style-type: none"><input type="checkbox"/> All PCI devices, and any ISA device necessary for loading the operating system will be configured for use.<input type="checkbox"/> Any ISA device that is not required for loading the operating system, will be initialized (prepared for loading of a device driver), but not fully configured for use.

Error Message Summary

The POST section of the HP BIOS no longer displays numeric error codes (such as 910B) but gives a self-explanatory, descriptive diagnosis, and a list of suggestions for corrective action. The following table summarizes the most significant of the problems that can be reported.

Message	Explanation or Suggestions for Corrective Action
Operating system not found	Check whether the disk, HDD, FDD or CD-ROM disk drive is connected. If it is connected, check that it is detected by POST. Check that your boot device is enabled on the <i>Setup</i> Security menu. If the problem persists, check that the boot device contains the operating system.
Missing operating system	If you have configured HDD user parameters, check that they are correct. Otherwise, use HDD type "Auto" parameters.
Failure fixed disk (preceded by a 30" time-out)	Check that HDD is connected. Check that HDD is detected in POST. Check that boot on hard disk drive is enabled in <i>Setup</i> .
Diskette Drive A (or B) error	Check whether the diskette drive is connected. Check <i>Setup</i> for the configuration.
System battery is dead	You may get this message if the computer is disconnected for a few days. When you Power-on the computer, run <i>Setup</i> to update the configuration information. The message should no longer be displayed. Should the problem persist, replace the battery.
Keyboard error	Check that the keyboard is connected.
Resource Allocation Conflict -PCI device 0079 on system board	Clear CMOS.
Video Plug and Play interrupted or failed. Re-enable in Setup and try again	You may have powered your computer Off/On too quickly and the computer turned off Video plug and play as a protection.
System CMOS checksum bad - run Setup	CMOS contents have changed between 2 power-on sessions. Run <i>Setup</i> for configuration.
I/O device IRQ conflict	Serial ports A and B may have been assigned the same IRQ. Assign a different IRQ to each serial port and save the configuration.
No message, system "hangs" after POST	Check that cache memory and main memory are correctly set in their sockets.
Other	An error message may be displayed and the computer may "hang" for 20 seconds and then beep. The POST is probably checking for a mass storage device which it cannot find and the computer is in Time-out Mode. After Time-out, run <i>Setup</i> to check the configuration.

Beep Codes

If a terminal error occurs during POST, the system issues a beep code before attempting to display the error. Beep codes are useful for identifying the error when the system is unable to display the error message.

Beep Pattern	Beep Code ¹	Numeric Code	Description
-	1	B4h	This does not indicate an error. There is one short beep before system startup.
— --	02	98h	Video configuration failure or option ROMs check-sum failure
— - - - - -	0223	16h	BIOS ROM check-sum failure
— - - - - -	0300	20h	DRAM refresh test failure
— - - - - -	0303	22h	8742 Keyboard controller test failure
— - - - - -	0340	2Ch	RAM failure
— - - - - -	0343	2Eh	RAM failure on data bits in low byte of memory bus
— - - - - -	0400	30h	RAM failure on data bits in high byte of memory bus
-- — - - -	2023	46h	ROM copyright notice check failure
- - - - - -	2230	58h	Unexpected interrupts test failure
— - - - - -	02022		Continuous beeps. Keyboard error

¹Where digits 1, 2, 3, 4 represent the number of short beeps, and 0 represents the occurrence of a single long beep.

Lights on the Status Panel

When the computer is first powered on, the *power-on* light on the status panel illuminates yellow for about a second before changing to green. This change of color is caused by the execution of an instruction early in the System BIOS code.

If the light remains at yellow, therefore, it indicates a failure of the processor or the System ROM in the instruction-fetch process. Check that the processor is correctly seated in its socket, and that its VRM is also correctly seated.

A

Audio 10, 11, 20, 48, 49, 52, 58, 60, 62, 65, 67, 72

B

BIOS 32, 33, 34, 57, 58, 60, 62, 63, 64, 65, 67, 68, 71, 72, 75, 76

C

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D

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G

Graphics 10, 11, 18, 20, 38, 39, 42, 44, 45, 47, 55, 58, 60, 62, 64, 65, 68, 72, 75, 76

I

IDE 10, 11, 18, 20, 23, 29, 30, 51, 58, 60, 62, 65, 67, 68, 72, 75

M

Mass storage 10, 11, 20, 50, 51, 58, 60, 62, 65, 72

N

Network 10, 11, 15, 18, 20, 34, 55, 58, 60, 62, 65, 72

O

Operating systems 34, 35, 45, 49, 50, 63, 64, 75

P

Package 10, 11, 12

Power supply 10, 11, 13, 18, 55

S

SCSI 10, 11, 51, 64, 68, 72

System board 10, 11, 17, 18, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 38, 44, 51, 55,
58, 60, 62, 63, 64, 65, 67, 68, 72, 75, 76

U

USB 10, 11, 18, 20, 23, 30, 55, 58, 60, 62, 65, 72

../././pictures/logohp.tif @ 300 dpi 1
eps/mokt08a.tif @ 300 dpi 10
eps/mokt38a.tif @ 300 dpi 10
eps/mokt03a.eps 10
eps/mokt04a.eps 10
eps/mokt39a.tif @ 300 dpi 10
eps/mokt03m.eps 11
eps/mokt04m.eps 11
eps/mokt39m.tif @ 300 dpi 11
eps/mokt12a.tif @ 300 dpi 26
eps/mokt15a.tif @ 300 dpi 44
eps/dtt31a.eps 55
eps/dtt32a.eps 55
eps/dtt33a.eps 55
eps/dtt30d.eps 55