Clock Gating Recommendations

Application Note

Advanced Micro Devices

Microprocessor motherboard design requires that special attention be paid to the design of the clock control circuitry. A designer must provide for timing control of the clock at startup. Keeping this requirement in mind, this application note provides three examples of clock delay circuits.

AMD recommends that the CLK input to an Am486® or $Am5_X86$™ microprocessor be grounded until V_{CC} has reached its normal operating level. Once V_{CC} reaches its normal operating level, the CPU is able to receive its specified clock frequency.

Methods of gating the CPU clock include:

- Using a chipset that does not clock the CPU until V_{CC} has fully ramped.
- Using a clock driver with an output enable.
- Using a clock clamping circuit to gate the CPU clock.

For proper operation of Am486 and $Am5_X86$ devices, the system timing must be maintained as illustrated in Figure 1. Good design practice dictates gating or "holding off" the CPU clock until the system V_{CC} has reached its normal operating voltage. The timing diagram illustrates that once V_{CC} reaches its operating voltage point (either 3.3 V or 5 V), and the PWRGOOD signal is active, RESET must be asserted for at least 1 ms to allow the CPUs internal PLL to lock prior to system operation.

Chipset with Internal Delay

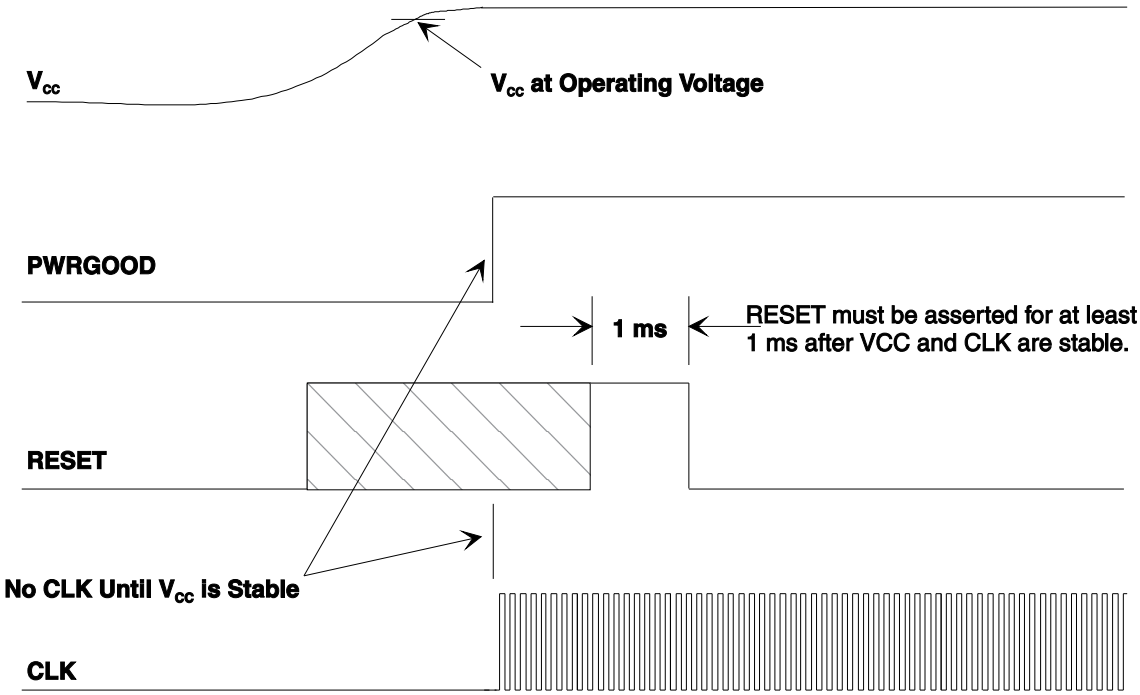
Because many 486 core logic chipsets use PWRGOOD and CLK as inputs to generate RESET and CPUCLK as outputs, they have the potential to incorporate an internal delay function, holding off the CPU until V_{CC} has reached it's normal operating voltage.

Figure 2 illustrates a chipset capable of providing internal clock gating.

Figure 2. Internal Delay Function of Chipset

Note: *Check your chipset's data sheet for specifics on your chipset's internal delay function.*

Figure 1. Timing Diagram of PicoPower Redwood Chipset Delay Function



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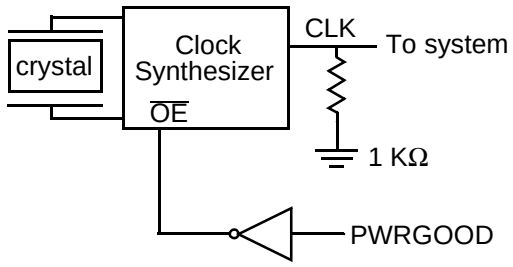
Clock Driver With Output Enable

A clock synthesizer (or other driver) with an output enable pin for the CPU clock can be used to prevent the CPU from being clocked until V_{CC} has reached its normal operating voltage.

The circuit in Figure 3 consists of a frequency generator with a dedicated $\overline{OE}$, which may be used to "hold off" or gate the clock until V_{CC} has reached its normal operating level using PWRGOOD as the output enable.

Figure 3. Clock Synthesizer With $\overline{OE}$



Clock Clamping Circuit

A third method of gating the CPU clock is to use a clock clamping circuit to effectively ground the clock input for a predetermined period of time.

In addition to delaying the CPU clock, the clock clamping circuit, shown in Figure 4, also prevents noise glitches on the clock signal from being sensed by the CPU during the power-on sequence when V_{CC} of the microprocessor is making the transition from 0 V to V_{CC} (e.g., 3.3 V or 5 V).

Microprocessor clock noise glitches usually are caused by one of the following conditions:

- Bad clock generator start-up circuit design
- Poor layout of the microprocessor printed circuit trace on the PC motherboard
- Power supply ringing during transition from 0 V to V_{CC}
- A very long voltage slew rate (e.g., 100 ms).

In any case, the clock clamping circuit ensures that a clock signal glitch is not sensed by the microprocessor clock input circuit during startup.

CPU clock signal integrity is best maintained by passing the clock directly from the core logic.

Figure 4. Clock Clamping Circuit