Advance Information

This document contains information on a product under development.
The parametric information contains target parameters that are subject to change.

Bt497A/498A

240 MHz Monolithic CMOS Triple 1K x 8 RAMDAC™

The Bt497A/8A is designed specifically for high-performance, high-resolution color graphics applications. The architecture enables the display of true-color 1920 x 1200 bit-mapped color graphics at 75 Hz refresh rates. The wide input pixel port and internal multiplexing modes enable TTL-compatible interfacing to the frame buffer, while maintaining PLL-generated 240 MHz, or externally provided 240 MHz video data rates required for high-refresh-rate, high-resolution color graphics.

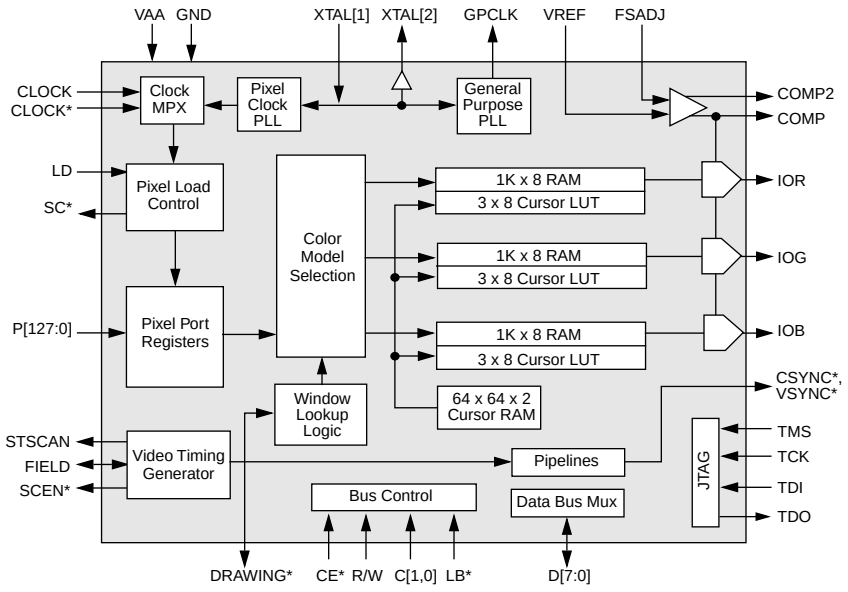
The Bt497A/8A supports PLL pixel clock generation, supporting a variety of frequencies using an M/N divisor scheme. This decreases system cost due to the elimination of multiple crystal oscillators that are used to support a variety of monitor and refresh rates.

The Bt497A/8A contains three 1K x 8 color lookup tables for color-space flexibility, triple 8-bit video D/A converters, a programmable 64 x 64 x 2 cursor, and a fully programmable video timing generator.

The Bt497A/8A RAMDAC allows different display modes of operation for each pixel. Utilizing a window-type scheme, each set of pixel and control bits maps the accompanying pixel data to a user-defined display mode. The window identification index addresses a color model table which determines the description of the pixel data. For example, separate windows displaying 24-plane true color, 8-plane pseudo color, and 24-plane double-buffer true color can exist within a single frame.

A programmable setup (0 or 7.5 IRE) is included.

Functional Block Diagram



Distinguishing Features

- PLL pixel clock generation (M/N)
- Supports true-color 1920 x 1200 resolutions
- Up to 128-bit input pixel port width
- 240 and 160 MHz operation
- Multiple display modes on a pixel basis
- High-resolution true-color support
- 2:1 and 4:1 multiplexed pixel port support
- Programmable pixel format
- Three 1K x 8 color palette RAMs
- 64 x 64 x 2 programmable cursor
- Programmable setup (0 or 7.5 IRE)
- VRAM shift clock generation
- On-chip user-definable video timing generator
- JTAG support
- 160-pin (Bt497A), 208-pin (Bt498A) PQFP packages
- LVTTL (3.3 V) I/O interface

Applications

- High-resolution color 3D graphics
- CAE/CAD/CAM
- Image processing
- Instrumentation
- Desktop publishing

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt497AKHF160	160-Pin PQFP	0–70° C with 100 LFPM airflow
Bt498AKHF240	208-Pin PQFP	0–70° C with 100 LFPM airflow

Print date: August 1997

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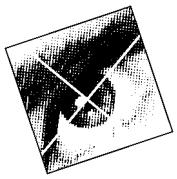


CIRCUIT DESCRIPTION

Introduction

The Bt497A and Bt498A are software-compatible RAMDACs designed for high-performance and high-resolution applications. The architecture supports a 1280 x 1024 160 MHz (Bt497A) or up to a 1920 x 1200 240 MHz (Bt498A) bit-mapped color-graphics display.

Two on-chip Phase Lock Loops (PLL) are provided to eliminate the high-speed signals on the Printed Circuit Board (PCB) and reduce the need for multiple, expensive Emitter-Coupled Logic (ECL) crystal oscillators required to support multiple monitors and refresh rates. The PLLs use an M/(L x N) scheme to program over 500 unique Pixel Clock or General Purpose Clock frequencies.

The Bt497A/8A allows different display modes of operation for each pixel. Utilizing a window attribute scheme, the control bits of every pixel are used to map the pixel data to a pre-defined display mode (pseudo color from three 1K x 8 color lookup tables or nonlinear true color) or to create an overlay image. The control bits on the Bt497A/8A can define the pixel port source to accommodate double-buffered operation for animation. The 128-pin pixel port supports a standard 2:1 and 4:1 format, as well as 4/2:1 and 8/2:1 interleaved format used in high-end 3D graphics Video RAMs (VRAMs).

The Bt497A/8A provides an on-chip, user-definable, three-color, 64 x 64 bit-map cursor and a programmable timing generator. With the timing generator, users can now achieve full control of sync and blank characteristics, for both interlaced and progressive scanned systems, that previous RAMDACs required externally. Video control can be sent to the monitor on discrete sync outputs or on the green (IOG) analog output. The Bt497A/8A contains three 8-bit DACs that can be programmed with a 7.5 IRE pedestal.

Pin Descriptions

The Bt497A is packaged in a 160-pin Plastic Quad Flatpack (PQFP), illustrated in Figure 1. The Bt498A is a 208-pin PQFP shown in Figure 2. Table 1 lists the pin descriptions, labels and I/O assignments for both packages.

Figure 1. Bt497A 160-pin PQFP

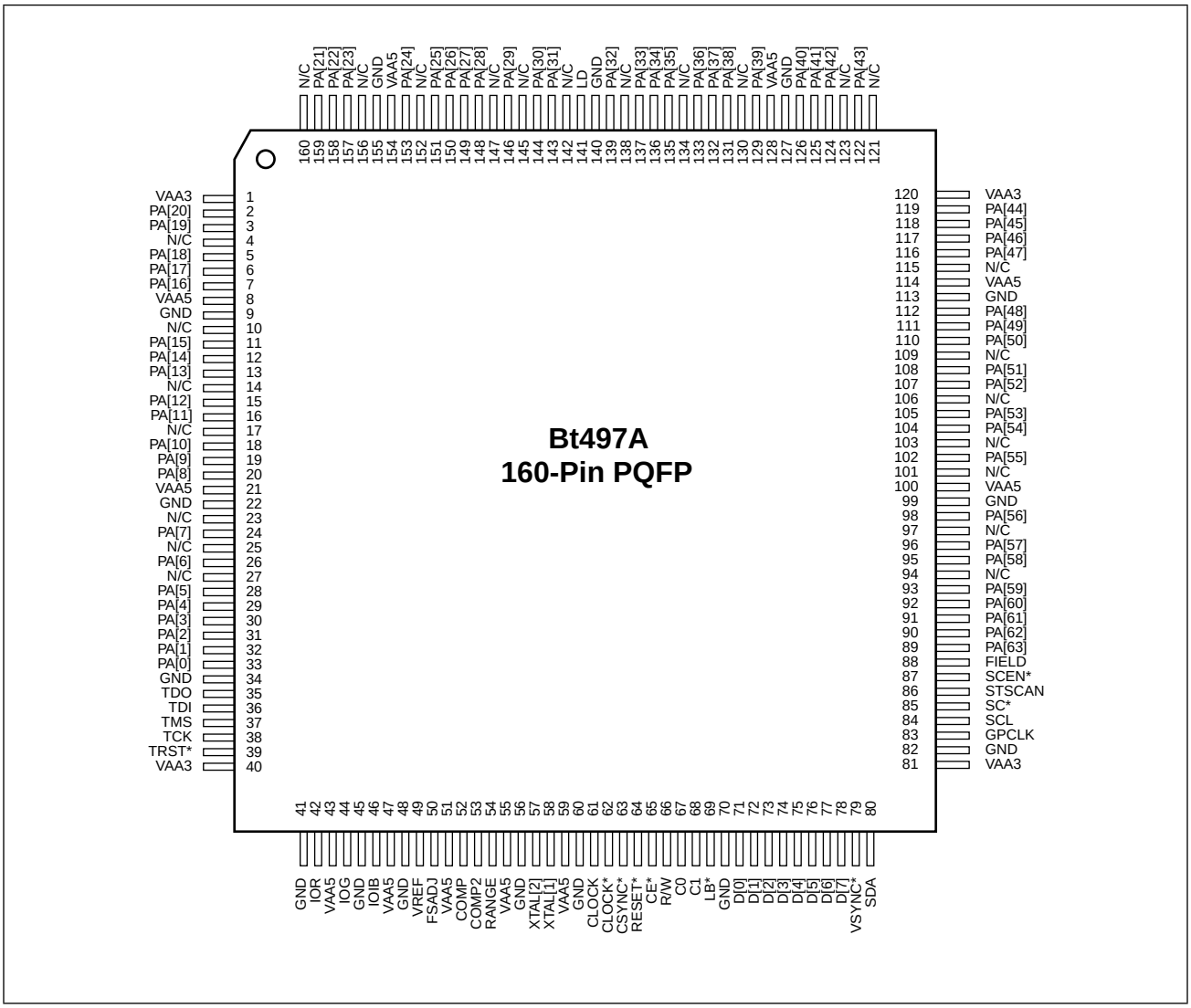


Figure 2. Bt498A 208-pin PQFP

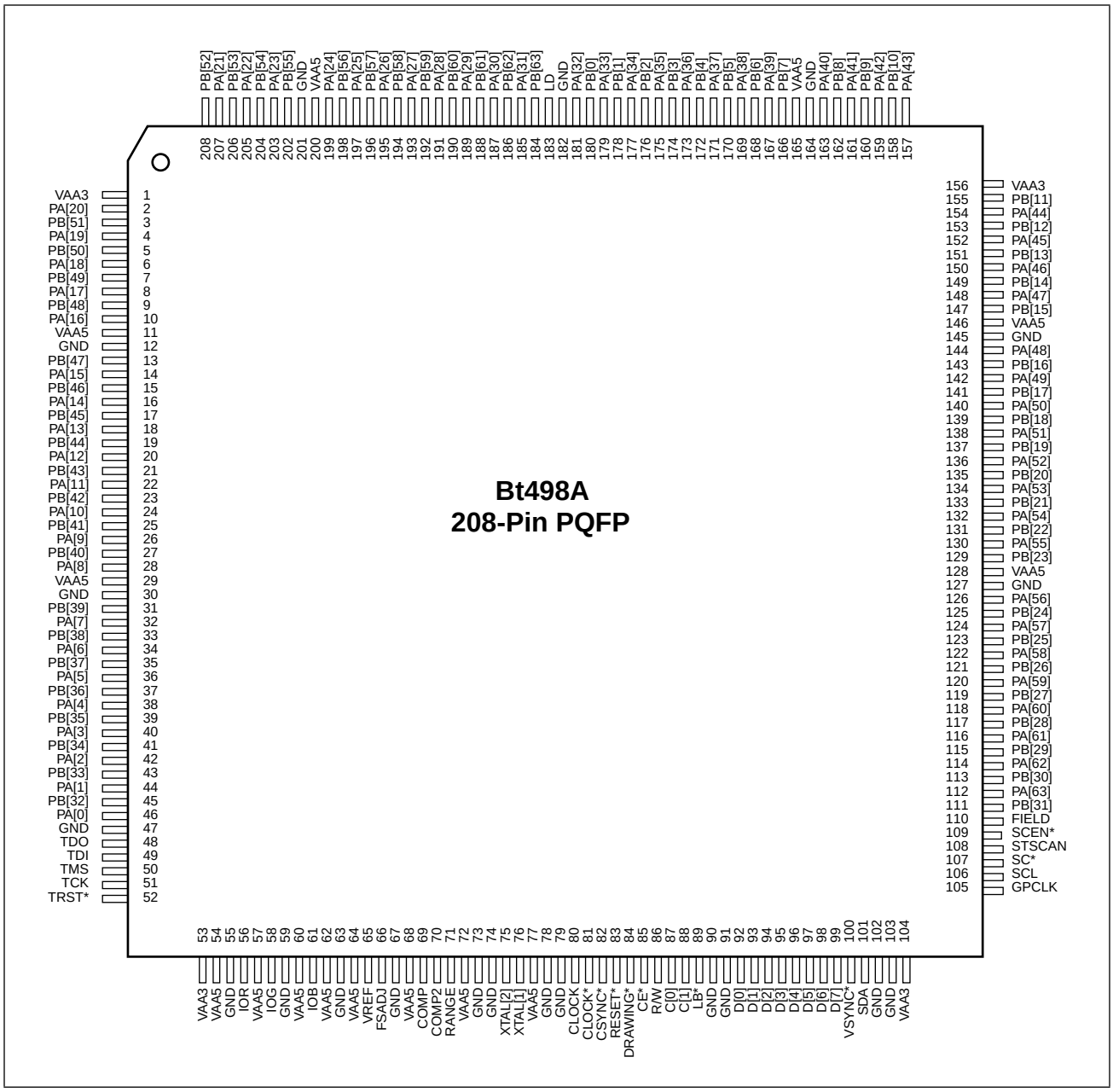


Table 1. Pin Assignments *(1 of 3)*

Pin Count	Signal Name	I/O/Z	Description
8	D[7:0]	I/O/Z	MPU Data Bus (LVTTL Compatible). Bidirectional data. The MPU port will zero fill unused bits on data reads.
2	C[1,0]	I	MPU Control Bus Input (LVTTL Compatible).
1	R/W	I	MPU Read/Write Control Input (LVTTL Compatible). Defines the transaction direction.
1	LB*	I	MPU Low Byte Control (LVTTL Compatible).
1	CE*	I	Chip Enable Control Input (LVTTL Compatible). This input must be a logical 0 to enable data to be written to or read from the device. During write operations, data is internally registered on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
128	P[63:0](A,B)	I	Pixel Port Inputs (LVTTL Compatible). These inputs have internal pullup resistors that cause the logic level to be high if they are left unconnected. Bt497A PA[63:0].
1	LD	I	Pixel Port Load Clock (LVTTL Compatible). The rising edge of this signal captures input pixel data.
1	SC*	O	Serial Clock Output (LVTTL Compatible). This signal is produced by the pixel clock divider. It is meant to be used as the clock for the serial port of the video memory.
1	SCEN*	O	Serial Clock Enable Output (LVTTL Compatible). This signal is produced by the timing generator and is meant to control the serial port of the video memory.
1	STSCAN	O	Horizontal Scan Line Indicator (LVTTL Compatible). This signal is produced by the timing generator and is meant for use by external circuitry for the purpose of indexing the serial port of the video memory.
1	FIELD	I/O/Z	Odd Field Indicator (LVTTL Compatible). This signal is produced by the timing generator and is meant for use by external circuitry for the purpose of indexing the serial port of the video memory.
1	XTAL1	I	Crystal Input. This input is either connected to a crystal or driven by a CMOS oscillator. The internal phase lock loop generates the pixel clock using this input.
1	XTAL2	O	Crystal Amplifier Output. This output is connected to the second terminal of the crystal when used.
1	GPCLK	O	General Purpose Clock Output. Frequency is determined by the GPCLK PLL Control Register.
1	DRAWING*	I/O/Z	Open-drain signal used for coordinating WLUT updates among multiple Bt498A devices.
2	CLOCK, CLOCK*	I	Clock Inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.

Table 1. Pin Assignments *(2 of 3)*

<table>
<tr><th>Pin Count</th><th>Signal Name</th><th>I/O/Z</th><th>Description</th></tr>
<tr><td>1</td><td>VREF</td><td>I</td><td>Voltage Reference Input. An external voltage reference circuit must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA5. The decoupling capacitor must be as close as possible to the device to keep lead lengths to an absolute minimum.</td></tr>
<tr><td>2</td><td>COMP, COMP2</td><td></td><td>Compensation pins. These pins provide compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between these two pins.</td></tr>
<tr><td>1</td><td>RANGE</td><td></td><td>Compensation for VCO. A 0.01 µF ceramic chip capacitor and a 4.7 µF tantalum capacitor must be connected between this pin and adjacent VAA5.</td></tr>
<tr><td>1</td><td>FSADJ</td><td>I</td><td>Full-Scale Adjust Control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. Note that the IRE relationships in Figures 29 and 30 are maintained, regardless of the full-scale output current.
The relationship between RSET and the full-scale output current on IOG is:
RSET (Ω) = K1 * VREF (V) / IOG (mA)
The full-scale output current on IOR and IOB for a given RSET is:
IOR, IOB (mA) = K2 * VREF (V) / RSET (Ω)
where K1 and K2 are defined as:
<table>
<tr><th>Setup</th><th>IOG</th><th>IOR, IOB</th></tr>
<tr><td>7.5 IRE</td><td>K1 = 3052</td><td>K2 = 2180</td></tr>
<tr><td>0 IRE</td><td>K1 = 2888</td><td>K2 = 2016</td></tr>
</table>
</td></tr>
<tr><td>1</td><td>IOR</td><td>O</td><td>Red analog current output.</td></tr>
<tr><td>1</td><td>IOG</td><td>O</td><td>Green analog current output.</td></tr>
<tr><td>1</td><td>IOB</td><td>O</td><td>Blue analog current output.</td></tr>
<tr><td>1</td><td>VSYNC*</td><td>O</td><td>Vertical Sync Output. Active low on reset, but may be programmed active high via DAC control register.</td></tr>
<tr><td>1</td><td>CSYNC*</td><td>O</td><td>Composite Sync Output. Active low on reset, but may be programmed active high via DAC control register.</td></tr>
<tr><td>1</td><td>SDA</td><td>I/O/Z</td><td>Serial Monitor Port Data. Open Drain pin.</td></tr>
<tr><td>1</td><td>SCL</td><td>I/O/Z</td><td>Serial Monitor Port Clock. Open Drain pin.</td></tr>
<tr><td>1</td><td>RESET*</td><td>I</td><td>Reset Input (LVTTL Compatible). This is the reset signal. Its assertion causes a number of actions, these are described in Initializing the Bt497+/8+ in the Applications Information section.</td></tr>
</table>

Table 1. Pin Assignments *(3 of 3)*

Pin Count	Signal Name	I/O/Z	Description
1	TRST*	I	Test Reset (LVTTL compatible). JTAG input pin to be asserted on power on to force all the boundary scan cells to their normal, non-JTAG state. The transitions on this signal reset the JTAG state machine. When not performing JTAG operations, this pin should be driven to a logic high.
1	TMS	I	Test Mode Select (LVTTL compatible). JTAG input pin whose transitions drive the JTAG state machine through its sequences. When not performing JTAG operations, this pin should be driven to a logic high.
1	TCK	I	Test Clock (LVTTL compatible). Used to synchronize all JTAG test structures. Maximum clock rate for this pin is 50 MHz. When not performing JTAG operations, this pin should be driven to a logic high.
1	TDI	I	Test Data In (LVTTL compatible). JTAG input pin used for loading instructions to the TAP controller or for loading test vector data for boundary scan operation. When not performing JTAG operations, this pin should be driven to a logic high.
1	TDO	O	Test Data Out (LVTTL compatible). JTAG output used for verifying test results of all JTAG sampling operations. This pin is active for certain JTAG sequences, and is three-stated at all other times. When not performing JTAG operations, this pin should be left floating.
4	VAA3		+3.3 V Power Supply. All VAA3 pins must be connected together.
14	VAA5		+5.0 V Power Supply. All VAA5 pins must be connected together. (Bt497A: 10 pins)
20	GND		Ground. (Bt497A: 15 pins)
Note: I = Input, O = Output, Z = Three-state.			

Table 2. 208-pin PQFP Pin Labels

Pin	Pin Label	Pin	Pin Label	Pin	Pin Label	Pin	Pin Label	Pin	Pin Label
1	VAA3	43	PB[33]	85	CE*	127	GND	169	PA[38]
2	PA[20]	44	PA[1]	86	R/W	128	VAA5	170	PB[5]
3	PB[51]	45	PB[32]	87	C[0]	129	PB[23]	171	PA[37]
4	PA[19]	46	PA[0]	88	C[1]	130	PA[55]	172	PB[4]
5	PB[50]	47	GND	89	LB*	131	PB[22]	173	PA[36]
6	PA[18]	48	TDO	90	GND	132	PA[54]	174	PB[3]
7	PB[49]	49	TDI	91	GND	133	PB[21]	175	PA[35]
8	PA[17]	50	TMS	92	D[0]	134	PA[53]	176	PB[2]
9	PB[48]	51	TCK	93	D[1]	135	PB[20]	177	PA[34]
10	PA[16]	52	TRST*	94	D[2]	136	PA[52]	178	PB[1]
11	VAA5	53	VAA3	95	D[3]	137	PB[19]	179	PA[33]
12	GND	54	VAA5	96	D[4]	138	PA[51]	180	PB[0]
13	PB[47]	55	GND	97	D[5]	139	PB[18]	181	PA[32]
14	PA[15]	56	IOR	98	D[6]	140	PA[50]	182	GND
15	PB[46]	57	VAA5	99	D[7]	141	PB[17]	183	LD
16	PA[14]	58	IOG	100	VSYNC*	142	PA[49]	184	PB[63]
17	PB[45]	59	GND	101	SDA	143	PB[16]	185	PA[31]
18	PA[13]	60	VAA5	102	GND	144	PA[48]	186	PB[62]
19	PB[44]	61	IOB	103	GND	145	GND	187	PA[30]
20	PA[12]	62	VAA5	104	VAA3	146	VAA5	188	PB[61]
21	PB[43]	63	GND	105	GPCLK	147	PB[15]	189	PA[29]
22	PA[11]	64	VAA5	106	SCL	148	PA[47]	190	PB[60]
23	PB[42]	65	VREF	107	SC*	149	PB[14]	191	PA[28]
24	PA[10]	66	FSADJ	108	STSCAN	150	PA[46]	192	PB[59]
25	PB[41]	67	GND	109	SCEN*	151	PB[13]	193	PA[27]
26	PA[9]	68	VAA5	110	FIELD	152	PA[45]	194	PB[58]
27	PB[40]	69	COMP	111	PB[31]	153	PB[12]	195	PA[26]
28	PA[8]	70	COMP2	112	PA[63]	154	PA[44]	196	PB[57]
29	VAA5	71	RANGE	113	PB[30]	155	PB[11]	197	PA[25]
30	GND	72	VAA5	114	PA[62]	156	VAA3	198	PB[56]
31	PB[39]	73	GND	115	PB[29]	157	PA[43]	199	PA[24]
32	PA[7]	74	GND	116	PA[61]	158	PB[10]	200	VAA5
33	PB[38]	75	XTAL[2]	117	PB[28]	159	PA[42]	201	GND
34	PA[6]	76	XTAL[1]	118	PA[60]	160	PB[9]	202	PB[55]
35	PB[37]	77	VAA5	119	PB[27]	161	PA[41]	203	PA[23]
36	PA[5]	78	GND	120	PA[59]	162	PB[8]	204	PB[54]
37	PB[36]	79	GND	121	PB[26]	163	PA[40]	205	PA[22]
38	PA[4]	80	CLOCK	122	PA[58]	164	GND	206	PB[53]
39	PB[35]	81	CLOCK*	123	PB[25]	165	VAA5	207	PA[21]
40	PA[3]	82	CSYNC*	124	PA[57]	166	PB[7]	208	PB[52]
41	PB[34]	83	RESET*	125	PB[24]	167	PA[39]		
42	PA[2]	84	DRAWING*	126	PA[56]	168	PB[6]		

Table 3. 160-pin PQFP Pin Labels

Pin	Pin Label	Pin	Pin Label	Pin	Pin Label	Pin	Pin Label	Pin	Pin Label
1	VAA3	33	PA[0]	65	CE*	97	N/C	129	PA[39]
2	PA[20]	34	GND	66	R/W	98	PA[56]	130	N/C
3	PA[19]	35	TDO	67	C[0]	99	GND	131	PA[38]
4	N/C	36	TDI	68	C[1]	100	VAA5	132	PA[37]
5	PA[18]	37	TMS	69	LB*	101	N/C	133	PA[36]
6	PA[17]	38	TCK	70	GND	102	PA[55]	134	N/C
7	PA[16]	39	TRST*	71	D[0]	103	N/C	135	PA[35]
8	VAA5	40	VAA3	72	D[1]	104	PA[54]	136	PA[34]
9	GND	41	GND	73	D[2]	105	PA[53]	137	PA[33]
10	N/C	42	IOR	74	D[3]	106	N/C	138	N/C
11	PA[15]	43	VAA5	75	D[4]	107	PA[52]	139	PA[32]
12	PA[14]	44	IOG	76	D[5]	108	PA[51]	140	GND
13	PA[13]	45	GND	77	D[6]	109	N/C	141	LD
14	N/C	46	IOB	78	D[7]	110	PA[50]	142	N/C
15	PA[12]	47	VAA5	79	VSYNC*	111	PA[49]	143	PA[31]
16	PA[11]	48	GND	80	SDA	112	PA[48]	144	PA[30]
17	N/C	49	VREF	81	VAA3	113	GND	145	N/C
18	PA[10]	50	FSADJ	82	GND	114	VAA5	146	PA[29]
19	PA[9]	51	VAA5	83	GPCLK	115	N/C	147	N/C
20	PA[8]	52	COMP	84	SCL	116	PA[47]	148	PA[28]
21	VAA5	53	COMP2	85	SC*	117	PA[46]	149	PA[27]
22	GND	54	RANGE	86	STSCAN	118	PA[45]	150	PA[26]
23	N/C	55	VAA5	87	SCEN*	119	PA[44]	151	PA[25]
24	PA[7]	56	GND	88	FIELD	120	VAA3	152	N/C
25	N/C	57	XTAL[2]	89	PA[63]	121	N/C	153	PA[24]
26	PA[6]	58	XTAL[1]	90	PA[62]	122	PA[43]	154	VAA5
27	N/C	59	VAA5	91	PA[61]	123	N/C	155	GND
28	PA[5]	60	GND	92	PA[60]	124	PA[42]	156	N/C
29	PA[4]	61	CLOCK	93	PA[59]	125	PA[41]	157	PA[23]
30	PA[3]	62	CLOCK*	94	N/C	126	PA[40]	158	PA[22]
31	PA[2]	63	CSYNC*	95	PA[58]	127	GND	159	PA[21]
32	PA[1]	64	RESET*	96	PA[57]	128	VAA5	160	N/C

MPU Interface

As illustrated in Figure 3, the Bt497A/8A supports a standard Microprocessor Unit (MPU) bus interface, which can access the internal control registers and color palettes. The on-chip color palette RAM and cursor color registers support color updating with minimum contention to the display refresh process.

All MPU words are 32 bits in length and require four CE* cycles. Accesses can be performed in two modes, direct and indirect, that are differentiated by the encoding of the control bits C[0] and C[1], as shown in Table 4. The indirect access requires an address pointer that can be written via the MPU port; the direct access pointer is read through the MPU port. All indirect MPU accesses generate an auto-increment function in the word dimension. The LB* signal is asserted on the first CE* cycle to indicate the least significant byte for every MPU access. D[0] corresponds to the Least Significant Bit (LSB) of each byte. Figure 4 illustrates the MPU read timing.

Table 5 and Table 6 illustrate how the C0 and C1 control inputs work in conjunction with the internal address register to specify which configuration or cursor function register will be accessed by the MPU. The MPU will zero fill reserved bits on data reads.

Toggling the RESET* pin presets the internal registers to the values shown in Table 5 and Table 6.

Figure 3. Detailed Functional Block Diagram

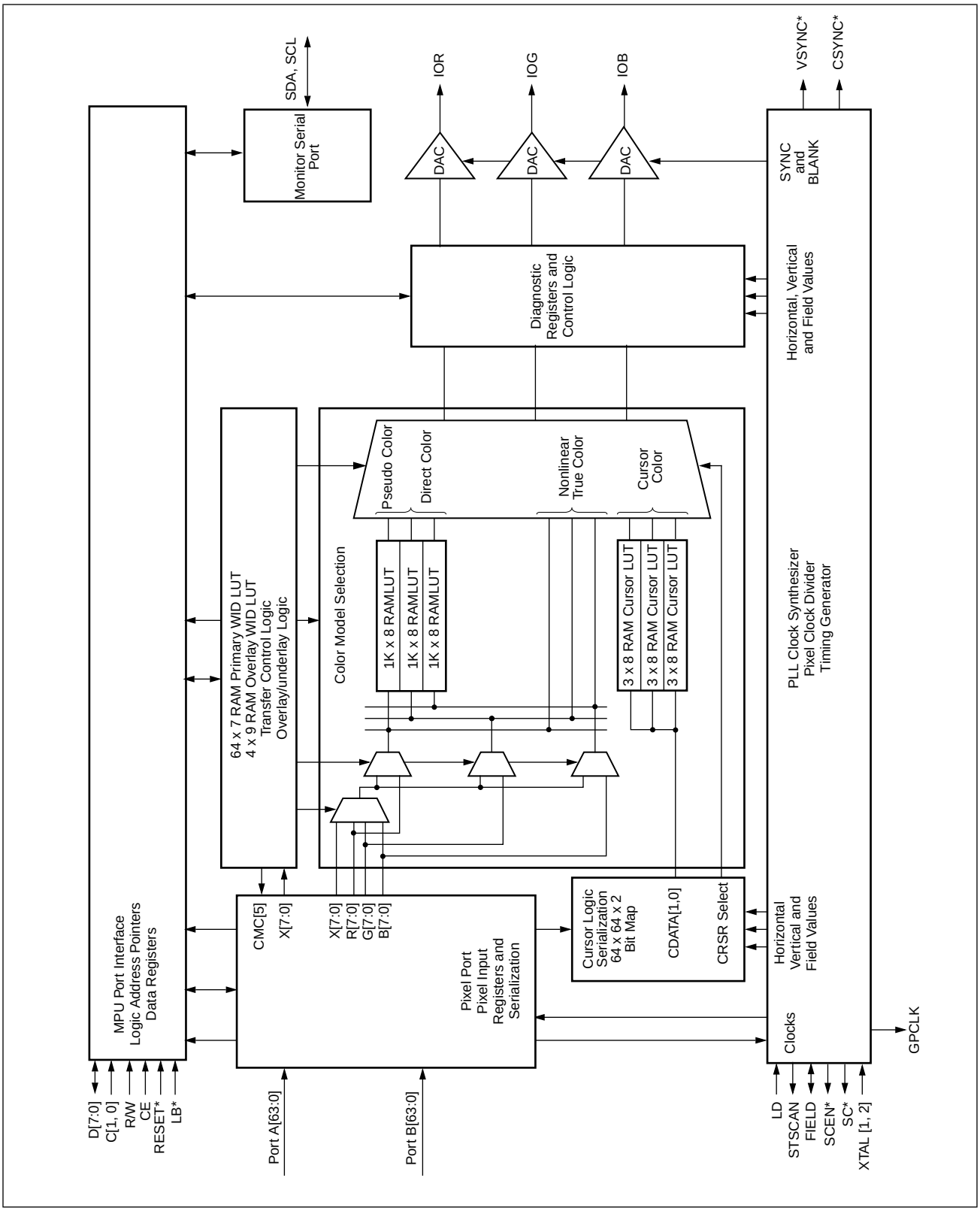


Table 4. MPU Interface Address Map-Control Field Definition

Function	Access Type	Control Field	
		Control Bit 1	Control Bit 0
Cursor Functions	Indirect	1	1
Cursor Address Pointer	Direct	1	0
Configuration Functions	Indirect	0	1
Configuration Address Pointer	Direct	0	0

Figure 4. MPU Full-Word Access Timing Diagram

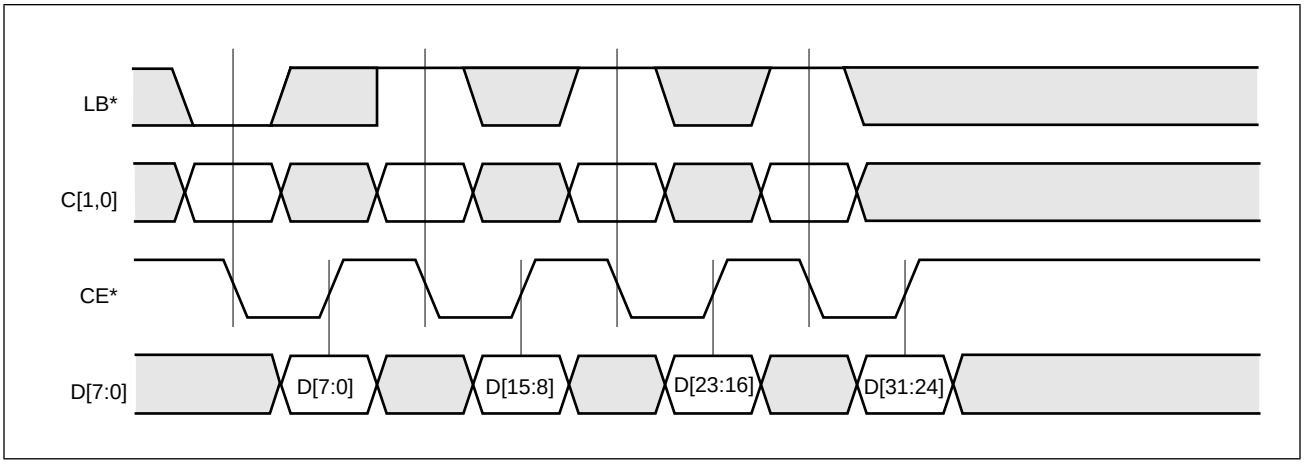


Table 5. Configuration Address Operation *(1 of 2)*

Pointer Address	C[1,0]	Reset Value	Function
$xxxx	00	N/R	Configuration Address Pointer Register
$0000	01	$227	Pixel PLL Control Register
$0001	01	$A1C	General Purpose PLL Control Register
$0002–$0FFF	01	N/A	Reserved
$1000	01	N/R	Pixel Format Control Register
$1001	01	$0	User Control Register
$1002–$1FFF	01	N/A	Reserved
$2000–$20FF	01	N/R	Color Lookup Palette (Red, Green, Blue, xx), Table 0
$2100–$21FF	01	N/R	Color Lookup Palette, Table 1
$2200–$22FF	01	N/R	Color Lookup Palette, Table 2
$2300–$23FF	01	N/R	Color Lookup Palette, Table 3
$2400–$30FF	01	N/A	Reserved
$3100–$3103	01	N/R	Shadow-Overlay Window Lookup Table
$3104–$311F	01	N/A	Reserved
$3120–$3123	01	N/R	Active-Overlay Window Lookup Table
$3124–$314F	01	N/A	Reserved
$3150	01	$0	Window Transfer Control Register
$3151	01	N/R	Transparent Mask Control Register
$3152	01	N/R	Transparent Color Key Register
$3153	01	N/R	Window Address Mask Register
$3154–$31FF	01	N/A	Reserved
$3200–$323F	01	N/R	Shadow-Primary Window Lookup Table
$3240–$327F	01	N/R	Active-Primary Window Lookup Table
$3280–$4FFF	01	N/A	Reserved
$5000	01	$00XXXXXX	Signature Analysis Control Register
$5001	01	$0	DAC Control Register
$5002–$5FFF	01	N/A	Reserved
$6000	01	$0	Timing Generator Control Register
$6001	01	N/R	Vertical Blank Negation Point Register
$6002	01	N/R	Vertical Blank Assertion Point Register
$6003	01	N/R	Vertical Sync. Negation Point Register
$6004	01	N/R	Vertical Sync. Assertion Point Register

Table 5. Configuration Address Operation *(2 of 2)*

Pointer Address	C[1,0]	Reset Value	Function
$6005	01	N/R	Horizontal Serration Negation Point Register
$6006	01	N/R	Horizontal Blank Negation Point Register
$6007	01	N/R	Horizontal Blank Assertion Point Register
$6008	01	N/R	Horizontal Sync. Negation Point Register
$6009	01	N/R	Horizontal Sync. Assertion Point Register
$600A	01	N/R	Horizontal SCEN Negation Point Register
$600B	01	N/R	Horizontal SCEN Assertion Point Register
$600C	01	N/R	Equalizing Pulse Negation Point Register
$600D	01	N/R	Equalization Interval Negation Point Register
$600E	01	N/R	Equalization Interval Assertion Point Register
$600F	01	$0	Timing Generator Vertical Counter
$6010	01	$0	Timing Generator Horizontal Counter
$6011	01	N/R	Timing Generator Test Register
$6012–$7FFF	01	N/A	Reserved
$8000	01	$A236E1AD	Device Identification Register
$8001	01	$3	Monitor Port Data Register
$8002	01	N/R	Monitor Port Sense Register
$8003–$FFFF	01	N/A	Reserved

Note: N/R = Register exists, but is not resettable. N/A = Reserved addresses indicate no register exists at the given pointer addresses. User should not attempt to access reserved addresses.

Table 6. Cursor Address Operation

Pointer Address	C[1,0]	Reset Value	Function
$xxx	10	N/R	Cursor Address Pointer Register
$000–$07F	11	N/R	Cursor RAM–Plane0
$080–$0FF	11	N/R	Cursor RAM–Plane1
$100	11	$0	Cursor Control Register
$101–$103	11	N/R	Cursor Color Lookup Table (Red, Green, Blue, xx)
$104	11	N/R	Cursor Position Register
$105–$1FF	11	N/A	Reserved

Note: N/R = Register exists, but is not resettable. N/A = Reserved addresses indicate no register exists at the given pointer addresses. User should not attempt to access reserved addresses.

Reading/Writing Color Data

To write color data, the MPU loads the appropriate address pointer with the address of the color palette RAM location or cursor color register to be modified. The MPU performs four successive write cycles: red, green, blue, and a dummy value. During the last write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then auto-increments to the next location, which the MPU can modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address pointer with the address of the color palette RAM location or cursor color register to be read. The MPU performs four successive read cycles: red, green, blue, and 00. Following the last read cycle, the address register increments to the next location, which the MPU can view by simply reading another sequence of color data. Note that MPU reads have priority over display refresh reads to the shared color palette read port. To avoid visual artifacts, it is recommended that MPU reads be restricted to the retrace intervals.

Additional Information

Although the color and cursor color registers are dual ported, if the pixel data is addressing the same palette entry being written to by the MPU during the write cycle, a maximum of 1 pixel may be disturbed. All control registers can be written to or read by the MPU at any time. To prevent pixels from being disturbed during writes to certain control registers, the DAC outputs should be disabled through the User Control Register. The setup times shown in the AC Characteristics section are the minimum required to internally capture the data.

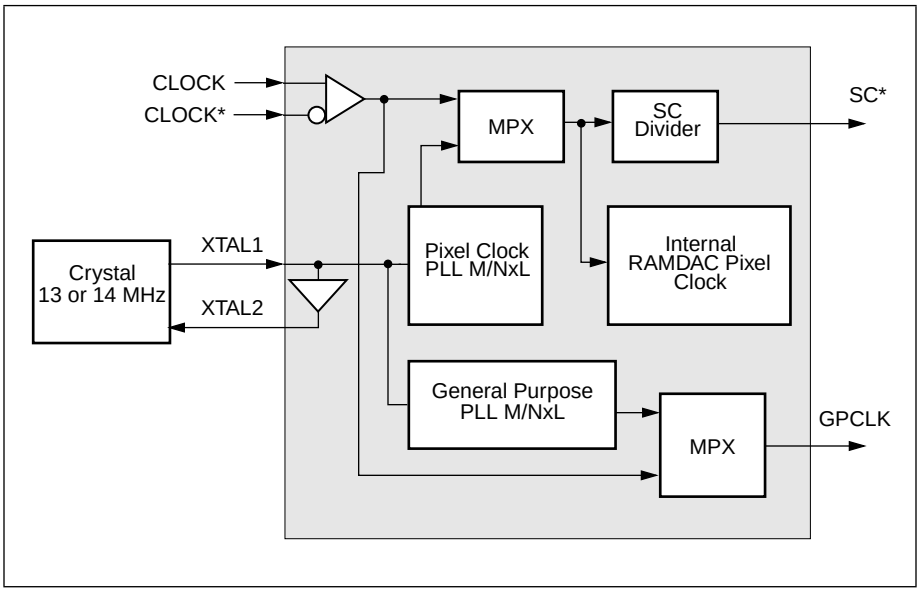
Note that if an invalid address is loaded into the address pointer, data written to the device will be ignored and invalid data will be read by the MPU. This is not recommended, as it could cause problems in Bt497A/8A-compatible products.

If an incomplete MPU access occurs, (less than four CE* cycles between LB*s) that access and the following full access will be ignored.

Clock Generation

The Bt497A/8A has two on-board PLLs for generating the pixel clock and the GP-CLK output pin as shown in Figure 5. The pixel clock is fully programmable, able to generate over 500 unique pixel clock frequencies using a single crystal.

Figure 5. PLL Clock Generation Block Diagram

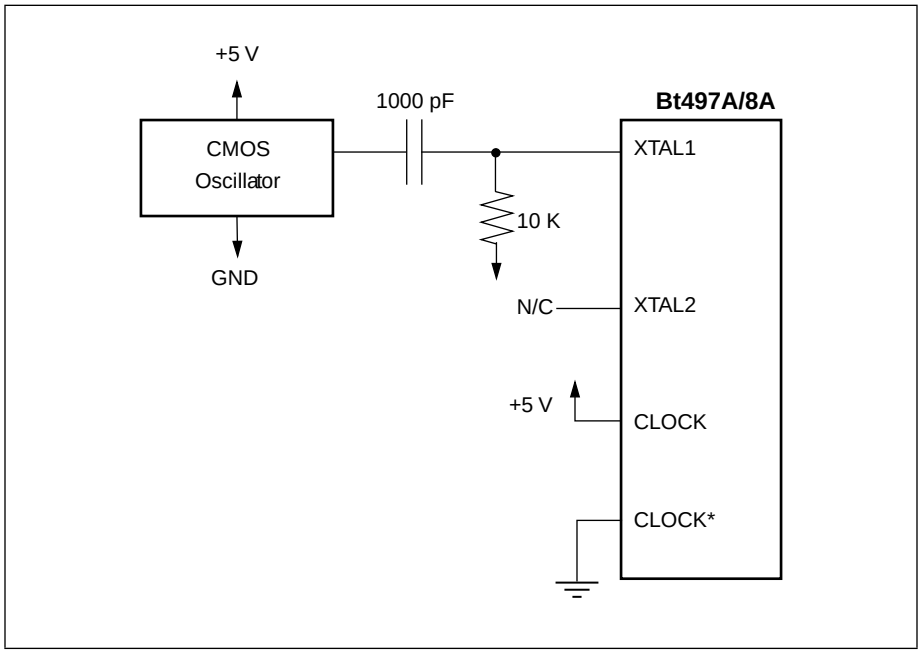


The advanced PLLs contain internal loop filters to provide maximum noise immunity and to reduce jitter. Except for the reference crystal or oscillator, no external components or adjustments are necessary.

The PLLs use an M/(L x N) scheme to provide precise frequencies. The M, N, and L values can be programmed through the command registers with a variety of values, which generally provide frequency granularity that averages less than 1 MHz. M is a binary 7-bit value, N is a binary 4-bit value, and L is selectable to be a value of one, two, four, or eight.

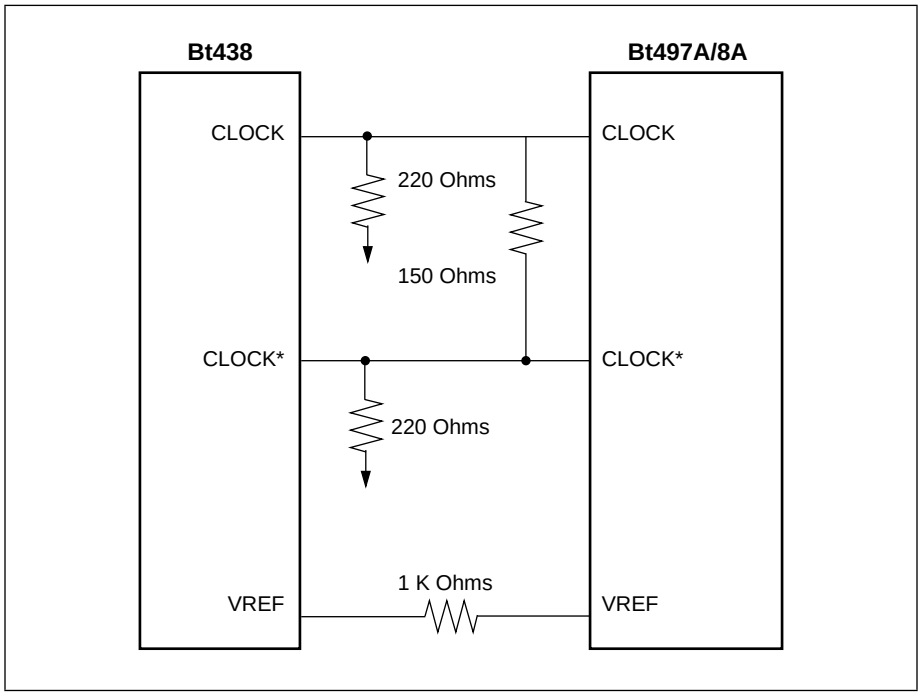
An oscillator reference can also be used by connecting the oscillator's output to the XTAL1 input using a 10000 pf coupling capacitor, as shown in Figure 6. For this configuration, the XTAL2 pin should be left disconnected.

Figure 6. CMOS Oscillator Interface



As an alternative to using the PLLs for clock generation, the Bt497A/8A is designed to accept differential clock signals (CLOCK and CLOCK* shown in Figure 7). These clock inputs can be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (220 Ω to GND) that should be located as close to the driving source as possible. A 150 Ω chip resistor near the Bt497A/8A pins is also needed to ensure proper termination.

Figure 7. Differential Clock Interface



A serial clock, SC*, is generated for the external clocking of the VRAM frame buffer and for loading pixel data. The serial clock frequencies are either one-half or one-fourth of the pixel clock frequency, Fp, depending on the pixel format selected, as shown in Table 7. The SC* output should be buffered and inverted and then used to drive the LD input and clock the frame buffer. For proper operation, the delay through the buffer should not exceed the limits in the AC specifications.

Table 7. Serial Clock Frequencies

Pixel Format	SC Frequency
2:1	Fp/2
4:1	Fp/4
4/2:1	Fp/2
8/2:1	Fp/4

With the assertion of RESET*, SC* is forced high. When RESET* is released, the first falling edge of SC* will be released by the next edge of the pixel clock.

Frame Buffer Interface

The Bt497A/8A incorporates internal latches and multiplexers that enable pixel data to be transferred from the frame buffer at VRAM data rates. On the rising edge of LD color information, 2 or 4 consecutive pixels are latched into the device. Two additional pixel formats are supported, 4/2:1 and 8/2:1, in which 4 or 8 consecutive pixels are latched in two load cycles. In each case, the SC* and LD rates are at one-half or one-fourth of the pixel clock rates. The pixel formats are controlled through the Pixel Format Control Register and are shown in Figures 8 through 13.

As shown in Table 8, the Bt498A pixel port is configured into two ports, A and B, which accommodate double-buffered operation for animation. The port selection is made by decoding the X field of each pixel, as explained in the Color Model sections. Each port is divided into 8 bytes, in which the LSB represents the LSB of each color, window attribute, or overlay, for a total of 128 inputs. The Bt497A is a 64-bit pixel port option, port A only, packaged in a 160-pin Plastic Quad Flatpack (PQFP). Because of the smaller port size, the only pixel formats supported are the 2:1 and 4/2:1.

Internal logic maintains an internal LOAD signal synchronous to the pixel clock, and is guaranteed to follow the LD signal by at least one but not more than three clock cycles. This LOAD signal transfers the registered pixel and overlay data into a second set of registers, which are then internally multiplexed at the pixel clock rate. Therefore, the LD may be phase shifted in any amount relative to the clock source, pseudo ECL or PLL. As a result, the pixel data is registered on the rising edge of LD independent of the internal or external clock phase.

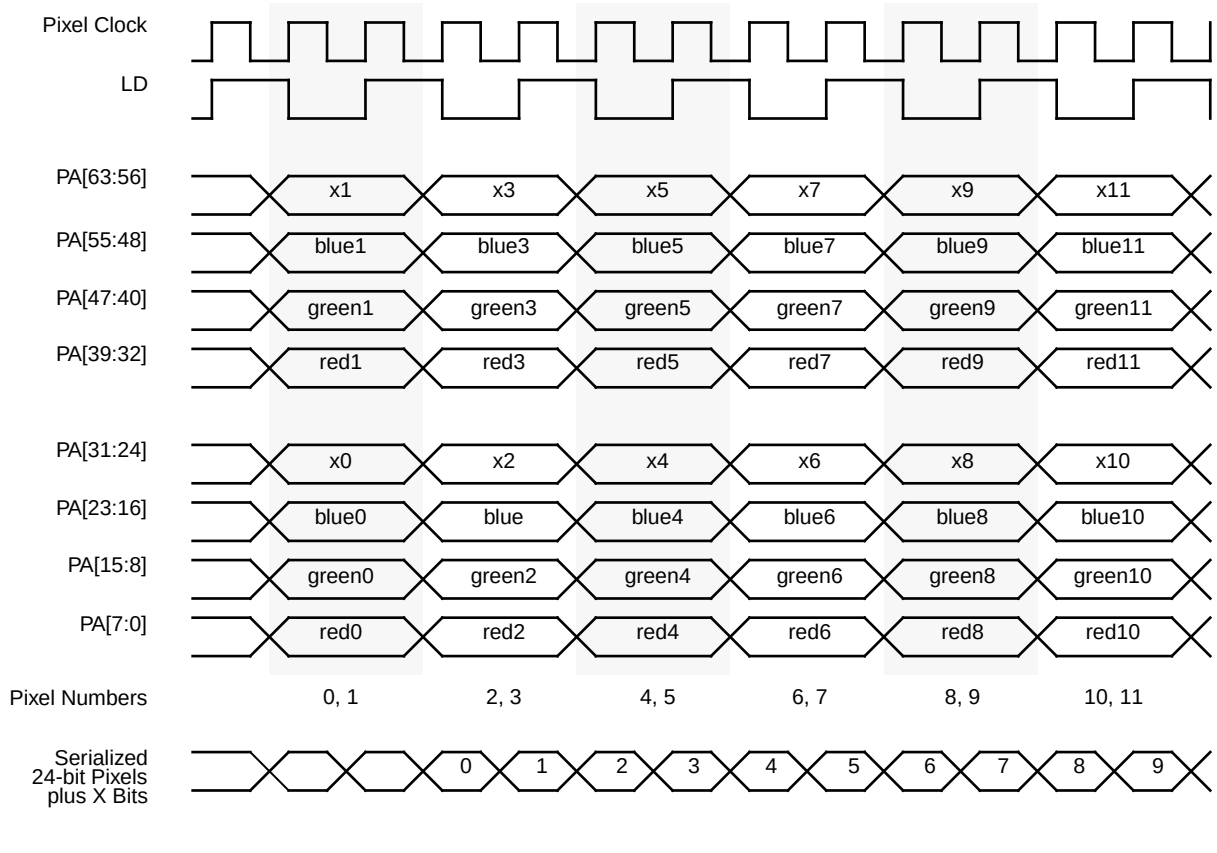
Table 8. Pixel Port Naming Convention *(1 of 2)*

Pixel Port	Device Bits
B (Not available on Bt497A)	PB[63:56]
	PB[55:48]
	PB[47:40]
	PB[39:32]
	PB[31:24]
	PB[23:16]
	PB[15:8]
	PB[7:0]

Table 8. Pixel Port Naming Convention *(2 of 2)*

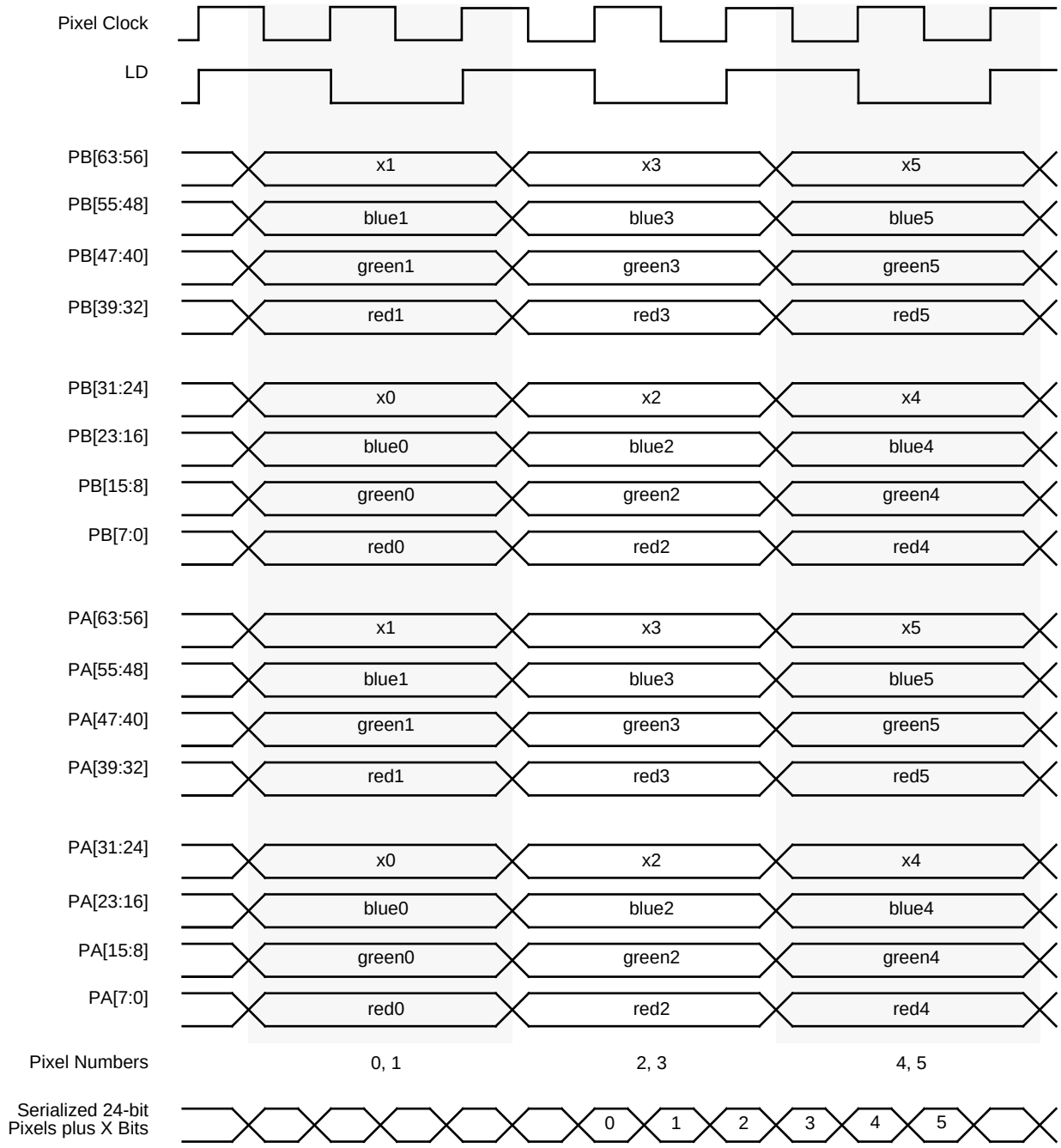
Pixel Port	Device Bits
A	PA[63:56]
	PA[55:48]
	PA[47:40]
	PA[39:32]
	PA[31:24]
	PA[23:16]
	PA[15:8]
	PA[7:0]

Figure 8. 2:1 Single-Buffered Pixel Format



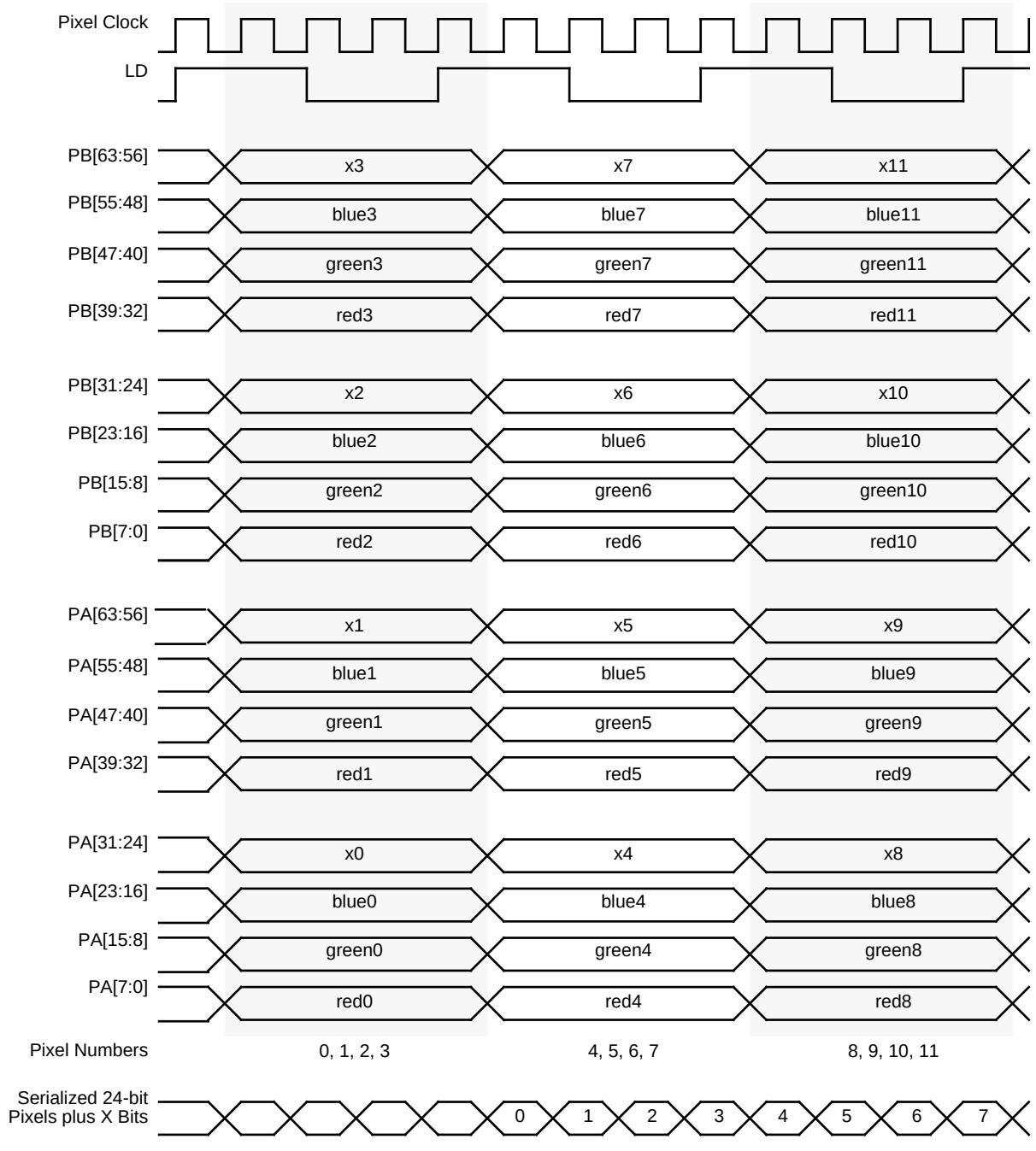
Note: This mode is valid for pixel clock Fp ≤ 160 MHz. LD frequency = Fp/2 MHz.

Figure 9. 2:1 Double-Buffered Pixel Format



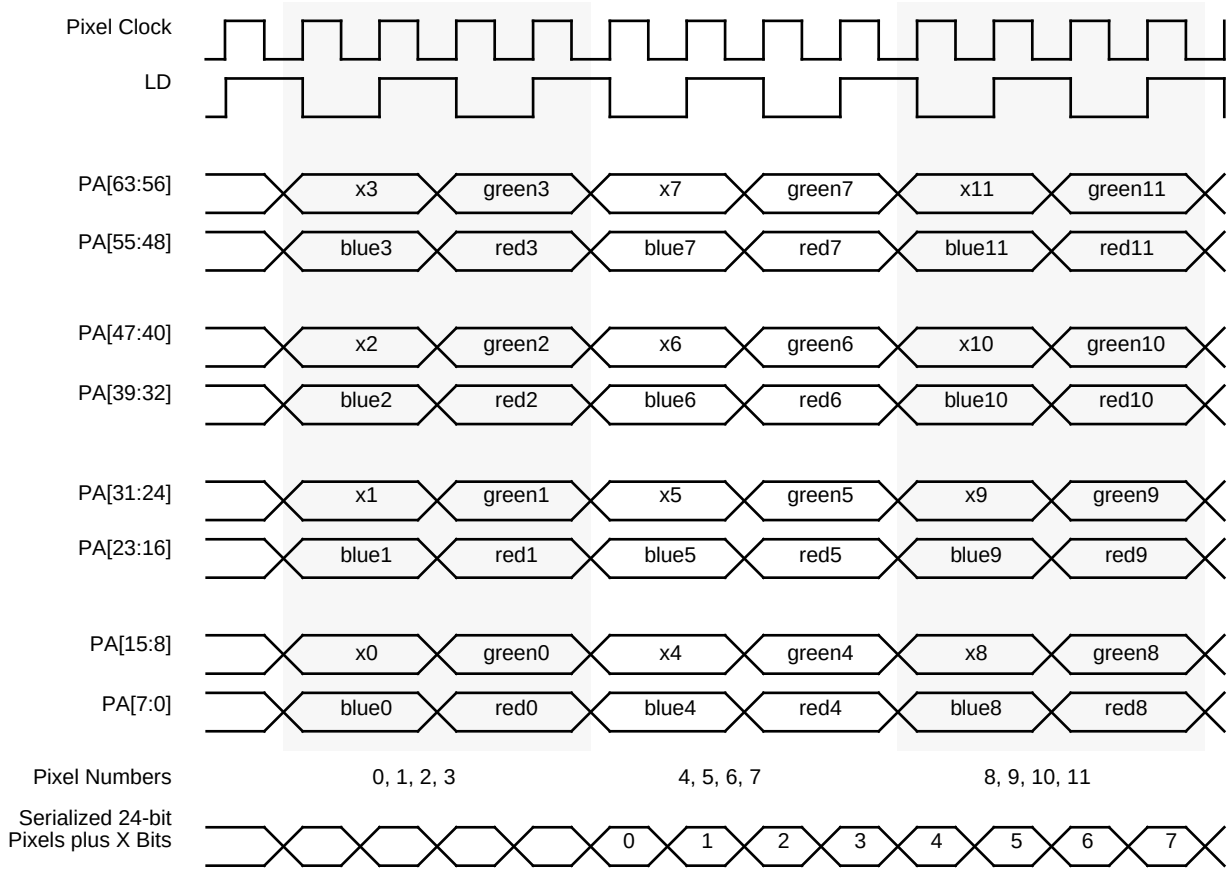
Note: This mode is valid for pixel clock Fp ≤ 160 MHz. LD frequency = Fp/2 MHz. Not valid for the Bt497A.

Figure 10. 4:1 Pixel Format



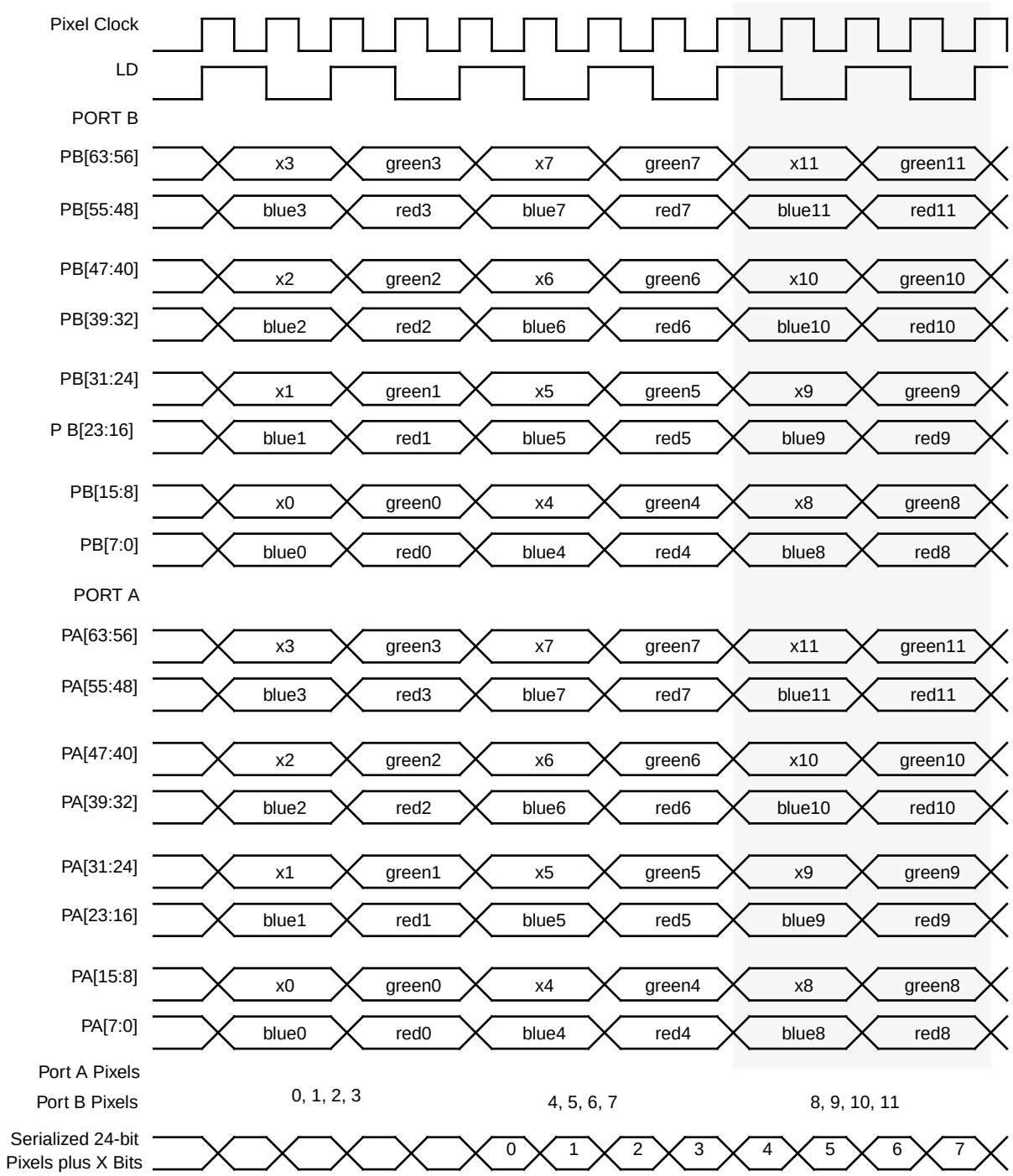
Note: This mode is valid for pixel clock Fp ≤ 240 MHz. LD frequency = Fp/4 MHz. Not valid for the Bt497A.

Figure 11. 4/2:1 Single-Buffered Pixel Format



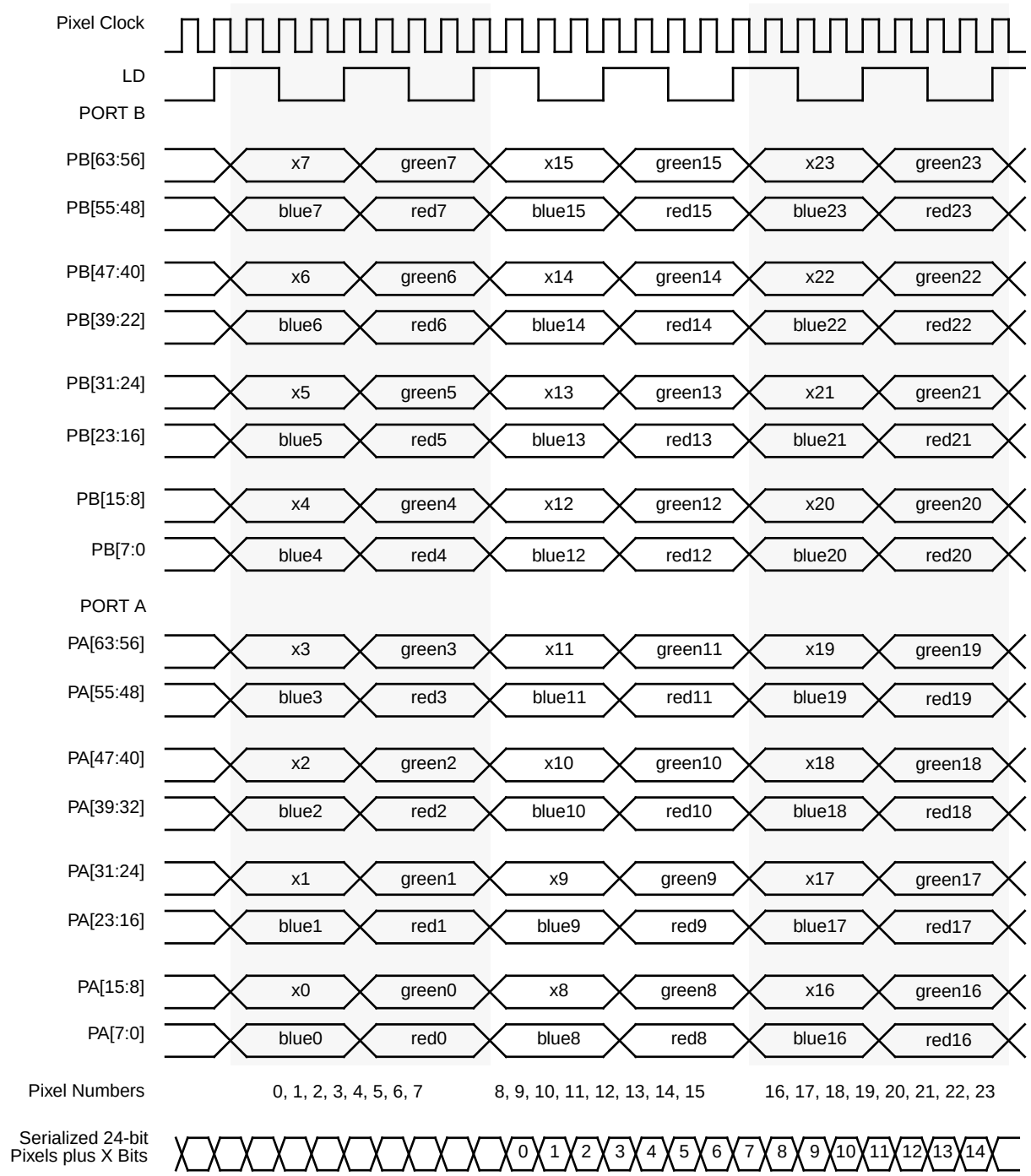
Note: This mode is valid for pixel clock Fp ≤ 160 MHz. LD frequency = Fp/2 MHz.

Figure 12. 4/2:1 Double-Buffered Pixel Format



Note: This mode is valid for pixel clock Fp ≤ 160 MHz. LD frequency = Fp/2 MHz. Not valid for the Bt497A.

Figure 13. 8/2:1 Pixel Format



Note: This mode is valid for pixel clock Fp ≤ 240 MHz. LD frequency = Fp/4 MHz. Not valid for the Bt497A.

Color Model Selection

As shown in Figure 14, the Bt497A/8A contains specialized logic that transforms pixel data into color information.

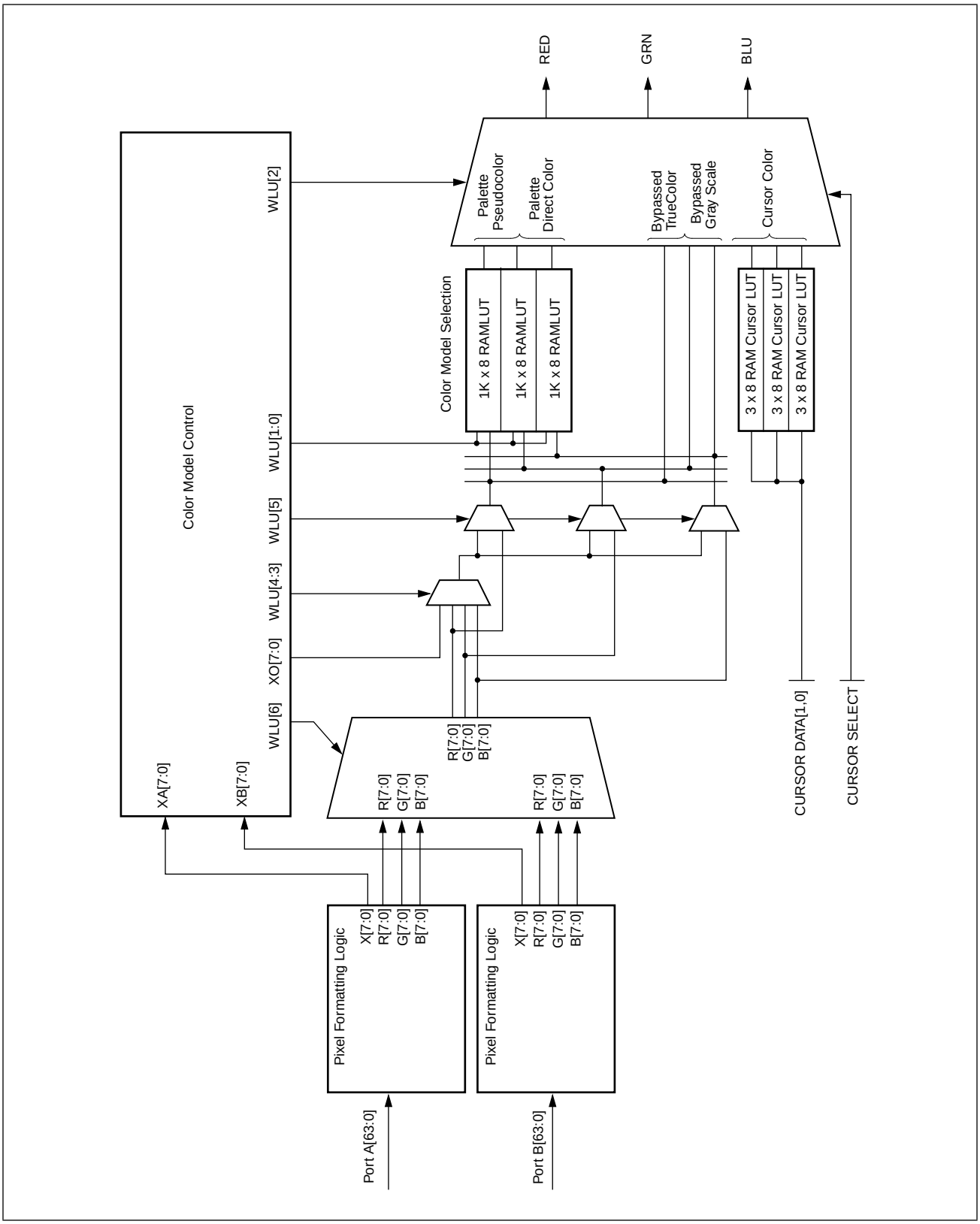
The diagrams describing the various pixel formats include a data field named X. The contents of this field are the dynamic primary input to the Color Model Control (CMC) logic, which is described later. The CMC outputs, labeled in Figure 14 as WLU (for "Window Look-Up"), serve to select the pixel source, e.g., port A or B, and to associate the pixel with a particular color model. The term Color Model refers to the final category of mux-selection and resultant color state that drives the RED, GRN and BLU outputs in Figure 14. A Color Model is fully determined by the WLU[6:0] outputs from the CMC block. There is a correspondence between the WLU bit values and specific CMC[15:0] bits which are described later. Table 9 describes the various Color Model effects of different WLU values in Figure 14.

The X field is a component of every pixel and its content may differ in contiguous pixels. Therefore, port and color model selection is performed for each individual pixel. The pixel formats are divided into two broad categories: single-buffered format and double-buffered format. The Bt497A can only support the 2:1 and 4/2:1 formats running single-buffered. It has no Port B available. The Bt498A supports all formats, including the double-buffered modes. In the WIDSEP8 mode, described later, the X field from Port A and the X field from Port B are both used. In 4:1 and 8/2:1 the X field from each pixel is used. Bit WLU[6] is don't care for 4:1 and 8/2:1 formats.

Table 9. Window Look-Up Attributes

WLU bits	Description	Value
WLU[6]	Double Buffering	0 = Buffer A 1 = Buffer B
WLU[5]	Color Depth	0 = 8 Bits/pixel 1 = 24 Bits/pixel
WLU[4:3]	Pseudocolor Source	00 = X[7:0] 01 = R[7:0] 10 = G[7:0] 11 = B[7:0]
WLU[2]	Color Lookup	0 = Bypass 1 = Palette
WLU[1:0]	Palette Table Selection	00 = Table 0 01 = Table 1 10 = Table 2 11 = Table 3

Figure 14. Color Model Selection Mechanism



Color Model Control

The Color Model Control (CMC) block introduced in Figure 14 is now fully described. The dynamic input is the X field which is output from the pixel unpacking logic. X is generated from both port A and port B, if the pixel format is 2:1 or 4/2:1. If the format is 4:1 or 8/2:1, then X is associated with the single extended pixel port. For these formats, there is only one buffer with its pixel value and corresponding X field. The X field is dynamic in that it may change with any new pixel position.

Static, or seldom changing inputs to CMC come from the User Control Register, the Window Address Control Mask Register, the Transparent Color Mask Register, the Transparent Color Key Register, and the Transfer Control Logic. In addition, the Window Look-Up Tables (WLUTs, described below) require standard MPU access. The outputs of the CMC are WLU[6:0], described in the previous section, and XO[7:0]. XO is the final X output bus which expresses into the Color Model Selection logic as a potential pixel source.

There are two main processes in the CMC: WLUT indexing and Overlay enable. The remainder of this section describes WLUT indexing and the composition of XO. A later section describes Overlay/Underlay operation.

WLUT indexing refers to the process of generating address inputs to the two active WLUTs in the CMC. These are: the Primary WLUT (PWLUT), which has 64 entries, with each entry 7 bits wide; and the Overlay WLUT (OWLUT), which has 4 entries, each being 11 bits wide. Both the PWLUT and the OWLUT are high speed Random Access Memories (RAMs) that are able to switch their entry outputs at pixel rate. These 2 WLUTS are shown in Figure 15, along with the other main CMC functions. Each WLUT has a shadow WLUT associated with it, that is the same size as its active reference RAM. The purpose of the shadow WLUTs is to provide a smooth, synchronous updating mechanism for changing the contents of the active WLUTs. When the UPDATE signal is asserted, the full contents of the shadow PWLUT are loaded directly into the active PWLUT. Simultaneously, the active OWLUT is loaded with the full contents of the shadow OWLUT. The conditions that cause UPDATE assertion are described later. Only the active PWLUT and OWLUT are involved in Color Model Control. All WLUT references in the remainder of this section are understood to indicate the Active PWLUT and OWLUT.

Refer to Figure 15. The “WM” control refers to “Window Mode,” a 2-bit control that is set by the User Control Register. The three Window Modes are: C = Combined, S4 = Separate_4, and S8 = Separate_8. These terms refer to the sources of Overlay Comparison versus that for PWLUT indexing. It is seen that the state of WM affects directly the index sources for the PWLUT and the OWLUT, as well as the mapping for the XO output. The XA and XB inputs come directly from the Pixel Unpacking logic. Review Table 10 to clarify the dependencies of these primary

inputs on pixel formats. It shows that the Separate_8 window mode is NOT supported for 4:1 and 8/2:1 pixel formats, since there is no concept of XB. The Combined and Separate_4 modes ARE supported for all pixel formats. Note that MPU access connections have been omitted in Figure 15 for clarity.

Again in Figure 15, the PMASK and OMASK blocks refer to the respective fields from the Window Address Mask Register. These blocks allow restriction of the selected entries within the two WLUTs. Program the fields with all 1s to allow maximum WLUT entry selection. The masking operation is described further in the respective Internal Register section.

After masking, the PWLUT and OWLUT are addressed and the selected entries generate corresponding output states. In the Figure, these outputs are referred to as PCM (for Primary Color Model) and OCM (for Overlay Color Model) respectively. At the Overlay Mux, the signal DO_OVLY selects between all of PCM or a subset of OCM to generate the final CMC state. The bit indexes for these busses are shown as greater than the widths of either WLUT. That is because the CMC, PCM, and OCM busses are referenced with the linked bit-assignments given in the WLUT 16 bit MPU programmed values. These assignments are shown in Table 11. The mapping between the MPU Color Model WLUT bits and the actual bit positions within the OWLUT and PWLUT RAMS is also given in Table 11. The MPU interface to the PWLUT and OWLUT will perform the translation between the expanded bit positions of Table 11 and the actual compressed bit positions in the 2 WLUTs. Note, the first Table 11 function, Double Buffering, is “don't-care” if the Pixel Format is either 4:1 or 8/2:1.

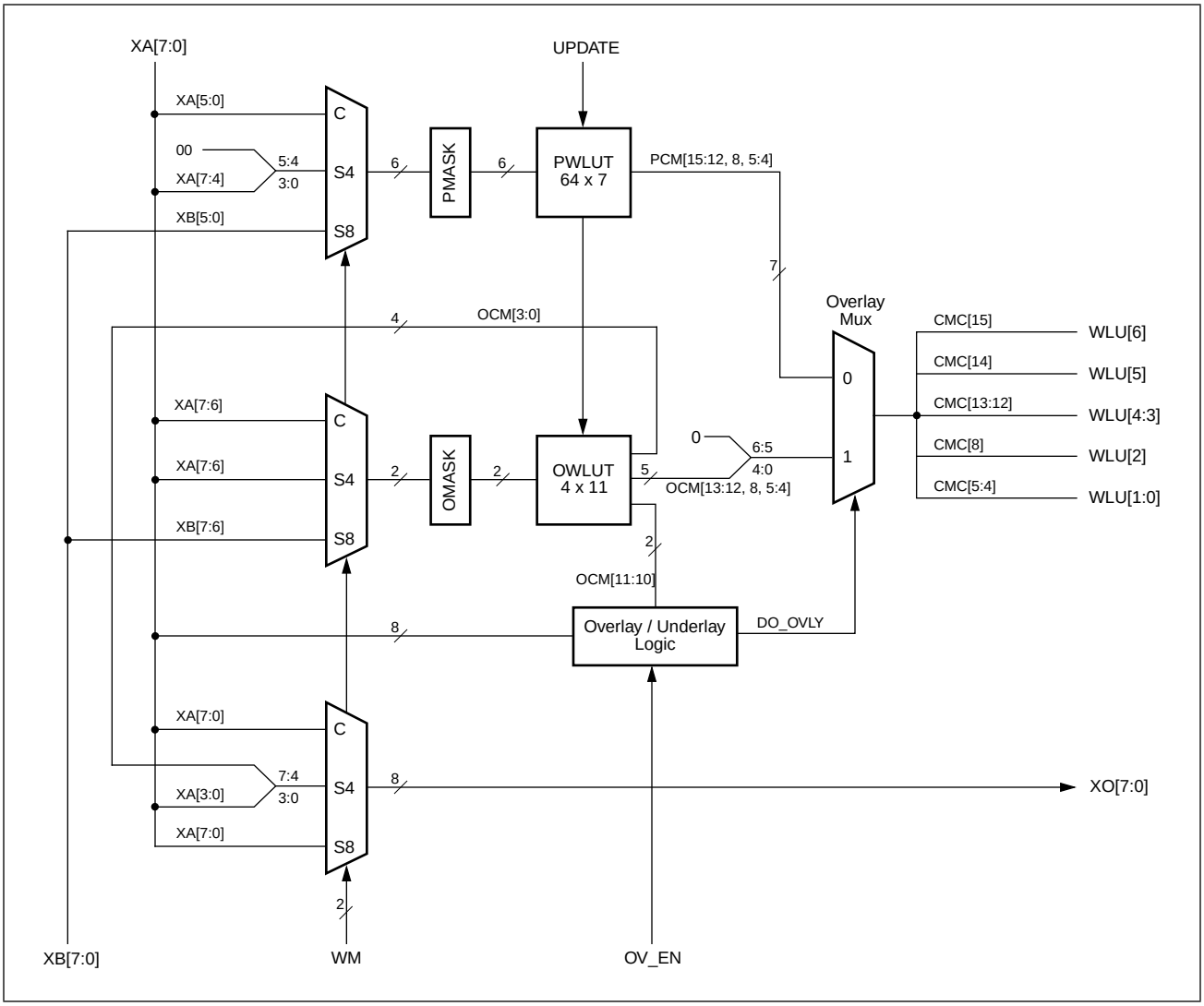
Table 10. Pixel Format Dependencies

Pixel Format	XA Source	XB Source	Separate_8 mode
2:1 and 4/2:1	64-pin port_A	64-pin port_B	Supported
4:1 and 8/2:1	128-pin port_A AND port_B	N/A	NOT Supported

Table 11. Color Model Control WLUT Linked Bit Definitions

Bit(s)	Function/Assignment	OCM State	OWLUT Mapping	PCM State	PWLUT Mapping
15	Double Buffering 0 = Buffer A 1 = Buffer B	<force 0>	N/A	PCM[15]	PWLUT[6]
14	Color Depth 0 = 8 Bits/pixel (Pseudo-color) 1 = 24 Bits/pixel (True-color)	<force 0>	N/A	PCM[14]	PWLUT[5]
13, 12	Pseudocolor Source 00 = X0[7:0] 01 = R[7:0] 10 = G[7:0] 11 = B[7:0]	OCM[13:12]	OWLUT[10:9]	PCM[13,12]	PWLUT[4:3]
11, 10	Overlay Type 00 = No Overlay 01 = Transparent Overlay 10 = Opaque Overlay 11 = Reserved	OCM[11,10]	OWLUT[8:7]	N/A	N/A
9	Reserved	N/A	N/A	N/A	N/A
8	Color Lookup 0 = Bypass the Palette 1 = Index thru Palette	OCM[8]	OWLUT[6]	PCM[8]	PWLUT[2]
7, 6	Reserved	N/A	N/A	N/A	N/A
5, 4	Palette Table 00 = Table 0 01 = Table 1 10 = Table 2 11 = Table 3	OCM[5,4]	OWLUT[5:4]	PCM[5,4]	PWLUT[1:0]
3–0	Palette Section, Separate_4 $0 = Section 0 $1 = Section 1 $2 = Section 2 : $F = Section 15	OCM[3:0]	OWLUT[3:0]	N/A	N/A

Figure 15. Color Model Control



Color Lookup Operations

Color Lookup refers to the final selection of a 24-bit color value that is then input to the Bt497A/8A DACs. This is shown on the right side of Figure 14. Color Lookup includes the Palette RAM, the Cursor LUT, and the Bypass Mux. The Palette refers to the 3 1Kx8 RAMs that store color values which are indexed (addressed) by the pixel value delivered after Color Model selection. The Cursor information always has highest priority. Whenever CURSOR_SELECT is asserted, then the Color Lookup will be one of the 3 Cursor LUT colors, as determined by the CURSOR_DATA value. The rest of this section assumes that the Cursor is NOT active.

If the CMC Lookup function = BYPASS, then the Palette's 24-bit input pixel data is routed directly to the DACs. Pipeline stages are incorporated to match the delays of the Palette. A Color Channel refers to one of the Palette's 1Kx8 RAMs, or that same RAM's potential Bypassing pixel-value. With its 3 color channels, the Palette can be used to generate true or pseudocolor information. The CMC Color Depth function controls this attribute. In true color each channel is addressed independently, while in pseudocolor the selected pixel input is replicated to the 3 channels. If both Pseudocolor and Bypass are asserted, the resulting display will be Gray Scale, with identical inputs to each of the 3 DACs.

The CMC Palette Table function serves to divide down the Palettes large 1K color space. In general, a given Color Model state corresponds to the specific attributes of different “windows” exhibited on the system display screen. The usual pixel space for such windows is 256, which corresponds to the 8-bit width of X, R, G, or B pixel components. Associated with such a pixel range is a Color Palette “table” of 256 locations. For greater color flexibility, the Bt497A/8A provides 4 distinct Palette tables selected by CMC.

The last function in Table 11 is labeled “Palette Section” for the Separate_4 mode. From Figure 15, it is seen that these OCM[3:0] bits are input to the XO mux, as an upper nibble. Thus, when the Color Model is “Pseudo-color from XO”, and the WM is Separate_4, then the Palette Section bits will divide and select the chosen Palette Table among 16 16-entry sections.

Overlay/Underlay Operation

As indicated previously, the data in the incoming X field can be interpreted as either a WLUT index or as an overlay select. Thus, pixel overlays are accommodated without incurring the expense of additional planes in the frame buffer memory and additional LUTs in the Bt497A/8A. This is accomplished by using the 1K x 8 x 3 Palette to contain overlay colors and by circuitry that regulates the selection of overlay or underlay data for display.

This function appears in the color model control diagram as the Overlay/Underlay Logic block of Figure 15. The details are illustrated in Figure 16. As repeated elsewhere, an active Overlay causes the CMC output to be the OCM state. Otherwise the color model is "Underlay," and CMC drives the PCM state. These two states are detailed in Table 11. In this framework, there are two Overlay types, which are selected from specific OCM bits. The control of overlay types is summarized in Table 12. Assuming the Overlay Enable bit is asserted, then SELECT_OVERLAY will be asserted whenever the OPAQUE overlay input is active (The "SELECT_OVERLAY" signal in Figure 16 is equivalent to "DO_OVLY" in Figure 15.) The remainder of this section assumes Overlay Enable is asserted and TRANSPARENT overlay is active. (Transparent and Opaque selections can NOT be active simultaneously.) The principle of transparent overlay/underlay operation is illustrated in Table 12, and works as follows.

The contents of two registers, the Transparent Mask Control Register and the Transparent Color Key Register, define a transparent overlay color key value. This color key value is compared to the value contained in XA[7:0]. If the two values are equal, the overlay is said to be transparent and the underlay (Primary WLUT) color model is driven, i.e., the overlay mux passes PCM state to WLU[6:0]; therefore, the color model and the color source are chosen by the contents of the PWLUT. If the two values are not equal, the overlay color model is active: the overlay mux passes the OCM state to WLU[6:0].

Figure 16. Overlay/Underlay Logic

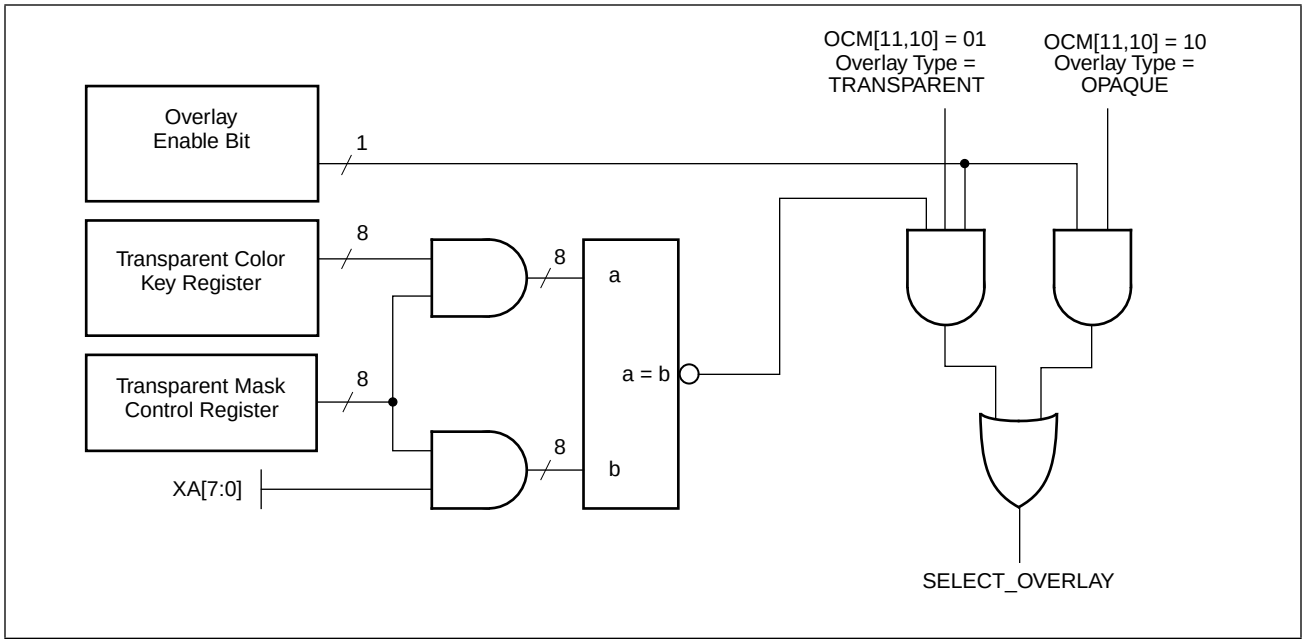


Table 12. Overlay Operation

Overlay Enable	OCM[11,10]	Overlay Type	Transparent Color	SELECT_OVERLAY
0	x	x	x	Under
1	10	Opaque	x	Over
1	00	None	x	Under
1	01	Transparent	Color key AND Mask = XA AND Mask	Under(1)
1	01	Transparent	Color key AND Mask ≠ XA AND Mask	Over

Notes: (1). For the special case where all of the Transparent Mask Control Register bits [7:0] are set to zero, the underlay will be used for color model control.

Overlay Enable Control Bit

The Overlay Enable Bit is contained within the User Control Register. When the overlay control is disabled, (set to a logical 0), the underlay data (PCM) is used for color model control (i.e., WLU[6:0]). When the overlay control is enabled, (set to a logical 1), the selection of overlays is controlled by the rest of the logic in Figure 16.

Transparent Overlay Mask Register

This 8-bit register operates on the contents of the Transparent Color Key Register and the XA data to define the extent (in the bit dimension) of the color key value. Transparent Mask Control Register bits set to logical 1 allow the corresponding bits of the Transparent Color Key Register and the XA field to participate in the transparent color comparison. Transparent Mask Control Register bits set to logical 0 preclude the corresponding bits of the Transparent Color Key Register and the XA field from comparison. Register initialization is not required.

Transparent Overlay Color Key Register

This 8-bit register defines the transparent color key value, subject to the contents of the Transparent Mask Control Register. Register initialization is not required.

Overlay Type Selection Bits

These two dynamic bits are input from the OWLUT location that is currently active. OCM[10], when asserted, indicates Transparent overlay type. OCM[11], when asserted, indicates Opaque overlay type.

Window Lookup Transfer Control

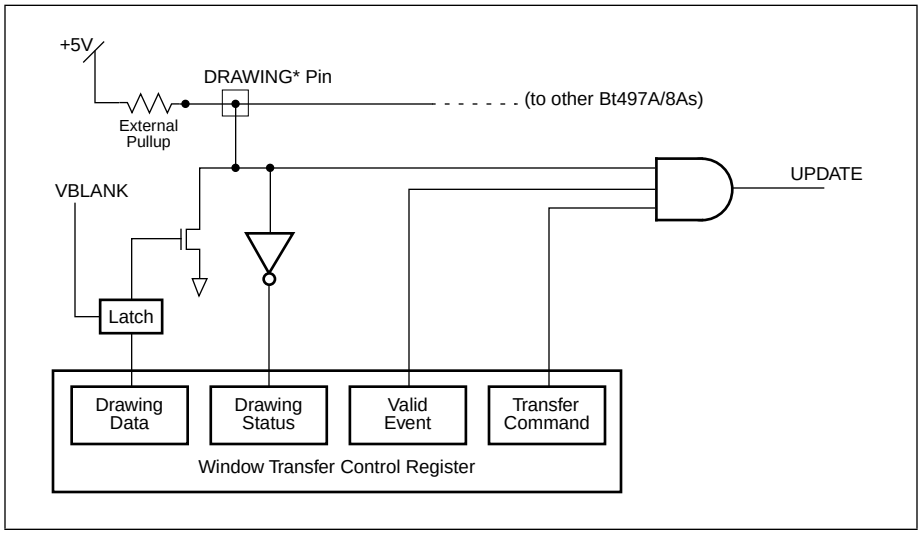
In the Color Model Control section, the 2 WLUT Shadow RAMS were introduced. These RAMs are loaded at any arbitrary time by the MPU with new window attribute information intended to become active for the system display. Note, the 2 Active WLUTs may be accessed by the MPU and should be initialized during the startup procedure. To avoid visual artifacts on the display screen, the active WLUTs should not be accessed during active video, but should instead get updated through the 2 respective Shadow WLUTs. This section describes the details of how and when the Active RAM contents get updated with the contents of the respective Shadow RAMs, a process referred to as "window transfer." The eventual updating, or transfer of RAM data from Shadow to Active WLUTs is handled by the Window Transfer Control (WTC) Register. The general operation of this register is given here, see the Internal Register section for specific bit assignments and descriptions.

The Bt497A/8A has several features which facilitate operation in a multiple RAMDAC configuration with other Bt497A/8As. One of those aspects is the synchronizing of window transfers by use of the DRAWING* pin, as shown in Figure 17. The intention is to provide a hold off of final window transfer for all Bt497A/8As, even though some local MPUs have requested it, until ALL the Bt497A/8As have signalled they are "ready" for the transfer. Accordingly, each Bt497A/8A has an open-drain DRAWING* pin which operates in a bidirectional fashion as follows.

Assume the user is ready for a major WLUT change, such as switching between Double Buffers. First the user programs the WTC Drawing Data bit to a 1, meaning that this local Bt497A/8A is pursuing window changes. In Figure 17, this activates the pulldown, which pulls the common DRAWING* line Low. The user then updates the local Shadow PLWUT (and OWLUT) as required. Finally the (local) user sets Drawing Data to 0, and sets the WTC Transfer Command to 1. The local Bt497A/8A is then in a "transfer pending" state. However, the transfer may not be fully enabled until all the chips on the network have also become pending. When that happens, no local node pulldown is active, and the external pullup brings the DRAWING* line high. The actual transfer will occur when Valid Event goes high, which is always at an appropriate VSYNC-active edge. ("Valid Event" symbolizes the more detailed effects of the Transfer Event bit and FIELD signal edges in WTC.) The "Latch" block in Figure 17 indicates that the DRAWING* pulldown will be prevented from changing its state if VBLANK happens to be active.

The target color model function for the above synchronizing mechanism is in fact Double Buffer changes. As Double Buffering is only supported in the Bt498A, the DRAWING* feature is only supported for that product. DRAWING* pin is not found in the Bt497A part. Users of Bt497A should set the Drawing Data bit to a constant 0, to allow normal window transfers. The same applies to users of single-chip Bt498A systems. In both cases, a weak internal pullup at the DRAWING* pad-buffer insures that the Drawing Status bit is low, and the DRAWING* pin (for Bt498A) may be left unconnected.

Figure 17. Multi-Chip Window Transfer Control



On-chip Cursor Operation

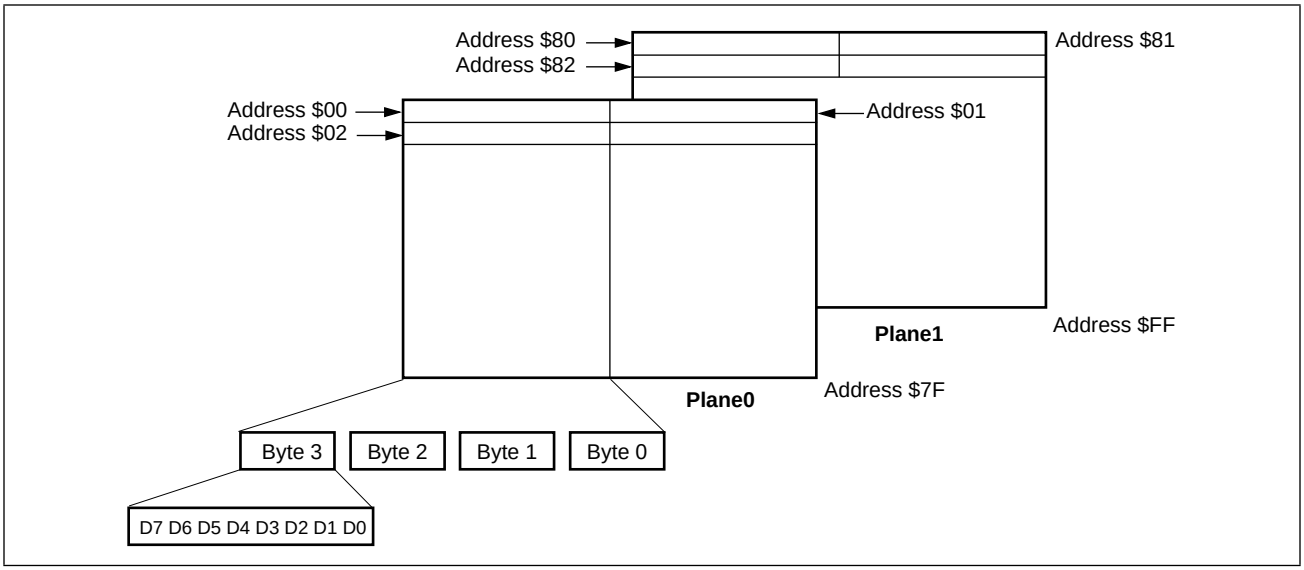
The Bt497A/8A has an on-chip, user-definable, three-color, 64 x 64 pixel cursor. The pattern for the cursor is provided by a two-plane 64 x 64 cursor RAM which can be accessed by the MPU at any time. Each plane provides 1 bit of cursor information every pixel clock cycle. These 2 bits are used to select a cursor color from a 3 x 24 LUT, as shown in Table 13. Each plane may also be independently enabled or disabled using the Cursor Control Register. Writing a 1 to the appropriate register bits immediately blocks the cursor from appearing, regardless of its position. This action is recommended before doing any updates to either the cursor RAM or the cursor color LUT, to avoid visual artifacts. Then re-enable the appropriate planes to view the completed changes. The assertion of RESET* enables both planes.

The cursor RAM is accessed through the MPU in a planar format. Each byte in the MPU write cycle constitutes 8 RAM bits in which the Most Significant Bit (MSB) becomes the leftmost location of each load group. The most significant byte corresponds to the leftmost position of each address. The Plane0 addresses are $00 to $7F and Plane1 addresses are $80 to $FF within the cursor configuration address space. See Figure 18 for an exact mapping between the MPU addresses and the corresponding bit map as it is observed on the screen.

Table 13. Cursor Color LUT

Plane1	Plane0	Color Displayed	Cursor Address
0	0	Transparent	
0	1	Cursor Color 1	$0101
1	0	Cursor Color 2	$0102
1	1	Cursor Color 3	$0103

Figure 18. Cursor RAM Address Map



Cursor Color LUT

Cursor color LUT follows the same load sequence through the MPU as the color palette LUT (red, green, blue, and a dummy value) and can be accessed at any time.

Cursor Positioning

The cursor position is determined by values in the Cursor Position Register. This 32-bit field contains the sign and magnitude of the X and Y start position of the 64 X 64 cursor's top left corner, as shown in Figure 19.

The Bt497A/8A contains an internal X counter that increments by pixel going right, from –64 to +4031, and a Y counter that increments by line, going down on the screen from –64 to +4031. When the values of the X and Y counter match the values in the Cursor Position Register the contents of the cursor RAM will be displayed on the screen. In noninterlaced mode, the latest position is loaded in from the register and the display counters are reset to zero (the top left corner of the screen) at the beginning of each vertical sync. In interlaced mode, the position update will not take effect until the next VSYNC* before an even field. Cursor position (0,0) constitutes the top left corner of the active video display. This enables the users to position the cursor off of the top (Y = –64) and the left side of the screen (X = –64). See Figure 20.

The assertion of RESET* resets the cursor RAM X and Y display counters, but does not reset the position register.

Note that all other cursor registers will exhibit immediate effects when they are written with new values by the MPU. When the Cursor Position Register is written, its new value may be read back immediately. However, the cursor will not move on the screen until the appropriate VSYNC* occurrence.

Figure 19. Cursor Position Register

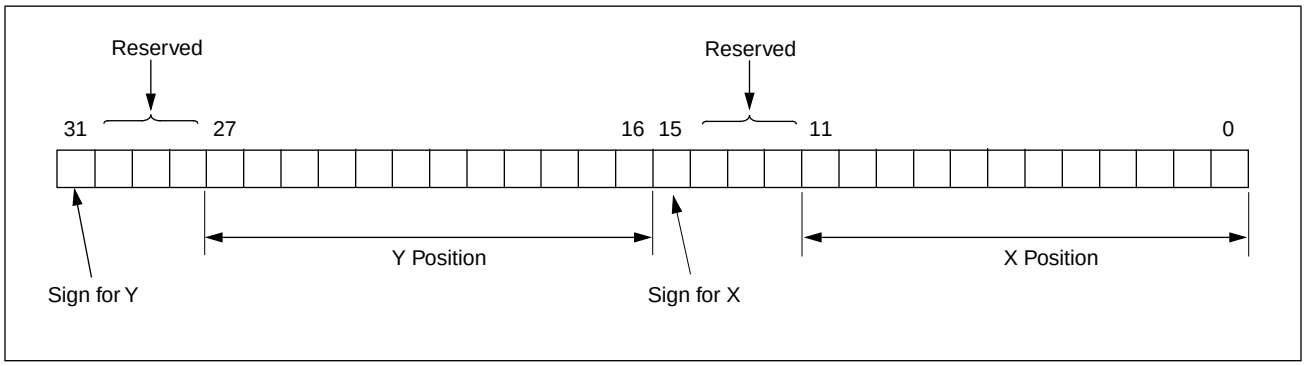
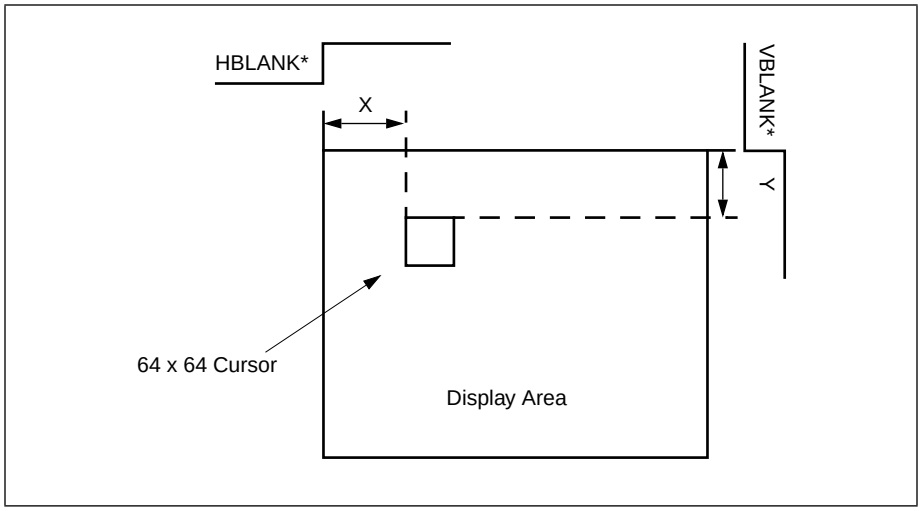


Figure 20. Cursor Positioning



Cursor Interlace Operation

When the Bt497A/8A is operated in the interlaced mode, the cursor is displayed in an odd and even field format. If the Y value in the Cursor Position Register is an even number, then the first row (Row 0) and all of the even rows of the cursor RAM will be displayed during the even field. The odd rows, starting with Row 1, will be displayed in the odd field. If the Y position value is an odd value, then the display sequence is reversed; even rows during odd fields and odd rows during even fields.

Timing Generator

The Bt497A/8A has an on-chip timing generator, operating from the serial clock, that provides video display and memory timing reference signals for interlaced and noninterlaced video formats. The timing boundaries are set by the values in the Timing Generator Control Register and in the various timing point registers. To avoid lockup or timing glitches it is required that the pixel clock be freely running whenever changes are made to any of the Timing Generator Registers.

System Reset

When asserted, the system reset signal (RESET*) has the following effects.

A registered function named Video Enable is forced to the video disabled state by the assertion of RESET*. This condition persists after the negation of RESET* and until it is overwritten via the MPU port. Video Enable, when in the disabled state, asserts composite blanking within the RAMDAC so that the video monitor remains black while the timing generator is being programmed.

When asserted, RESET* forces the Timing Generator Horizontal and Vertical Counters to a zero value. Timing Generator Enable is forced to the disabled state by the assertion of RESET*. This condition persists after the negation of RESET* and until it is overwritten via the MPU port. The purpose is to hold the timing generator in a known state while it is being programmed. No other Timing Generator functions or waveforms are affected when Video Enable is in the disabled state.

When asserted, RESET* causes the timing generator to be in the slave mode. In this case, the FIELD signal is placed in the high-impedance mode.

Timing Generator Test Features

To enable the user to observe timing generator operation, several internal timing signals can be output onto the MPU bus by accessing the Timing Generator Test Register ($6011). This is accomplished by loading the register value in the address pointer and setting the MPU port into the read mode. When the CE* is enabled (low) the signals listed in Table 14 will be output onto the MPU port. When the CE* is disabled (high) the MPU port will return to normal operation. Three additional CE* cycles are still required to increment to the next address.

Table 14. Internal Timing Generator Signals

MPU Output	Internal Signal	Description
D[7]	HSYNC*	Internal Horizontal Sync
D[6]	SERRATION*	Internal Serration Pulses
D[5]	EQUALIZE	Internal Equalizing Pulses
D[4]	CBLANK	Internal Composite Blank
D[3]	CSYNC*	Internal Composite Sync
D[2]	VSYNC*	Internal Vertical Sync
D[1]	VBLANK*	Internal Vertical Blank
D[0]	HBLANK*	Internal Horizontal Blank

Timing Generator Display Formats

The timing generator is controlled by programming the appropriate values into the Timing Generator Control Register. Both interlaced and noninterlaced modes of operation are supported. All horizontal register values are in units of the serial clock rate. All vertical register values are in units of horizontal lines.

The origin of the timing coordinates is the serial clock period immediately following the start of vertical sync. This means that line 0 is the first line of vertical sync, and horizontal unit 0 is the first serial clock period immediately following the start of horizontal sync. The values to load into the registers are one less than the desired timing point. Neither the horizontal nor the vertical registers can be programmed to have a value of zero. When operated in pixel formats of 4/2:1 and 8/2:1, the horizontal active interval, represented by the Horizontal Blank Negation Point and Horizontal Blank Assertion Point registers, should be programmed with an even value. The programming of these registers is described in the Internal Registers section.

The video display timing information is sent to the monitor by inserting the blank and sync information onto the DAC outputs, via the Timing Generator Control Register. The sync information is also available on two digital pins: CSYNC* and VSYNC*. In noninterlaced mode the CSYNC* contains horizontal and vertical, optionally serrated sync information. In interlaced mode the horizontal Equalization information is also included. VSYNC* always expresses the Vertical Sync transitions, with Vsync active driven to a low level. For separate sync monitors, CSYNC* may be reduced to HSYNC* by setting appropriate bit(s) in the Timing Generator Control Register.

Output Signals

Bt497A/498A provides the following timing generator outputs: SC*, SCEN*, STSCAN, FIELD, VSYNC*, and CSYNC*. Assuming the Timing Generator is enabled, all these signals will preserve their programmed waveforms even if the screen is set to “constant blank” by other Bt497A/498A registers.

FIELD Output

The FIELD signal, when in master mode, transitions with the leading edge of the internal VSYNC*. Additionally, the level is used to output the current field when in interlaced mode (logical 0 = even field, logical 1 = odd field). In noninterlaced mode, transitional edges of this signal will still occur near the leading edge of every VSYNC*; however, the level of the FIELD signal has no meaning. Externally, the signal may be used to differentiate between left and right views of a stereo display.

STSCAN Output

The STSCAN output is an internally generated signal that can be used by the memory controller to determine the proper row transfer address timing for the VRAM frame buffer serial port. The logic will set the STSCAN signal at the rising edge of SCEN* if the next line is visible and reset the STSCAN at the falling edge of SCEN*.

SCEN* Output

The SCEN* output is used for enabling the clocking of the serial data from the VRAMs. The assertion of SCEN* is controlled by programming the timing generator registers Vertical Blank Negation Point (VBNP), Vertical Blank Assertion Point (VBAP), Horizontal Serial Clock Enable Assertion Point (HSCENAP), and Horizontal Serial Clock Enable Negation Point (HSCENNP).

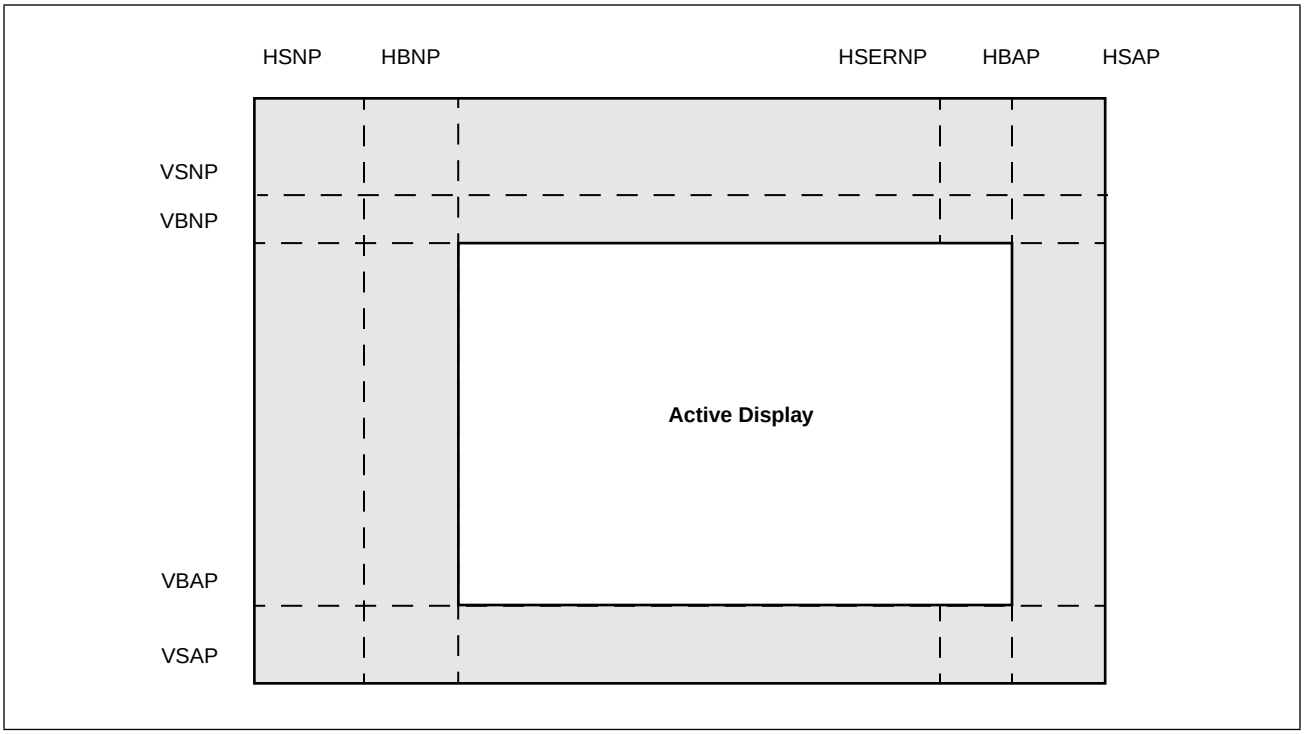
VSYNC* and CSYNC* Outputs

These two outputs are distinguished from the others in that A) they are pipeline delayed to be consistent with the Analog DAC outputs; and B) they are synchronized by the pixel clock. (The above outputs belong to the serial clock domain.) The waveforms of VSYNC* and CSYNC* were described in the previous section. Both VSYNC* and CSYNC* may be disabled (forced to high level) by setting bits in the Timing Generator Control Register. The active state may be programmed via sync polarity bit in DAC control register.

Noninterlaced Timing

The noninterlaced timing points are illustrated in Figure 21. Timing diagrams are shown in Figures 22 and 23. Register values represent the SC* period or line before the event occurrence and should be programed to a value one less than the desired time point. An example of a 1280 x 1024 display is given in the Applications Information section. The timing points are defined in two groupings: horizontal and vertical.

Figure 21. Noninterlaced Format Timing Boundaries



Horizontal Timing Generation

For generating the horizontal and serrated sync signals, the Horizontal Sync Assertion Point (HSAP), Horizontal Sync Negation Point (HSNP), and Horizontal Serration Negation Point (HSERNP) registers are programmed with the desired durations in SC* clock units. All the parameters should be programmed as one less than the desired duration.

The operation is described as follows: The Timing Generator Horizontal Counter begins at a value of zero, with the HSYNC* and SERRATION* waveforms active (i.e., low). When the counter reaches the HSNP value, HSYNC* is deasserted on the next serial clock. The Timing Generator Horizontal Counter continues counting up until the programmed HSERNP value is reached, at which point the SERRATION* waveform is deasserted on the next serial clock. The Timing Generator Horizontal Counter continues until the HSAP value is reached, after which the Timing Generator Horizontal Counter will be restarted at zero on the next serial clock. Timing diagrams for the generation of composite sync are shown in Figure 22. A diagram illustrating the relative register values related to active screen area is shown in Figure 23. The generation of the horizontal blanking signal is relatively straightforward; HBLANK* is asserted on the next serial clock after the Timing Generator Horizontal Counter reaches the value programmed in the Horizontal Blank Assertion Point Register (HBAP). HBLANK* is then deasserted on the next serial clock after the Timing Generator Horizontal Counter reaches the value programmed in the Horizontal Blank Negation Point Register (HBNP).

The horizontal timing register values should satisfy the following relationships:

$$0 < HSNP < HSERNP < HSAP$$

$$0 < HSNP < HBNP < HBAP < HSAP$$

HSNP	Endpoint Hsync and start of Horizontal Back Porch.
HBNP	Endpoint HBLANK* and start of active video.
HBAP	Endpoint active video and start of HBLANK*.
HSAP	Endpoint Horizontal Front Porch and start of Hsync. HSAP +1 represents the total number of serial clock periods in a line.
HSCENNP	The last serial clock period that SCEN* will be active.
HSCENAP	SCEN* is active on the next serial clock period. HSCENAP should be less than HBNP by exactly the number of serial clocks that it takes for pixel data to be clocked in at Bt497A/8A input. HBNP-HSCENAP should always equal HBAP-HSCENNP.
HSERNP	The last serial clock period of horizontal sync during the vertical sync interval.

Figure 22. Horizontal Timing and Composite Sync Generation–Noninterlaced Format

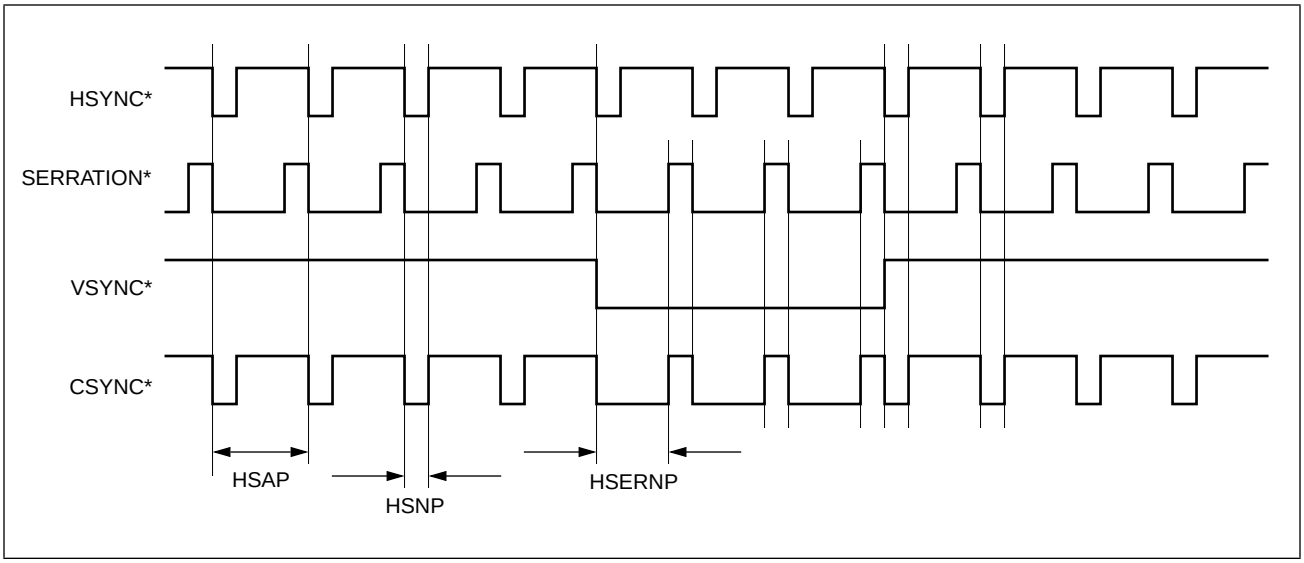
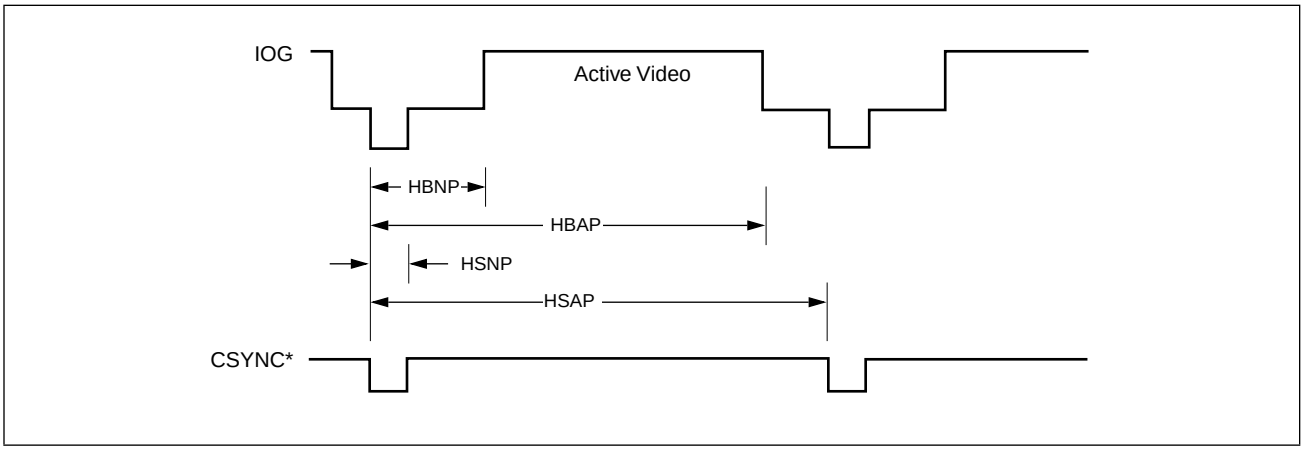


Figure 23. Noninterlaced Horizontal Timing



Vertical Timing Generation

The VSYNC* vertical timing signal is generated using the values contained in the Vertical Sync Negation Point (VSNP) and Vertical Sync Assertion Point (VSAP) registers. The VBLANK* vertical timing signal is generated using the values contained in the Vertical Blank Assertion Point (VBAP) and Vertical Blank Negation Point (VBNP) registers. In noninterlaced mode, all vertical timing register intervals are specified in units of horizontal lines (i.e., the load period x HSAP). The vertical timing counter is incremented at each horizontal sync assertion time; subsequently, the only time that any vertical timing signals may transition is at HSYNC* assertion.

The vertical timing registers should be programmed to satisfy the following relationship:

$$0 < VSNP < VBNP < VBAP < VSAP$$

The composite blank signal is derived by logically *OR*'ing internal HBLANK* with VBLANK*.

VSNP — Endpoint Vsync and start of Vertical Back Porch. VSNP +1 represents the number of lines during the vertical sync period.

VBNP — Endpoint of VBLANK* and start of active video. The register values represent the number of blanked lines above the active video display plus the lines of Vertical Sync –1.

VBAP — Video is blanked starting on the next line.

VSAP — Endpoint VBLANK* and start of Vsync. VSAP +1 represents the total number of lines in the frame. The Timing Generator Vertical Counter is reset to zero after Vertical Sync is asserted.

Composite Sync

The composite sync signal combines the Hsync with the serration pulses during the vertical sync interval onto a discrete output. The components of the CSYNC* output can be enabled or disabled using the Timing Generator Control Register, as shown in Table 15.

Note that the characteristics of CSYNC* as defined by Table 15 are also exhibited in the analog IOG output SYNC component timing.

Table 15. CSYNC* Output: HSYNC* and VSYNC* Control

Timing Control Register		CSYNC* Output
HSYNC* (Bit 2)	**VSYNC* (Bit 3)**	
Enabled	Enabled	Normal operation
Enabled	Disabled	CSYNC* looks like HSYNC* (no serrations)
Disabled	Enabled	CSYNC* looks like VSYNC* (no serrations)
Disabled	Disabled	CSYNC* inactive (high level)
Note: Non interlaced mode only.		

Interlaced Timing

Due to the nature of the composite sync and video signals during the Equalization and vertical sync intervals, interlace mode timing events are based on half-line intervals. Equalization refers to the process whereby special pulses, different from HSYNC timings, appear on CSYNC* during a significant portion of the vertical blank interval. Equalizing refers to these special pulses, or their duration. During the equalization interval, CSYNC* expresses equalizing pulses every half-line. Outside of equalization however, CSYNC* expresses HSYNC pulses every other half-line. To generate half-lines, the timing generator clocks the horizontal and vertical counters twice per scan line. The first starts the external horizontal sync interval. The second occurs at the half-way point of the scan line and is used mainly to trigger the consecutive serration or equalizing pulses during the vertical sync.

The Timing Registers are described in this section and in the Internal Register section. The register values represent the SC* period or half-line before the event occurrence and should be programmed to a value one less than desired time point. Note that since the counters are clocked twice per scan line, the values in the registers are half of the value programmed for the noninterlaced mode. Examples of the timing values for NTSC and PAL are included in the Application Information section. The timing points are defined into two groupings, Horizontal and Vertical.

Horizontal Timing Generation

The relationships between the programmed register values and the waveforms are shown in Figures 24 and 25. One additional horizontal time point is required in interlaced mode.

EQNP — Equalizing Negation Point (EQNP) is the value programmed in the control register that represents the equalizing pulse width (minus one SC*) and is normally programmed to half of the HSYNC* width. The equalizing pulses may only occur during the pre- and post-Equalization intervals shown in Figure 26.

The start of the horizontal timing is determined by the field to be displayed. If the field is even, it starts on an even half-line; if it is odd, it starts on an odd half-line as shown in Figure 26. The state of the field is reflected on the FIELD pin, which changes at the onset of Vertical Sync. During an Even Field, FIELD is low; during an odd field, FIELD is high.

The SCEN* and STSCAN signals extend over half-line boundaries and follow the same behavior as the noninterlaced mode.

Figure 24. Horizontal Timing Waveforms–Interlaced Format

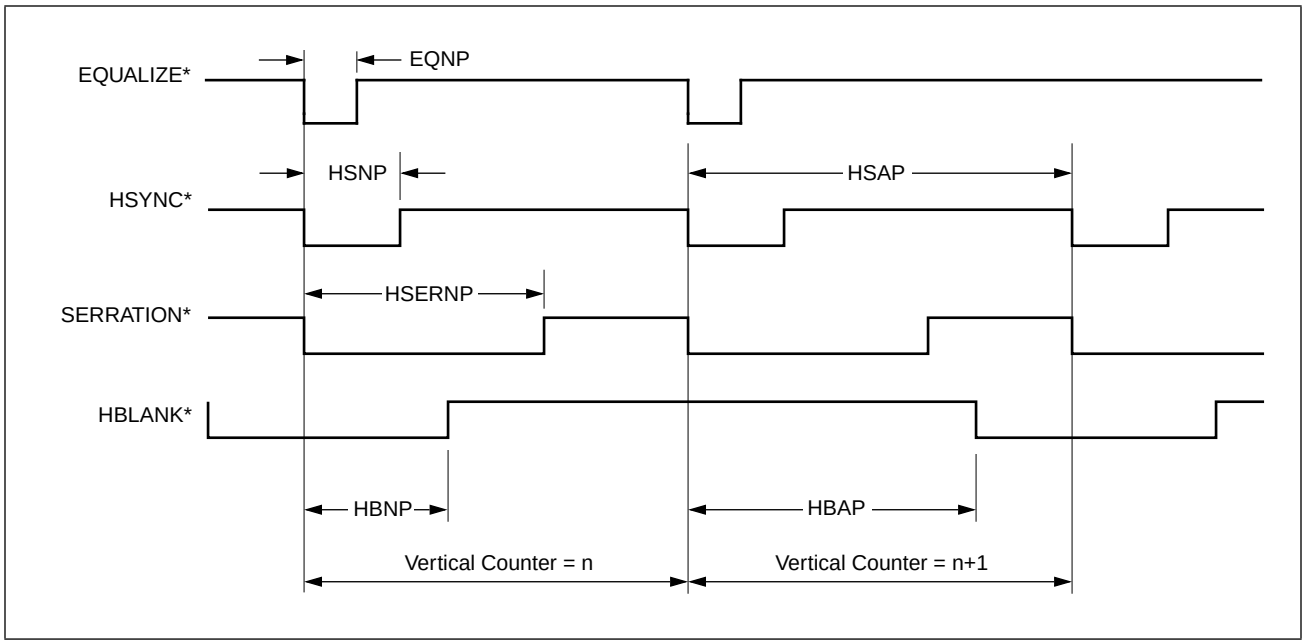


Figure 25. Interlaced Horizontal Timing for CSYNC* Signal

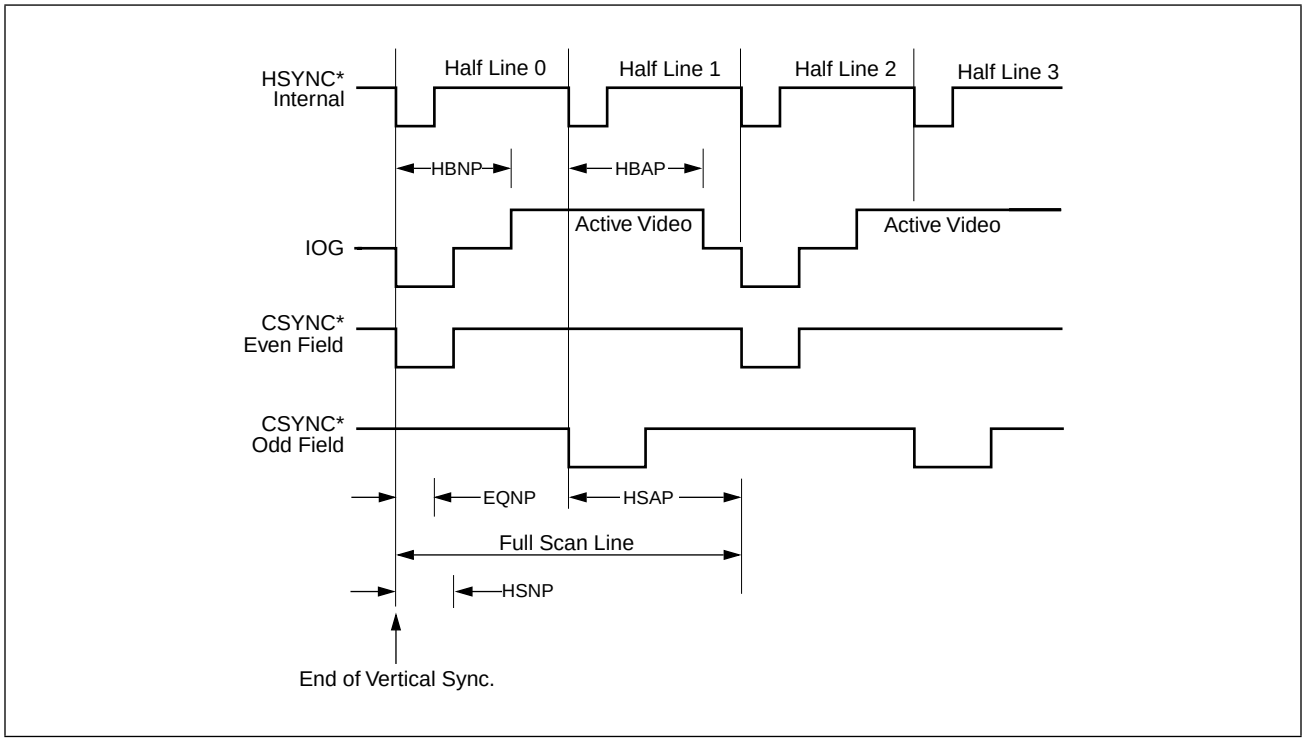
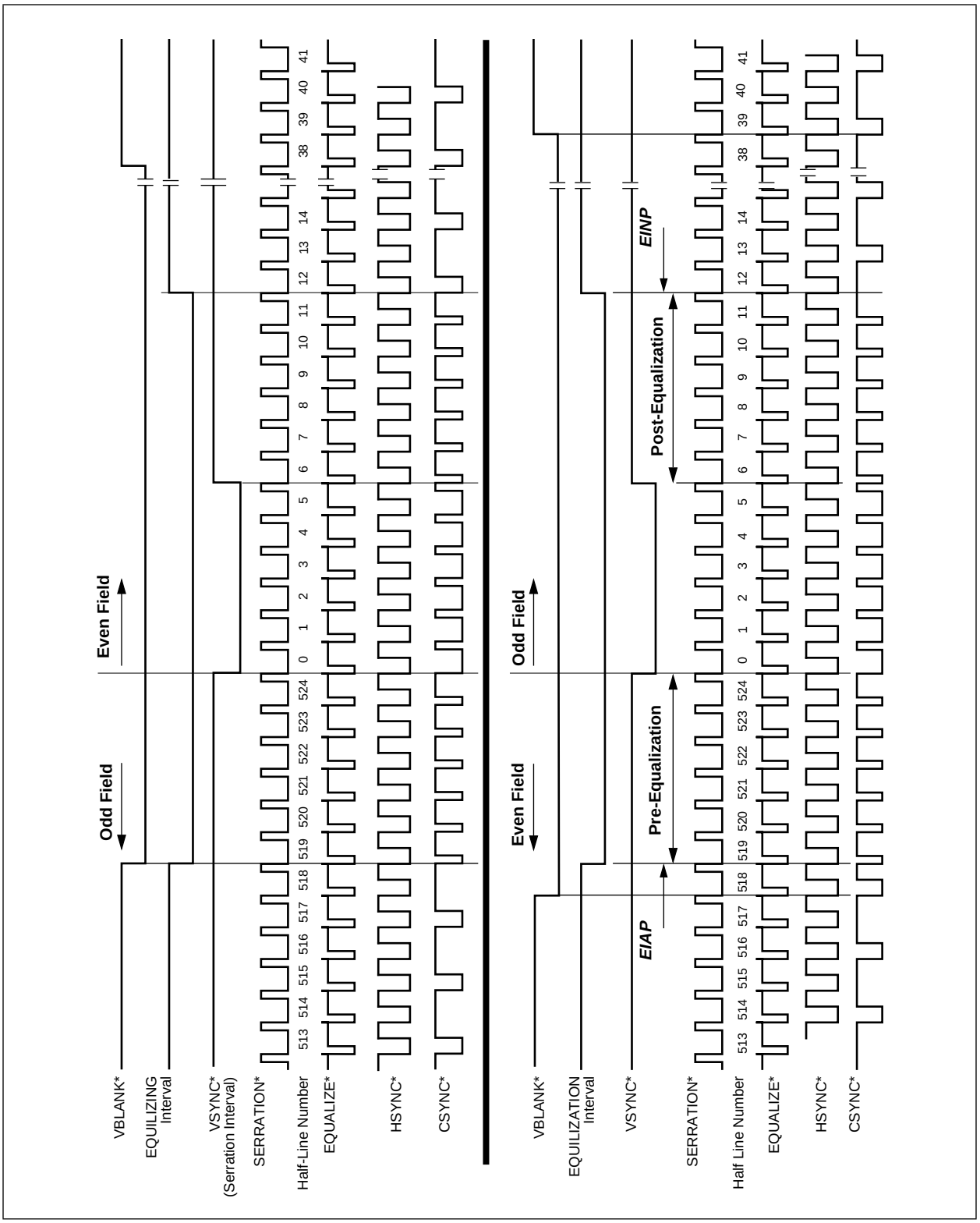


Figure 26. NTSC Interlaced Timing



Vertical Timing Generation

Interlaced display on the Bt497A/498A adopts the convention of displaying the first line of active video, corresponding to the first line of the frame buffer on an even field; the second line of the frame buffer is displayed as the first line at the odd field. This allows the Bt497+/8+ to properly order the cursor scan line. To keep this convention, the VBNP must be programmed with an odd value to ensure that the beginning of the horizontal events happened on an even cycle. VBAP can be programmed as an even or odd value depending on the number of lines in the frame buffer. The value in the VSAP register represents the total number of half-lines –1, while the value in the VSNP reflects the number of half-lines of serration during vertical sync.

Two additional timing parameters, shown in Figure 26, are required for interlaced operation.

EINP — Equalization Interval Negation Point (EINP) indicates the last half-line following vertical sync on which to generate an equaliz~~ing~~ pulse. The value in this register and the VSNP register determine the number of Equalizing pulses in the post-equalization interval.

EIAP — Equalization Interval Assertion Point (EIAP) corresponds to the first equalizing pulse before vertical sync. The value in this register and the VSAP register determine the number of equaliz~~ing~~ pulses in the pre-equalization interval.

The vertical timing registers should satisfy the following relationship:

$$0 < VSNP < EINP < VBNP < VBAP \leq EIAP \leq VSAP$$

Composite Sync Generation

The composite sync signal combines the HSYNC* with the serration and equalizing pulses on a discrete output. The start of the HSYNC* component depends on the field to be displayed. If it is an even field it starts on the first even half-line after the VSYNC* interval; if it is an odd field it will start on the first odd half-line. For composite monitors running interlace, the two Sync Disable bits in the Timing Control Register should match each other. If they are enabled, CSYNC* will operate normally; if they are disabled, CSYNC* will output a high level.

Slave Mode Operation

When the Timing Generator Control Register is programmed to slave mode, the timing generator accepts the FIELD signal as an input. In this mode, a transition occurring on this input will cause the Timing Generator Vertical Counter to be reset and VSYNC to be asserted, regardless of the VSAP value, at the subsequent horizontal sync occurrence. If the Bt497A/498A is in interlaced mode, the level that the FIELD input transitions to will determine which field is current (i.e., a high-to-low transition causes the timing generator to start at the top of an even field on the next HSYNC* leading edge). Since the Timing Generator Horizontal Counters are not reset, the clock drift will eventually cause the blanked front porch for the slave to be one line longer, or shorter. Master field transition must occur after VBAP and EIAP. Vertical front porch may need to be extended to accommodate this.

Monitor Identification and Control Interface

The Bt497A/8A incorporates two separate 2-bit registers for use as the hardware portion of a software driven, synchronous, half-duplex, serial interface. This interface provides the means for reading video monitor identification codes and for controlling certain monitor functions from the host system. The host system communicates with the interface registers via the MPU port. It is important to note that no interface control circuitry is required. The serial monitor features will not be active during active video. These features could be accessed during blanking.

The Monitor Port Data Register, shown in Figure 27, contains the levels intended for driving out on the individual open-drain monitor pins, SDA and SCL. A ‘0’ in either bit will cause the respective pin’s buffer to drive an active low. A ‘1’ causes the pin to be 3-stated. In this condition, the read-only Monitor Port Sense Register (Figure 28) may be accessed by the MPU to determine the actual level driven by the monitor on either SDA or SCL.

Figure 27. Monitor Port Data Register

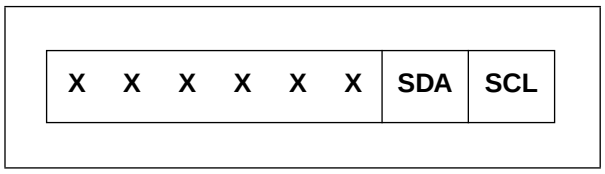
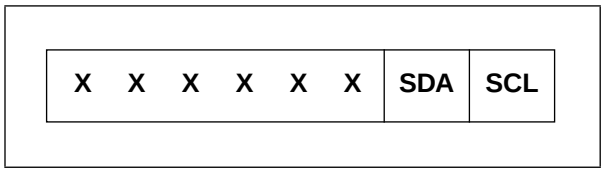


Figure 28. Monitor Port Sense Register



Video Generation

Every clock cycle, the selected color information from the color model or cursor is presented to the D/A converters. Sync and blank information adds appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 29 and Figure 30.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) may contain sync information. Table 16 and Table 17 detail how the sync and blank information from the timing generator modifies the output levels.

The D/A converters on the Bt497A/8A7A use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full-scale output current against temperature and power supply variations.

Figure 29. Composite Video Output Waveform (7.5 IRE Setup)

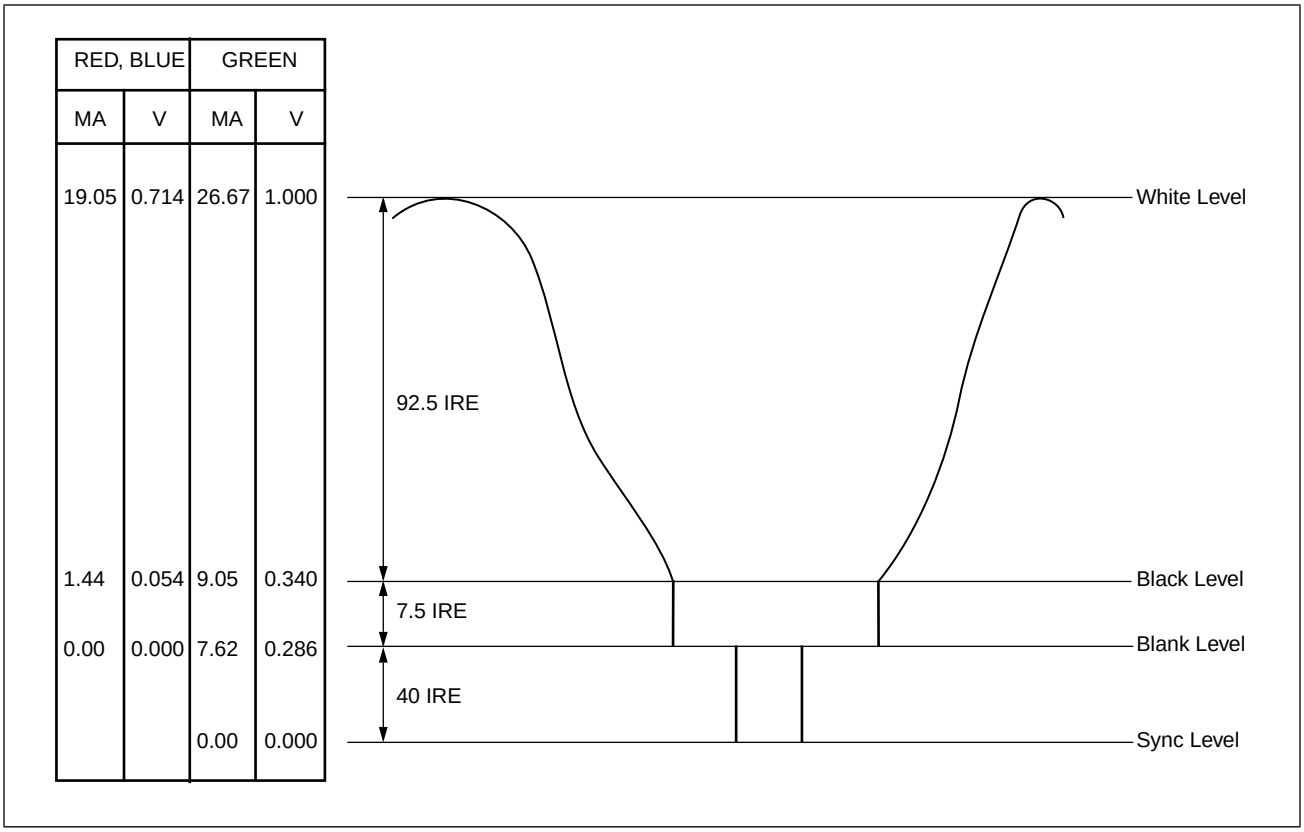


Table 16. Video Output Truth Table (7.5 IRE Setup)

Analog Level	IOG (mA)	IOR (mA) IOB (mA)	VSYNC* HSYNC*	VBLANK* HBLANK*	DAC Input Data
White	26.67	19.05	Disabled	Disabled	$FF
Data	Data + 9.05	Data + 1.44	Disabled	Disabled	Data
Data–Sync	Data + 1.44	Data + 1.44	Enabled	Disabled	Data
Black	9.05	1.44	Disabled	Disabled	$00
Black–Sync	1.44	1.44	Enabled	Disabled	$00
Blank	7.62	0	Disabled	Enabled	$xx
Sync	0	0	Enabled	Enabled	$xx

Figure 30. Composite Video Output Waveform (0 IRE Setup)

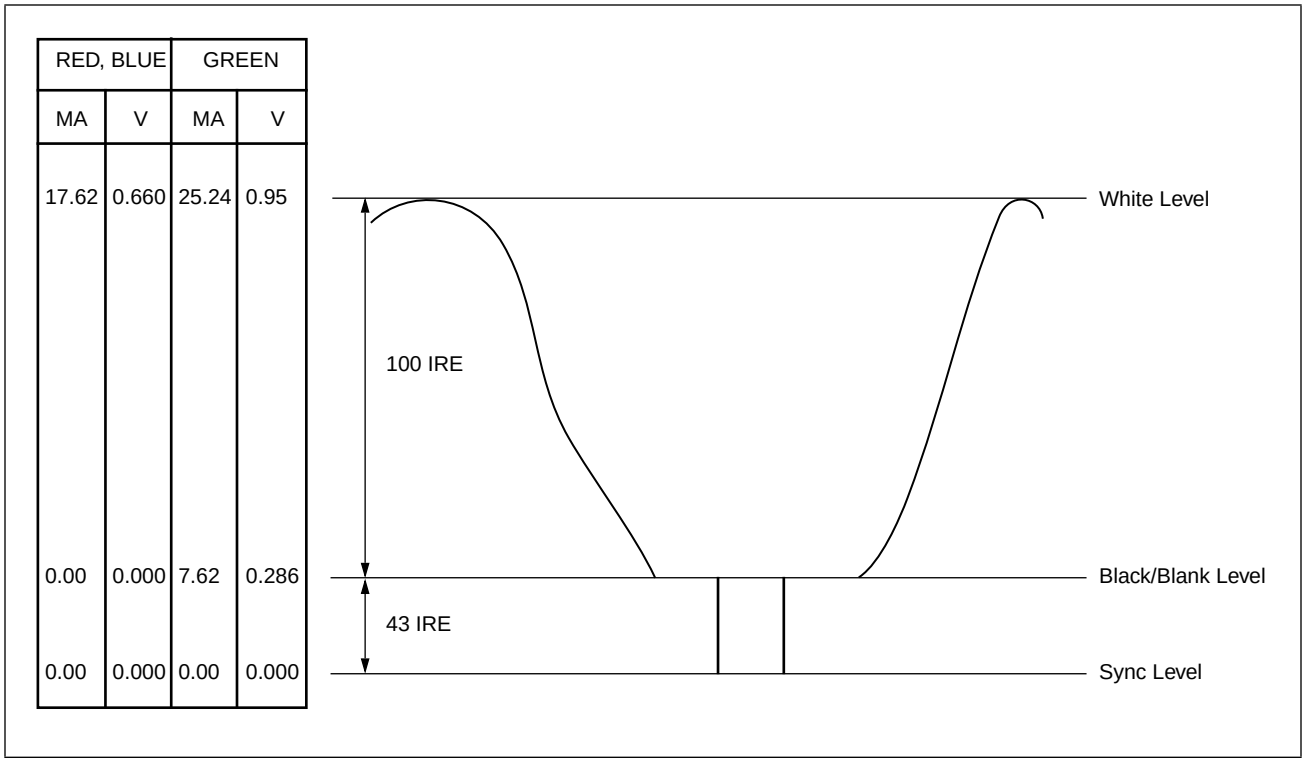
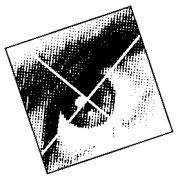


Table 17. Video Output Truth Table (0 IRE Setup)

Analog Level	IOG (mA)	IOR (mA) IOB (mA)	VSYNC* HSYNC*	VBLANK* HBLANK*	DAC Input Data
White	25.24	17.62	Disabled	Disabled	$FF
Data	Data + 7.62	Data	Disabled	Disabled	Data
Data–Sync	Data	Data	Enabled	Disabled	Data
Black	7.62	0	Disabled	Disabled	$00
Black–Sync	0	0	Enabled	Disabled	$00
Blank	7.62	0	Disabled	Enabled	$xx
Sync	0	0	Enabled	Enabled	$xx



INTERNAL REGISTERS

This section details the Bt497+/8+ internal registers. The user should not access reserved address locations. Furthermore, the user needs to be aware of reserved bits when accessing internal registers via the MPU interface. Reserved bits do nothing if they are written to, and most give a zero value when their register is read out. However, to ensure compatibility with future Bt497+/8+ code-compatible products, it is recommended that the reserved bits are maintained with read-modify-write access, which only updates unreserved bits. Also, in some registers, unreserved bits may not be resettable, but reserved bits have a reset value of zero.

NOTE: R/O = Read Only, N/R = Not Resettable, R/W = Readable and Writable.

Pixel PLL Control Register (C[1,0] = 01, Address = $0000)

Bit(s)	Field	Read /Write	Reset Value	Description
31–15	Reserved	R/O		Reserved. Returns zeros when read.
14	PLL Enable (0) Disable PLL (1) Enable PLL	R/W	0	PLL enable control. A logical 1 enables the pixel PLL as the pixel clock source, using the crystal connected to the XTAL1 and XTAL2 inputs as the reference. A logical 0 disables the PLL. CLOCK and CLOCK* would then be directly used for the internal pixel clock.
13	Reserved	R/O		Reserved. Returns zeros when read.
12,11	L (00) Divide by 1 (01) Divide by 2 (10) Divide by 4 (11) Divide by 8	R/W	00	Post VCO frequency divider.
10–7	N ($0) Reserved : ($3) Reserved ($4) Divide by 4 ($5) Divide by 5 : ($A) Divide by 10 ($B) Divide by 11 ($C) Divide by 12 ($D) Reserved : ($F) Reserved	R/W	$4	PLL VCO divisor.
6–0	M ($00) Reserved : ($1F) Reserved ($20) Multiply by 32 ($21) Multiply by 33 : ($4F) Multiply by 79 ($50) Multiply by 80 ($51) Reserved : ($7F) Reserved	R/W	$27	PLL VCO multiplicand.

General Purpose PLL Control Register (C[1,0] = 01, Address = $0001)

Bit(s)	Field	Read / Write	Reset Value	Description
31–15	Reserved	R/O		Reserved. Returns zeros when read.
14	PLL Enable	R/W	0	PLL enable control. A logic 1 enables the GP PLL as the General Purpose Clock source, using the XTAL1 and XTAL2 pins as reference. A logical 0 disables the PLL. CLOCK and CLOCK* would then be directly used as the GPCLK reference.
13	Reserved	R/O		Reserved. Returns zeros when read.
12,11	L (00) Divide by 1 (01) Divide by 2 (10) Divide by 4 (11) Divide by 8	R/W	1	Post VCO frequency divider.
10–7	N ($0) Reserved : ($3) Reserved ($4) Divide by 4 ($5) Divide by 5 : ($E) Divide by 14 ($F) Divide by 15	R/W	4	PLL VCO divisor.
6	Reserved	R/O		Reserved. Returns zeros when read.
5–0	M ($0) Reserved : ($14) Reserved ($15) Multiply by 21 ($16) Multiply by 22 : ($3E) Multiply by 62 ($3F) Multiply by 63	R/W	$1C	PLL VCO multiplicand.

Pixel Format Control Register (C[1,0] = 01, Address = $1000)

Bit(s)	Field	Read / Write	Reset Value	Description
31–2	Reserved	R/O		Reserved. Returns zeros when read.
1,0	Pixel Format Control (00) 2:1 (01) 4:1 (10) 4/2:1 (11) 8/2:1	R/W	N/R	Selects the pixel interleaving format. The LD frequency in each multiplex rate would be as follows: FLD = Fp/2 MHz FLD = Fp/4 MHz FLD = Fp/2 MHz FLD = Fp/4 MHz

User Control Register (C[1,0] = 01, Address = $1001)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–8	Reserved	R/O	N/A	This four bit field contains the current manufacturing revision for this device.
7,6	Reserved	R/O	0	Returns zeros when read.
5,4	Window Mode (00) Combined (01) Separate_4 (10) Separate_8 (11) Reserved	R/W	0	The Window Mode selection determines the specific source components to the 2 Window Lookup Tables, and the XO bus in the Color Model Control section.
3	Overlay Enable (0) Disabled (1) Enabled	R/W	0	When this bit is 0, the color model control always expresses underlays. When this bit is 1, the color model control is determined by the Overlay/Underlay logic.
2	Double-Buffer Enable (0) Single Buffered (1) Double Buffered	R/W	0	This field is valid only when in the 4/2:1 or 2:1 pixel format. Other formats require that this bit be set to zero.
1	Asynchronous Blank (0) Normal Operation (1) BLANK is constant	R/W	0	Allows user to force a blank to the screen.
0	Input Pullup Disable (0) Enabled (1) Disabled	R/W	0	Disables input pullup resistors on pins where present. Should be enabled during normal operation.

Shadow-Overlay Window Lookup Table (C[1,0] = 01, Address: $3100–$3103) and Active-Overlay Window Lookup Table (C[1,0] = 01, Address: $3120–$3123)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–14	Reserved	R/O		Reserved. Returns zeros when read.
13, 12	Pseudo-Color Source (00) XO[7:0] (01) R[7:0] (10) G[7:0] (11) B[7:0]	R/W	N/R	If overlays are active, these bits determine which pixel component gets replicated.
11,10	Overlay Type (00) No Overlay (01) Transparent Overlay (10) Opaque Overlay (11) Reserved	R/W	N/R	If Overlays are enabled, these bits determine if and when the Overlay state becomes active.
9	Reserved	R/O		Reserved. Returns zeros when read.
8	Color Lookup (0) Bypass the Palette (1) Index through Palette	R/W	N/R	If Overlays are active, this bit controls whether the Overlay pixel state addresses the Palette or bypasses it.
7,6	Reserved	R/O		Reserved. Returns zeros when read.
5,4	Palette Table (00) Table 0 (01) Table 1 (10) Table 2 (11) Table 3	R/W	N/R	If Overlays are active, these bits select which of the 4 Palette tables are active for color lookup.
3–0	Palette Section, Separate_4 ($0) Section 0 ($1) Section 1 ($2) Section 2 : ($F) Section 15	R/W	N/R	These bits form the upper nibble of the XO field, if the Window Mode is “Separate_4.” If XO addresses the Palette, then this Section value corresponds to a contiguous 16-location section within the Palette.

Window Transfer Control Register (C[1,0] = 01, Address = $3150)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–5	Reserved	R/O		Reserved. Returns zeros when read.
4	Drawing Status (1) Network Drawing Active (0) Network Drawing Idle	R/O	N/R	This bit gives the overall status of a networked system of multiple Bt497A/8A nodes. WLUT transfers may not occur until this bit is 0.
3	Drawing Data (1) Local Drawing Active (Pulldown) (0) Local Drawing Idle (3-state)	R/W	0	This bit controls the level and drive of the Bt497A/8A's DRAWING* pin. Changes to this bit are latched and delayed such that the DRAWING* pin will not change its state anytime VBLANK is active. Systems using Bt497A, and single-Bt498A systems should leave this bit at 0.
2	Transfer Event (1) Next Frame (0) Next Field	R/W	0	This bit controls the actual occurrence of the transfer, if the Transfer Command bit is set. If this bit is set to 0, then the transfer will occur on any transition of the field signal ($0 \geq 1$ or $1 \geq 0$). If this bit is set to 1, the transfer occurs on the falling edge of field signal ($1 \geq 0$).
1	Transfer Command (1) Transfer (0) No Action	R/W	0	Directs RAMDAC hardware to execute the transfer operation immediately upon, but not before, the arrival of the transfer event interval. This bit is set by software and is cleared by either of two events: by RAMDAC hardware when the transfer operation has been completed; or by software, indicating the command has been withdrawn.
0	Device Status (1) Busy, Table Unavailable (0) Idle, Table Available	R/O	0	This bit is controlled by the Bt497A/8A and indicates when a transfer is underway.

Transparent Mask Control Register (C[1,0] = 01, Address = $3151)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–8	Reserved	R/O		Reserved. Returns zeros when read.
7–0	Overlay Mask (0) Deselect (1) Select	R/W	N/R	When a bit in this field is set to a logical 1, it selects the bit in the Overlay Color Key Register to be compared with the bits in the X field.

Transparent Color Key Register (C[1,0] = 01, Address = $3152)

Bit(s)	Field	Read / Write	Reset Value	Description
31–8	Reserved	R/O		Reserved. Returns zeros when read.
7–0	Overlay Color Key	R/W	N/R	When Overlays are enabled, the bits in this field that are selected by the Overlay Mask Control Register are compared to the bits in the X field. If they are equal, the underlay pixel is displayed. If they are not equal the Overlay State governs the Color Model selection.

Window Address Mask Register (C[1,0] = 01, Address = $3153)

Bit(s)	Field	Read / Write	Reset Value	Description
31–10	Reserved	R/O		Reserved. Returns zeros when read.
9,8	OMASK (00) Single OWLUT entry (Address 0) (01) Two OWLUT entries (Addresses 0 and 1) (10) Two OWLUT entries (Addresses 0 and 2) (11) All four OWLUT entries	R/W	N/R	The OMASK bits determine the range and entries within the OWLUT that may control the Overlay State.
7,6	Reserved	R/O		Reserved. Returns zeros when read.
5–0	PMASK (0) Deselect (1) Select	R/W	N/R	The PMASK bits determine the range and selection of the 64 entries within the PWLUT that may control the Underlay State.

Shadow-Primary Window Lookup Table (C[1,0] = 01, Address: $3200–$323F) and Active-Primary Window Lookup Table (C[1,0] = 01, Address: $3240–$327F)

Bit(s)	Field	Read / Write	Reset Value	Description
31–16	Reserved	R/O		Reserved. Returns zeros when read.
15	Double Buffering (0) Buffer A (1) Buffer B	R/W	N/R	If Underlays are active, this bit selects pixel data between Port A and Port B, for 2:1 and 4/2:1 Pixel Formats.
14	Color Depth (0) Pseudo-Color (1) True-Color	R/W	N/R	If Underlays are active, this bit selects whether one 8-bit component is replicated to all 3 Color Channels.
13,12	Pseudo-Color Source (00) XO[7:0] (01) R[7:0] (10) G[7:0] (11) B[7:0]	R/W	N/R	If Underlays are active and the Color Depth = Pseudo-Color, these bits determine which pixel component gets replicated.
11–9	Reserved	R/O		Reserved. Returns zeros when read.
8	Color Lookup (0) Bypass the Palette (1) Index through Palette	R/W	N/R	If Underlays are active, this bit controls whether the Underlay pixel state addresses the palette or bypasses it.
7,6	Reserved	R/O		Reserved. Returns zeros when read.
5,4	Palette Table (00) Table 0 (01) Table 1 (10) Table 2 (11) Table 3	R/W	N/R	If Underlays are active, these bits select which of the 4 Palette tables are active for Color lookup.
3–0	Reserved	R/O		Reserved. Returns zeros when read.

Signature Analysis Control Register (C[1,0] = 01, Address = $5000)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–28	Reserved	R/O		Reserved. Returns zeros when read.
27	Data Strobe Mode (0) Signature Analysis Mode (1) Data Strobe Mode	R/W	0	This bit determines the method of high-speed test used. Signature analysis registers are used to hold the test results for both test methods.
26	Signature Analysis Busy (0) Idle (1) Busy	R/O	0	Status of signature analysis logic. A logical 0 indicates that the signature analysis has completed the previous signature acquisition. A logical 1 indicates that a requested signature acquisition has been requested, but not completed.
25	Signature Capture Request (0) Cancel Signature Request (1) Request Signature Capture	R/W	0	Writing a one causes the signature analysis logic to become busy and requests that the signature analysis logic capture a signature. The data written into bits 23 through 0 will be used as the seed for signature acquisition for the frame. Writing a zero cancels any previously requested signature acquisition.
24	Signature Analysis Seed/ Result Dummy Bit	R/W	N/R	Seed value or test result for dummy bit.
23–16	Signature Analysis Seed/ Result Blue DAC	R/W	N/R	Seed value or test result for the blue DAC.
15–8	Signature Analysis Seed/ Result Green DAC	R/W	N/R	Seed value or test result for the green DAC.
7–0	Signature Analysis Seed/ Result Red DAC	R/W	N/R	Seed value or test result for the red DAC.

DAC Control Register (C[1,0] = 01, Address = $5001)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–9	Reserved	R/O		Reserved. Returns zeros when read.
8	Sync Polarity Bit (0) VSYNC* and CSYNC* active low (1) VSYNC* and CSYNC* active high	R/W	0	Reset or writing a zero causes VSYNC* and CSYNC* pins to be active low. Writing a one causes VSYNC* and CSYNC* to be active high.
7	VSYNC* Pin Disable (0) Pin expresses VSYNC* (1) Pin drives high if bit 8 is 0, low if bit 8 is 1	R/W	0	Reset or writing a zero enables the VSYNC* pin. The active state is determined by bit 8 of this register.
6	Pedestal Enable (0) No pedestal (1) 7.5 IRE pedestal	R/W	0	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
5	SYNC on Green Enable (0) Disabled (1) Enabled	R/W	0	This bit specifies whether sync information is to be output onto IOG. It has no effect on the CSYNC* pin.
4	Comparator Result (0) Operand 1 < Operand 2 (1) Operand 1 > Operand 2	R/O	N/R	This bit yields the result of the comparison of the DAC and/or reference output. Comparing operands whose values lie within a few LSBs will yield unpredictable results. Data written to this bit is ignored, as it is read only. The result is valid only after the required comparison setting time is reached (i.e., 5 µs after the operand becomes constant).
3,2	Operand 1 Select (00) Normal Operation (01) Select Green DAC Output (10) Select Red DAC Output (11) Reserved	R/W	00	This field selects Operand 1 of the comparator. For normal operation, the operand 1 and 2 fields should both contain 00.
1,0	Operand 2 Select (00) Normal Operation (01) Select 145 mv Reference (10) Select Blue DAC Output (11) Reserved	R/W	00	This field selects Operand 2 of the comparator. For normal operation, the operand 1 and 2 fields should both contain 00.

Timing Generator Control Register (C[1,0] = 01, Address = $6000)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–7	Reserved	R/O		Reserved. Returns zeros when read.
6	Interlaced Mode (0) Noninterlaced Mode (1) Interlaced Mode	R/W	0	This bit selects the timing generators mode of operation. Reset or writing a zero causes the timing generator to operate in noninterlaced mode. A logical 1 causes the timing generator to operate in interlaced mode.
5	Master Mode (0) Slave (1) Master	R/W	0	This bit controls the FIELD I/O signal direction. Reset or writing a zero to this bit causes the timing generator to be in slave mode, forcing the bidirectional FIELD signal to be an input (provided by the master timing generator). Writing a one causes the timing generator to be in the master mode, forcing the FIELD signal to be an output.
4	Equalization Disable (0) Equalization Enabled (1) Equalization Disabled	R/W	0	If the chip is in interlaced mode, reset or writing a zero to this bit enables the equalizing pulses on CSYNC*. Otherwise, CSYNC* should look like the noninterlaced case. Horizontal syncs occur on CSYNC* except during vertical sync; during vertical sync CSYNC* has serration pulses.
3	Vertical Sync Disable(1) (0) VSYNC* Enabled (1) VSYNC* Disabled	R/W	0	Reset or writing a zero to this bit causes the vertical sync to be enabled on the CSYNC* signal. Disabling VSYNC* during interlaced operation also disables HSYNC*.
2	Horizontal Sync Disable(1) (0) HSYNC* Enabled (1) HSYNC* Disabled	R/W	0	Reset or writing a zero to this bit causes the horizontal sync to be enabled on the CSYNC* signal. Disabling HSYNC* during interlaced operation also disables VSYNC*.
1	Timing Generator Enable (0) Disabled (1) Enabled	R/W	0	Upon reset or writing a zero to this bit, both the Timing Generator Horizontal and Vertical Counters are disabled and reset to zero. Writing a one enables both Timing Generator Horizontal and Vertical Counters.
0	Video Enable (0) Disabled (1) Enabled	R/W	0	Reset or writing a zero to this bit causes the DAC outputs to be blanked. Writing a one, enables them. Any signature acquired during the video disable state will have data equal to zero.
Notes: (1). Bits 3, 2, 0 disabling these output signals does not disable the internal timing generator				

Vertical Blank Negation Point Register (C[1,0] = 01, Address = $6001)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	VBNP	R/W	N/R	This field represents the value of the Timing Generator Vertical Counter that corresponds to the end of the vertical blank interval. The next vertical count [VBNP+1] will trigger the first line of active video. Programmed value should be greater than zero.

Vertical Blank Assertion Point Register (C[1,0] = 01, Address = $6002)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	VBAP	R/W	N/R	This field represents the value of the Timing Generator Vertical Counter that corresponds to the last line of active video. The next vertical count [VBAP+1] will trigger the beginning the vertical blank interval. Programmed value should be greater than zero.

Vertical Sync. Negation Point Register (C[1,0] = 01, Address = $6003)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	VSNP	R/W	N/R	This field represents the value of the Timing Generator Vertical Counter that corresponds to the last line of the vertical sync interval. Programmed value should be greater than zero.

Vertical Sync. Assertion Point Register (C[1,0] = 01, Address = $6004)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	VSAP	R/W	N/R	This field represents the value of the Timing Generator Vertical Counter that corresponds to the line before the beginning of vertical sync. The Timing Generator Vertical Counter will be zero on the next line. VSAP+1 is the total number of lines. Programmed value should be greater than zero.

Horizontal Serration Negation Point Register (C[1,0] = 01, Address = $6005)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	HSERNP	R/W	N/R	This field represents the value of the Timing Generator Horizontal Counter that represents the duration –1 in serial clock periods of the serration pulses on CSYNC* during the vertical sync interval.

Horizontal Blank Negation Point Register (C[1,0] = 01, Address = $6006)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	HBNP	R/W	N/R	This field represents the value of the Timing Generator Horizontal Counter that corresponds to the last serial clock period of blanking before active video on a line. Programmed value should be greater than zero

Horizontal Blank Assertion Point Register (C[1,0] = 01, Address = $6007)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	HBAP	R/W	N/R	This field represents the value of the Timing Generator Horizontal Counter that corresponds to the last serial clock period of active video. Horizontal blanking starts with the next serial clock period. Programmed value should be greater than zero.

Horizontal Sync. Negation Point Register (C[1,0] = 01, Address = $6008)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	HSNP	R/W	N/R	This field represents the value of the Timing Generator Horizontal Counter that corresponds to the last serial clock period of horizontal sync. Programmed value should be greater than zero.

Horizontal Sync. Assertion Point Register (C[1,0] = 01, Address = $6009)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	HSAP	R/W	N/R	This field represents the value of the Timing Generator Horizontal Counter that corresponds to the last serial clock period of a line. HSAP+1 is the total number of serial clock periods in a line. The Timing Generator Horizontal Counter will be zero on the next serial clock period. Programmed value should be greater than zero.

Horizontal SCEN Negation Point Register (C[1,0] = 01, Address = $600A)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	HSCENNP	R/W	N/R	This field represents the value of the Timing Generator Horizontal Counter that corresponds to the last serial clock period that SCEN* will be active. Programmed value should be greater than zero.

Horizontal SCEN Assertion Point Register (C[1,0] = 01, Address = $600B)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	HSCENAP	R/W	N/R	This field represents the value of the Timing Generator Horizontal Counter that corresponds to the start SCEN*. SCEN* is active on the next serial clock period. HSCENAP should be less than HBNP by exactly the number of serial clocks that it takes for pixel data to be clocked in at the Bt497A/8A inputs. HBNP and HSCENAP should always equal (HBAP and HSCENNP). Programmed value should be greater than zero.

Equalizing Pulse Negation Point Register (C[1,0] = 01, Address = $600C)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	EQNP	R/W	N/R	This field represents the value of the Timing Generator Horizontal Counter that corresponds to the last serial clock period of an equalizing pulse. Equalizing pulses always begin at horizontal coordinate 0. Equalizing pulses are generally one-half the duration of horizontal sync. Programmed value should be greater than zero.

Equalization Interval Negation Point Register (C[1,0] = 01, Address = $600D)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	EINP	R/W	N/R	This field represents the value of the Timing Generator Vertical Counter that corresponds to the last half-line following vertical sync on which to generate an equalizing pulse. Programmed value should be greater than zero.

Equalization Interval Assertion Point Register (C[1,0] = 01, Address = $600E)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	EIAP	R/W	N/R	This field represents the value of the Timing Generator Vertical Counter that corresponds to the half-line before the beginning of the pre-equalization interval. The first equalizing pulse before vertical sync will occur on the next half-line. Programmed value should be greater than zero.

Timing Generator Vertical Counter (C[1,0] = 01, Address = $600F)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	Vertical Line Counter	R/O	0	This read-only field gives the real-time value of the Timing Generator Vertical Counter at the time it is read by the MPU.

Timing Generator Horizontal Counter (C[1,0] = 01, Address = $6010)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–12	Reserved	R/O		Reserved. Returns zeros when read.
11–0	Horizontal Serial Clock Counter	R/O	1	This read-only field gives the real-time value of the Timing Generator Horizontal Counter at the time it is read by the MPU.

Device Identification Register (C[1,0] = 01, Address = $8000)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–28	Device Revision	R/O	$A	Manufacturer Marketing Revision. The value stored in this field can be read through the JTAG Tap Access Port or the MPU Port.
27–12	Device Part Number	R/O	$236E	Manufacturer Part Number. The value stored in this field can be read through the JTAG Tap Access Port or the MPU Port.
11–1	Device Manufacturer ID $0D6	R/O	$0D6	Manufacturer Identification Number. The value stored in this field can be read through the JTAG Tap Access Port or the MPU Port.
0	Bit 0 = 1	R/O	1	Final value for the register is $A236E1AD

Monitor Port Data Register (C[1,0] = 01, Address = $8001)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–28	Reserved	R/O		Reserved. Returns zeros when read.
1	SDA Data	R/W	1	The SDA Data bit determines the drive state of the open-drain SDA pin. A 0 causes the pin to drive an active low level. A 1 causes the pin to be 3-stated. Its level will be determined by the external Monitor connection.
0	SCL Data	R/W	1	The SCL Data bit determines the drive state of the open-drain SCL pin. A 0 causes the pin to drive an active low level. A 1 causes the pin to be 3-stated. Its level will be determined by the external Monitor connection.

Monitor Port Sense Register (C[1,0] = 01, Address = $8002)

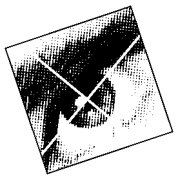
Bit(s)	Field	Read/ Write	Reset Value	Description
31–2	Reserved	R/O		Reserved. Returns zeros when read.
1	SDA Sense	R/O	N/R	The SDA Sense bit allows the external SDA pin level to be detected, whenever the corresponding SDA Data bit is 1. If SDA Data is 0, then SDA Sense will always contain 0. The Sense level is captured on the first falling edge of CE* during MPU read cycle.
0	SCL Sense	R/O	N/R	The SCL Sense bit allows the external SCL pin level to be detected, whenever the corresponding SCL Data bit is 1. If SCL Data is 0, then SCL Sense will always contain 0. The Sense level is captured on the first falling edge of CE* during MPU read cycle.

Cursor Control Register (C[1,0] = 11, Address = $100)

Bit(s)	Field	Read/ Write	Reset Value	Description
31–2	Reserved	R/O	N/R	Reserved. Returns zeros when read.
1	64 x 64 Cursor Plane1 Display Enable (0) Enabled (1) Disabled	R/W	$0	This bit specifies whether Plane1 of the 64 x 64 cursor is to be displayed.
0	64 x 64 Cursor Plane0 Display Enable (0) Enabled (1) Disabled	R/W	$0	This bit specifies whether Plane0 of the 64 x 64 cursor is to be displayed.

Cursor Position Register (C[1,0] = 11, Address = $104)

Bit(s)	Field	Read/ Write	Reset Value	Description
31	(0) Positive (1) Negative	R/W	N/R	Sign for the Y position of the cursor.
30–28	Reserved	R/O	N/R	Returns zeros when read.
27–16	Y Position	R/W	N/R	Y cursor position, in number of lines, of the cursor. Values from $0000 to $0FFF can be written.
15	(0) Positive (1) Negative	R/W	N/R	Sign for the X position of the cursor.
14–12	Reserved	R/O	N/R	Reserved. Returns zeros when read.
11–0	X Position	R/W	N/R	X cursor position, in number of pixels, of the cursor. Values from $0000 to $0FFF can be written.



PC BOARD LAYOUT CONSIDERATIONS

Optimize the Bt497A/8A layout for lowest noise on the power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing. This layout enables the Bt497A/8A to be located as close to the power supply connector and the video output connector as possible.

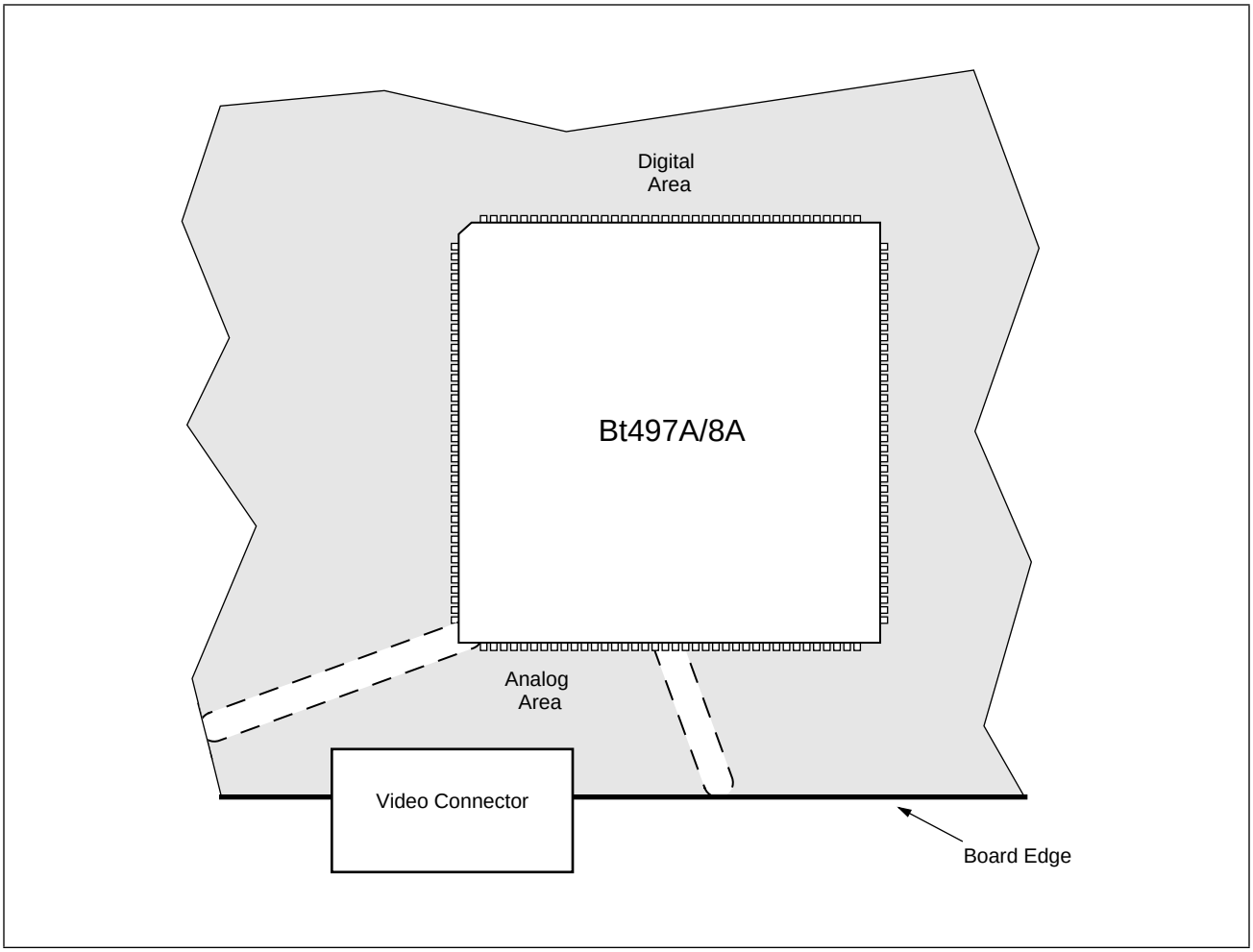
A well-designed power distribution network is critical to eliminating digital switching noise. The ground planes must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. Use the ground layer as a shield to isolate noise from the analog traces with layer 1 (top), the analog traces; layer 2, the ground plane (preferable analog ground plane); and layer 3, the analog power plane. Use the remaining layers for digital traces and digital power supplies.

Power and Ground Planes

The power and ground planes need isolation gaps at least 1/8-inch wide to minimize digital switching noise effects on the analog signals and components. Gaps are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector (a sample layout is shown in Figure 31). It is necessary to have separate planes for VAA3 and VAA5.

The VAA3 plane should cover all the digital signal line terminations at the Bt497A/8A with occasional openings for VAA5 access.

Figure 31. Representative Power/Ground Analog Area Layout



Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained by providing a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor to decouple each group of VAA3 and VAA5 pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins.

The 33 µF capacitor shown in Figure 32 and Table 18 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the VAA3, VAA5, and GND pins, using short, wide traces.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

Figure 32. Typical Analog Connection Diagram

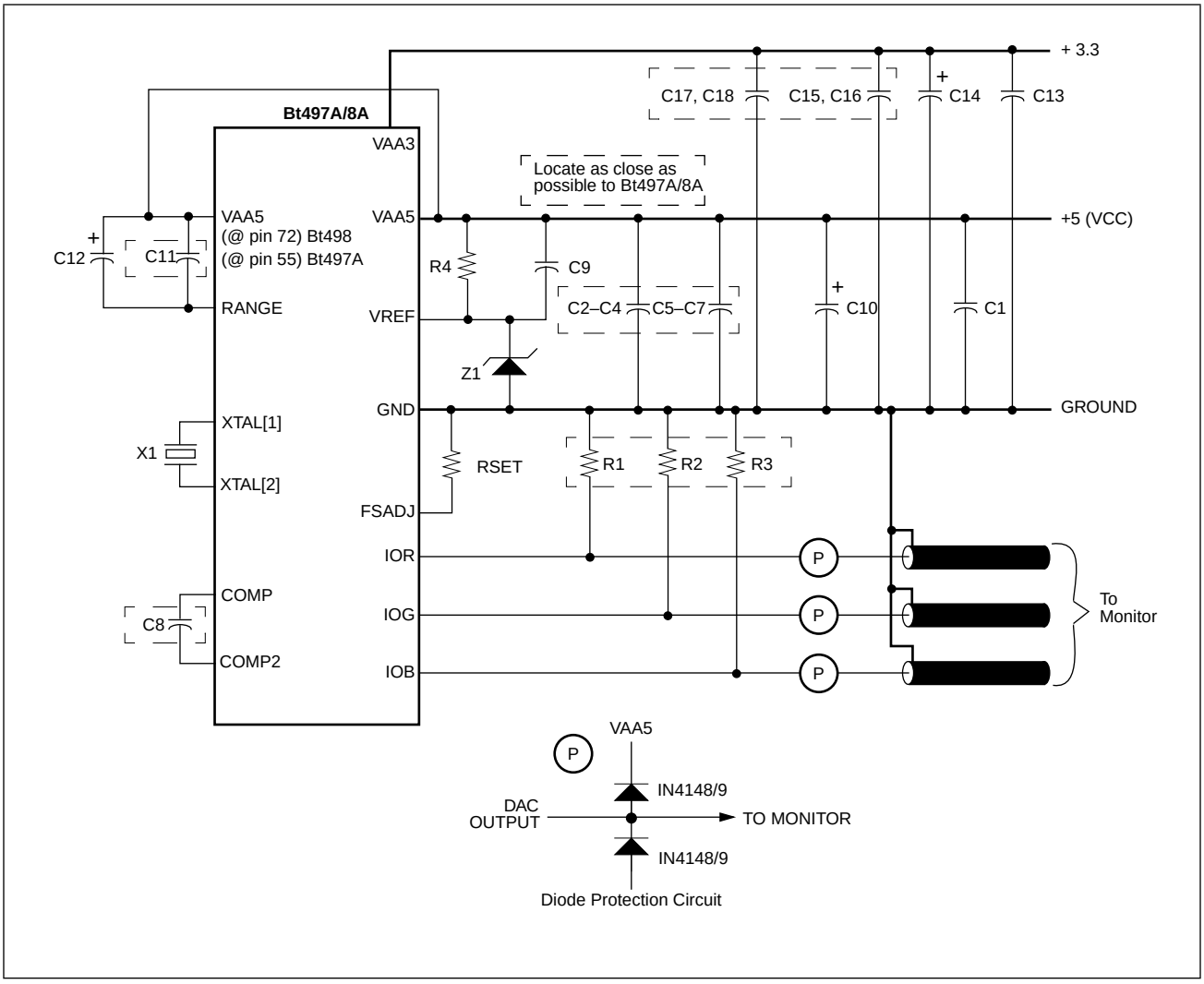


Table 18. Typical Parts List

Location	Description	Vendor Part Number
C1–C4, C8, C9, C13, C17, C18	0.1 µF Ceramic capacitor	Erie RPE112Z5U104M50V
C5–C7, C11, C15, C16	0.01 µF Ceramic chip capacitor	AVX 12102T103QA1018
C10, C14	33 µF Tantalum capacitor	Mallory CSR13F336KM
C12	4.7 µF Tantalum capacitor	Mallory CSR13F477KM
R1, R2, R3	75 Ω 1% Metal film resistor	Dale CMF-55C
R4	1000 Ω 5% Metal film resistor	
RSET	1% Metal film resistor	Dale CMF-55C
X1	10–24 MHz Crystal	
Z1	1.2 V Voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt497A/8A. Also, the VAA5 pins shown refer to the analog VAA5s which are located in the vicinity of the other analog pins.

COMP Decoupling

The COMP pin must be decoupled to COMP2, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close to the COMP and COMP2 pins as possible. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help fix the problem.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA5. If VAA5 is excessively noisy, better performance may be obtained by decoupling VREF to GND. Providing alternate PCB pads (one to VAA5 and one to GND) is recommended for the VREF decoupling capacitor.

Digital Signal Interconnect

The digital inputs to the Bt497A/8A should be isolated as much as possible from the analog outputs and other analog circuitry. These input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should be no faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if they do not match the source and destination impedance. This degrades signal fidelity if the line length reflection time is greater than one-fourth the signal edge time. Line termination or line length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing is reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

The clock driver and all other digital devices on the circuit board must have adequate decoupling to prevent the noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt497A/8A should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

To maximize the high-frequency power supply rejection, the video output signals should overlay the analog ground plane.

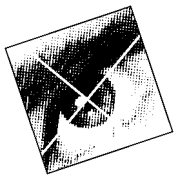
For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt497A/8A analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from “hot-switching” AC-coupled monitors.

The diode protection circuit shown in Figure 32 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).



APPLICATION INFORMATION

Test Features of the Bt497A/8A

The Bt497A/498A contains a Signature Analysis Control Register (SAR), a DAC output comparator, and JTAG test structures that assist the user in evaluating the performance and functionality of the part. This section explains the operating usage of these test features.

Signature Analysis Control Register (SAR)

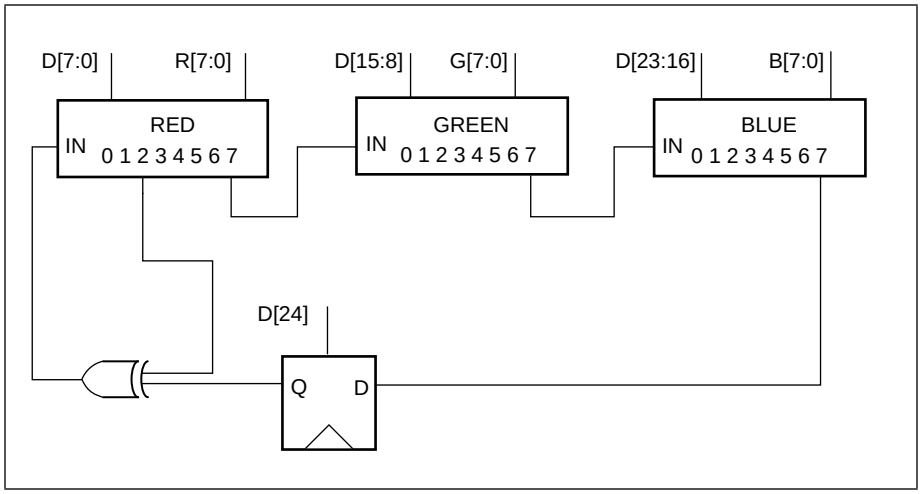
When enabled, the output SAR operates with the 24 bits of data that are presented to the DAC inputs. These 24-bit vectors represent a single pixel color, and are presented simultaneously as inputs to the red, green, and blue SARs, as well as the three on-chip DACs.

The SAR acts as a wide linear feedback shift register on each succeeding DAC input. To simplify the feedback circuitry a 25th bit has been added, but has no corresponding test input. It can be written and read through the MPU port as bit 24, which represents the LSB in the fourth CE* load cycle.

The Bt497A/8A will only generate signatures during the active video of two fields, starting on the first even field following a Signature Capture Request in the SAR. After the signature has been acquired, the SAR is available for reading and writing via the MPU port.

Typically, the user will write a specific 25-bit seed value into the SAR, then set the Signature Capture Request bit. A full field of known pixel information will then be input to the chip, after which the resultant 25-bit signature can be read by the MPU. The 25-bit signature results from the same color data that is fed to the DACs. Thus, overlay, cursor, and palette bypass data validity is also tested using the SARs. The linear feedback configuration is shown in Figure 33.

Figure 33. Signature Analysis Feedback Circuit



Analog Comparator

The other dedicated test structure in the Bt497A/8A is the analog comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the DAC Control Register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the Timing Generator Test Register. The capture occurs at the bottom-right point of the 64 x 64 cursor bit map.

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, until capture.

Device Identification Register

The Bt497A/8A incorporates a Device Identification Register (Figure 34) which can be accessed via the MPU port. The register is read only and uniquely identifies the device in accordance with requirements and principles set forth by the JEDEC organization. The Device Identification value may also be read out via the JTAG interface.

The final value read by the MPU port is $A236E1AD.

Figure 34. Device Identification Register

Version				**Part Number**																**Manufacturer ID**											
1	0	1	0	0	0	1	0	0	0	1	1	0	1	1	0	1	1	1	0	0	0	0	1	1	0	1	0	1	1	0	1
$A				9070, $236E																$0D6											
4 bits				16 bits																11 bits											

JTAG Registers

The Bt497A/8A incorporates special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group (JTAG). Conforming to IEEE P1149.1, *Standard Test Access Port and Boundary Scan Architecture*, the Bt497A/8A has dedicated pins that are used for test purposes only.

JTAG uses boundary-scan cells placed at each digital pin, both inputs and outputs, shown in Figure 35. All scan cells are interconnected into a Boundary-Scan Register (BSR), which applies or captures test data used for functional verification of the Bt497A/8A. Note that even though the Bt497A has 64 pixel pins connected to its package, JTAG users of the Bt497A still need to account for all the unconnected Port B boundary-scan cells when they utilize the Bt497A Boundary-Scan Register. JTAG is particularly useful for board testers using functional testing methods.

JTAG has five dedicated pins that comprise the Test Access Port (TAP): Test Mode Select (TMS), Test Clock (TCK), Test Data Input (TDI), Test Data Out (TDO) and Test Reset (TRST*). Connection verification of the Bt497A/8A can be achieved through these five TAP pins. With boundary-scan cells at each digital pin, the Bt497A/8A is able to apply and capture the logic level. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all of the pins necessary to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the Bt497A/8A from the other components on the board, the user has easy access to all Bt497A/8A digital pins through the TAP and can perform complete interconnect testing without using expensive bed-of-nails testers.

The bidirectional MPU port and other digital I/Os require extra attention with respect to JTAG. Because JTAG requires full control over each digital pin, additional Output Enable (OE) cells are included in the BSR for the I/O and open-drain pins. Table 19 describes the scope and effects of the <OEFM> and <OEMPU> control cells.

Tables 20 and 21 give further details concerning the JTAG accessible registers and test instructions supported.

A BSDL has been created with the AT&T BSD Editor. Should JTAG testing be implemented, a disk with an ASCII version of the complete BSDL file may be obtained by calling 1-800-2BtApps.

Figure 35. JTAG Boundry Scan Registers

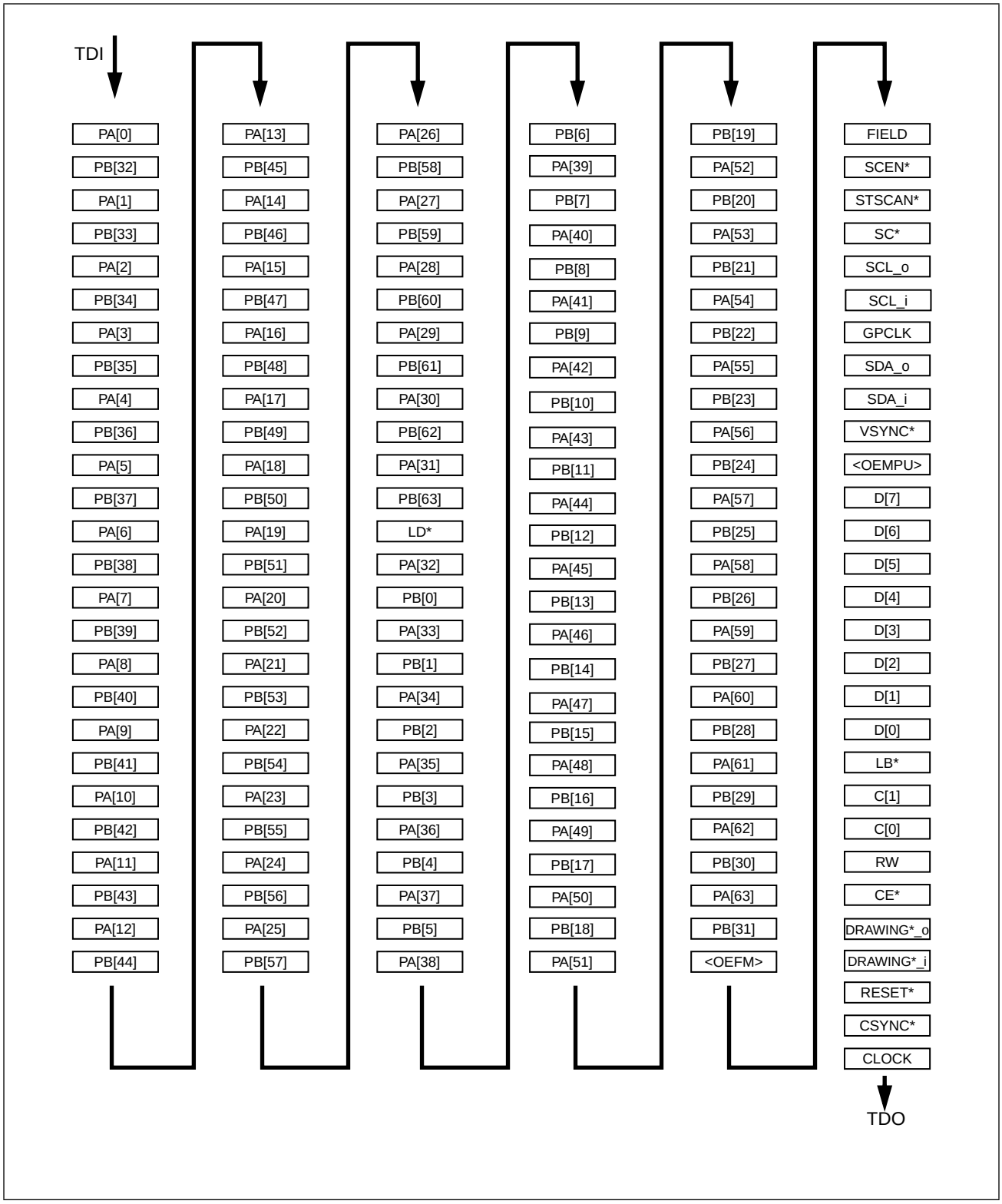


Table 19. JTAG Bidirectional Control

Control Cell <OEFM> <OEMPU>	Bidirect Pins FIELD D[7:0]
Control = 1	Bidirect is Output mode. Level driven is determined by value scanned into corresponding Data cell.
Control = 0	Bidirect is Input mode. Pin level may be latched into the corresponding Data cell.

Table 20. JTAG Registers

Name	Width	Description
Instruction Register (IR)	4	Holds and decodes active instruction.
Boundary Scan Register (BSR)	159	Corresponds to all chip digital pins.
Bypass Register (BYR)	1	Holding D–FF, for bypassing chip.
Device ID Register (DID)	32	Contains official part and manufacturing numbers.

Table 21. JTAG Instructions

Code	Name	Register	Description
0	EXTEST	BSR	Scan in test-vector, apply at outputs.
1	INTEST	BSR	Scan in test-vector, apply at inputs.
2	SAMPLE	BSR	Capture pin levels in BSR, scan out.
3–5, 7	<Reserved>		
6	IDCODE	BYR	Pass data from TDI direct to TDO.
8–$F	BYPASS	DID	Scan out the [read-only] DID information.

Initializing the Bt497A/8A

Power up the VAA5 and VAA3 supplies in any order.

Assert and release TRST*.

Assert and release RESET* twice.

The write instructions given in the MPU initialization sequence will configure the Bt497A/8A to the following settings:

2:1 pixel format

Block Cursor, enabled for both planes

Cursor position X = 48, Y = 64

Sync-on-green enabled, 7.5 IRE blank pedestal, no analog compare

PLL enabled to 135 MHz (assumes 13.5 MHz crystal, plus M = 40, N = 4, and L = 1)

All (active) WID locations programmed to:

- True color, with input from port_A, color model = palette

Timing generator programmed to:

- 1280 x 1024, 76 Hz noninterlaced mode, VSYNC* enabled, HSYNC* enabled, EQUALIZING disabled.

The following register states will endure from their Reset defaults:

- SAR is not enabled
- Serial monitor is all inputs
- No transparent overlay, No double buffer, display enabled, pullups enabled
- No pending transfer for WID RAM

MPU Initialization Sequence

For best results, follow the Order of Writes given below. It is important to have the intended Pixel Format Register selection done before enabling the PLL via the PLL Control Register. Every MPU access consists of four CE* cycles, where each CE* cycle transfers 1 byte.

Pixel and Clock Control	**C1,C0**
Write $1000 to Configuration Pointer	00
Write 0 to Pixel Format Register	01
Write 0 to Configuration Pointer	00
Write $4228 to pixel PLL Control Register	01
Load Cursor: Bitmap, Colors, Position	
Write 0 to Cursor Pointer	10
Write $FFFFFFFF to Cursor RAM (location 0)	11
Write $FFFFFFFF to Cursor RAM (location 1)	11
:	:
Write $FFFFFFFF to Cursor RAM (location $FF)	11
Write red, green, blue data to Color 1	11
Write red, green, blue data to Color 2	11
Write red, green, blue data to Color 3	11
Write $400030 to Cursor Position Register	11
Load Palette RAM	**C1,C0**
Write $2000 to Configuration Pointer	00
Write red, green, blue data to Palette 0	01
Write red, green, blue data to Palette 1	01
:	:
Write red, green, blue data to Palette $FF	01
Load WID Registers, DAC Control	
Write $3120 to Configuration Pointer	00
Write $10 to Active WID (location 0)	01
Write $10 to Active WID (location 1)	01
:	:
Write $10 to Active WID (location $1f)	01
Write $5001 to Configuration Pointer	00
Write $60 to DAC Control Register	01

Load Timing Generator Registers	**C1,C0**
Write $6001 to Configuration Pointer	00
Write $027 to VBNP Register	01
Write $427 to VBAP Register	01
Write $007 to VSNP Register	01
Write $429 to VSAP Register	01
Write $31F to HSERNP Register	01
Write $0AF to HBNP Register	01
Write $32F to HBAP Register	01
Write $01F to HSNP Register	01
Write $33F to HSAP Register	01
Write $32E to HSCENNP Register	01
Write $0AE to HSCENAP Register	01
Release Timing Generator, Begin Display	
(Assumes frame buffer or pixel generator are ready:)	
Write $6000 to Configuration Pointer	00
Write $023 to Timing Generator Control Register	01
Enable WID transfer control post Timing Generator Enable (Optional)	

Table 22. 1280 x 1024 Noninterlaced Register Values

Register	Value (dec)	Hex
VBNP	39	$027
VBAP	1063	$427
VSNP	7	$007
VSAP	1065	$429
HSERNP	799	$31F
HBNP	175	$0AF
HBAP	815	$32F
HSNP	31	$01F
HSAP	831	$33F
HSCENNP	814	$32E
HSCENAP	174	$0AE

1280 x 1024 x 76 Hz Noninterlaced Display

See Table 22 for noninterlaced register values.
Horizontal Pixels: 1280
Vertical Lines: 1024
Horizontal Frequency: 81.13 KHz
Horizontal Sync: 0.474 µS
Horizontal Unblanked: 9.48 µS
Horizontal Blanking: 2.84 µS
Total Vertical Lines: 1066
Vertical Frequency: 76.11 Hz
Vertical Sync: 8 Lines
Pixel Clock: 135 Mhz
Crystal: 13.5 Mhz
Frame Buffer Pipeline: 1 serial clock cycle

NTSC Interlaced Display

See Table 23 for NTSC register values.
Horizontal Pixels: 640
Vertical Lines: 480
Horizontal Frequency: 15.73 KHz
Horizontal Sync: 4.73 µS
Horizontal Unblanked: 52.15 µS
Horizontal Blanking: 11.41 µS
Total Vertical Lines: 525
Vertical Frequency: 59.94 Hz
Vertical Sync: 3 Lines
Equal. Pulses: 6 Pre and Post
12 full lines after equal before 1st line of active video for field 0.
Pixel Clock: 12.273 Mhz
Crystal: 13.5 Mhz
PLL Control Register
PLL: Enable
M = 80
N = 11
L = 8
Pixel Format Control Register
Pixel Format: 4/2:1 or 2:1
Timing Generation Control Register
EQUAL*: Enabled
Interlaced mode: Enabled
VSYNC*: Enabled
HSYNC*: Enabled
Frame Buffer Pipeline: 1 serial clock cycle

Table 23. NTSC Register Values

Register	Value (dec)	Hex
VBNP	37	$25
VBAP	517	$205
VSNP	5	$5
VSAP	524	$20C
HSERNP	165	$A5
HBNP	59	$3B
HBAP	184	$B8
HSNP	28	$1C
HSAP	194	$C2
HSCENNP	183	$B7
HSCENAP	58	$3A
EQNP	13	$D
EINP	11	$B
EIAP	518	$206

PAL Interlaced Display

See Table 24 for PAL register values.
Horizontal Pixels: 768
Vertical Lines: 625
Horizontal Frequency: 15.62 KHz
Horizontal Sync: 4.79 µS
Horizontal Unblanked: 52.51 µS
Horizontal Blanking: 11.49 µS
Total Vertical Lines: 570
Vertical Frequency: 50 Hz
Vertical Sync: 2.5 Lines
Equalizing Pulses:5 Pre and Post
17 full lines after equal before 1st line of active video for field 0
Pixel Clock: 14.625 Mhz
Crystal = 13.5 Mhz
PLL Control Register
PLL: Enable
M = 52
N = 6
L = 8
Pixel Format Control Register
Pixel Format: 4/2:1 or 2:1
Timing Generation Control Register
EQUAL*: Enabled
Interlaced Mode: Enabled
VSYNC*: Enabled
HSYNC*: Enabled
Frame Buffer Pipeline: 1 serial clock cycle

Table 24. PAL Register Values

Register	Value (dec)	Hex
VBNP	43	$2B
VBAP	618	$26A
VSNP	4	$4
VSAP	624	$270
HSERNP	200	$C8
HBNP	76	$4C
HBAP	226	$E2
HSNP	34	$22
HSAP	233	$E9
HSCENNP	225	$E1
HSCENAP	75	$4B
EQNP	16	$10
EINP	9	$9
EIAP	619	$26B

PLL Initialization

The Bt497A/8A-Generated VRAM Shift Clock and Pixel PLL-Generated Pixel Clock

In this configuration, the pixel clock is generated using the on-chip Pixel PLL. SC* runs continuously and is meant to shift out pixel data from the VRAMs. Here, a relatively low-frequency crystal is connected to the XTAL1 and XTAL2 inputs, instead of using an ECL oscillator operated on a pseudo-ECL supply (i.e., +5 and GND) connected to the CLOCK and CLOCK* inputs of the Bt497A/8A, as shown in Figures 5, 6, and 7 in the Circuit Description section of this document.

Crystal Frequency Selection

The crystal frequency should be selected based on the required pixel rate(s) and the display pixel rate tolerance. The desired ratio for the PLL can then be computed by dividing the required pixel rate by the crystal frequency, looking up the M and N values in the ratio table (Table 25) for the closest ratio, and ensuring that the display can still operate satisfactorily within the best-fit pixel rate and associated CRT timings. It is assumed that the choice of crystal will be dictated by desired pixel frequencies, and that GPCLK frequency choices are lower priority.

Ratio Selection

The PLL clock ratios are set by programming the M and N values through the MPU port.

Table 25 and Table 26 show the complete range of pixel clock and GPCLK frequencies corresponding to various settings for M, N, and L. Table 25 shows VCO frequency only. Pixel rate is further selectable to be 1/1, 1/2, 1/4, or 1/8 of VCO frequency by programming the L value.

Pixel PLL Deselection

Users planning to utilize the two PLLs exclusively should still provide definite connections to the CLOCK and CLOCK* pins, as shown in Figure 36. With this hookup, the user may shut off the pixel display operation of the chip at any time to save AC power. This clock shut off is accomplished by writing a 0 into bit 14 of the Pixel PLL Control Register. Among other effects, note that this will also force the SC* output to a DC state. The two PLLs will be deselected by chip Reset.

Figure 36. CLOCK and XTAL Connections for PLL Operation

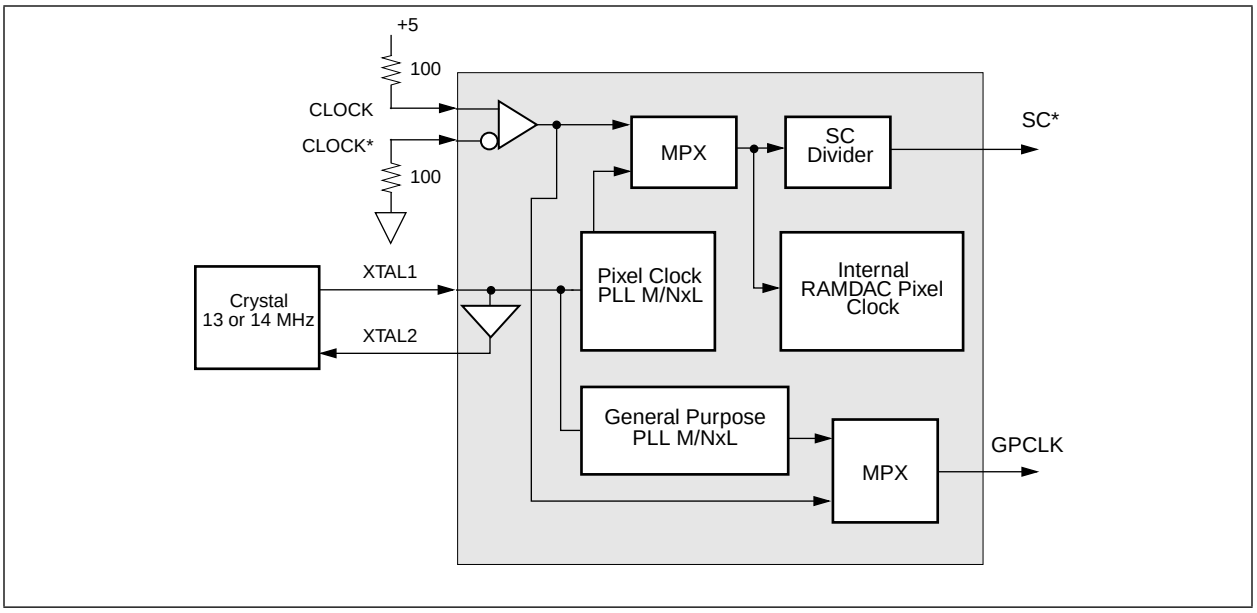


Table 25. Pixel Rate Selection *(1 of 6)*

Pixel Clock Rate (MHz), L = 0		**M/N**	**M**	**N**
w/Reference Crystal =				
13.50 MHz	**14.31818 MHz**			
N/A	96.136	6.714	47	7
N/A	96.322	6.727	74	11
N/A	96.648	6.750	54	8
N/A	97.045	6.778	61	9
N/A	97.364	6.800	34	5
N/A	97.624	6.818	75	11
N/A	97.841	6.833	41	6
N/A	98.182	6.857	48	7
N/A	98.437	6.875	55	8
N/A	98.636	6.889	62	9
N/A	98.795	6.900	69	10
N/A	98.926	6.909	76	11
N/A	100.227	7.000	35	5
N/A	101.529	7.091	78	11
N/A	101.659	7.100	71	10
96.000	101.818	7.111	64	9
96.188	102.017	7.125	57	8
96.429	102.273	7.143	50	7
96.750	102.614	7.167	43	6
96.955	102.831	7.182	79	11
97.200	103.091	7.200	36	5
97.500	103.409	7.222	65	9
97.875	103.807	7.250	58	8
98.182	104.132	7.273	80	11
98.357	104.318	7.286	51	7
98.550	104.523	7.300	73	10
99.000	105.000	7.333	44	6
99.563	105.597	7.375	59	8
99.900	105.955	7.400	37	5
100.286	106.364	7.429	52	7

Table 25. Pixel Rate Selection *(2 of 6)*

Pixel Clock Rate (MHz), L = 0		M/N	M	N
w/Reference Crystal =				
13.50 MHz	14.31818 MHz			
100.500	106.591	7.444	67	9
101.250	107.386	7.500	45	6
102.000	108.182	7.556	68	9
102.214	108.409	7.571	53	7
102.600	108.818	7.600	38	5
102.938	109.176	7.625	61	8
103.500	109.773	7.667	46	6
103.950	110.250	7.700	77	10
104.143	110.455	7.714	54	7
104.625	110.966	7.750	62	8
105.000	111.364	7.778	70	9
105.300	111.682	7.800	39	5
105.750	112.159	7.833	47	6
106.071	112.500	7.857	55	7
106.313	112.756	7.875	63	8
106.500	112.955	7.889	71	9
106.650	113.114	7.900	79	10
108.000	114.545	8.000	32	4
109.500	116.136	8.111	73	9
109.688	116.335	8.125	65	8
109.929	116.591	8.143	57	7
110.250	116.932	8.167	49	6
110.700	117.409	8.200	41	5
111.000	117.727	8.222	74	9
111.375	118.125	8.250	33	4
111.857	118.636	8.286	58	7
112.500	119.318	8.333	50	6
113.063	119.915	8.375	67	8
113.400	120.273	8.400	42	5
113.786	120.682	8.429	59	7

Table 25. Pixel Rate Selection *(3 of 6)*

Pixel Clock Rate (MHz), L = 0		M/N	M	N
w/Reference Crystal =				
13.50 MHz	14.31818 MHz			
114.000	120.909	8.444	76	9
114.750	121.705	8.500	34	4
115.500	122.500	8.556	77	9
115.714	122.727	8.571	60	7
116.100	123.136	8.600	43	5
116.438	123.494	8.625	69	8
117.000	124.091	8.667	52	6
117.643	124.773	8.714	61	7
118.125	125.284	8.750	35	4
118.500	125.682	8.778	79	9
118.800	126.000	8.800	44	5
119.250	126.477	8.833	53	6
119.571	126.818	8.857	62	7
119.813	127.074	8.875	71	8
120.000	127.273	8.889	80	9
121.500	128.864	9.000	36	4
123.188	130.653	9.125	73	8
123.429	130.909	9.143	64	7
123.750	131.250	9.167	55	6
124.200	131.727	9.200	46	5
124.875	132.443	9.250	37	4
125.357	132.955	9.286	65	7
126.000	133.636	9.333	56	6
126.563	134.233	9.375	75	8
126.900	134.591	9.400	47	5
127.286	135.000	9.429	66	7
128.250	136.023	9.500	38	4
129.214	137.045	9.571	67	7
129.600	137.455	9.600	48	5
129.938	137.812	9.625	77	8

Table 25. Pixel Rate Selection *(4 of 6)*

Pixel Clock Rate (MHz), L = 0		M/N	M	N
w/Reference Crystal =				
13.50 MHz	14.31818 MHz			
130.500	138.409	9.667	58	6
131.143	139.091	9.714	68	7
131.625	139.602	9.750	39	4
132.300	140.318	9.800	49	5
132.750	140.795	9.833	59	6
133.071	141.136	9.857	69	7
133.313	141.392	9.875	79	8
135.000	143.182	10.000	40	4
136.929	145.227	10.143	71	7
137.250	145.568	10.167	61	6
137.700	146.045	10.200	51	5
138.375	146.761	10.250	41	4
138.857	147.273	10.286	72	7
139.500	147.955	10.333	62	6
140.400	148.909	10.400	52	5
140.786	149.318	10.429	73	7
141.750	150.341	10.500	42	4
142.714	151.364	10.571	74	7
143.100	151.773	10.600	53	5
144.000	152.727	10.667	64	6
144.643	153.409	10.714	75	7
145.125	153.920	10.750	43	4
145.800	154.636	10.800	54	5
146.250	155.114	10.833	65	6
146.571	155.455	10.857	76	7
148.500	157.500	11.000	44	4
150.429	159.545	11.143	78	7
150.750	159.886	11.167	67	6
151.200	160.364	11.200	56	5
151.875	161.080	11.250	45	4

Table 25. Pixel Rate Selection *(5 of 6)*

Pixel Clock Rate (MHz), L = 0		M/N	M	N
w/Reference Crystal =				
13.50 MHz	14.31818 MHz			
152.357	161.591	11.286	79	7
153.000	162.273	11.333	68	6
153.900	163.227	11.400	57	5
154.286	163.636	11.429	80	7
155.250	164.659	11.500	46	4
156.600	166.091	11.600	58	5
157.500	167.045	11.667	70	6
158.625	168.239	11.750	47	4
159.300	168.955	11.800	59	5
159.750	169.432	11.833	71	6
162.000	171.818	12.000	48	4
164.250	174.205	12.167	73	6
164.700	174.682	12.200	61	5
165.375	175.398	12.250	49	4
166.500	176.591	12.333	74	6
167.400	177.545	12.400	62	5
168.750	178.977	12.500	50	4
170.100	180.409	12.600	63	5
171.000	181.364	12.667	76	6
172.125	182.557	12.750	51	4
172.800	183.273	12.800	64	5
173.250	183.750	12.833	77	6
175.500	186.136	13.000	52	4
177.750	188.523	13.167	79	6
178.200	189.000	13.200	66	5
178.875	189.716	13.250	53	4
180.000	190.909	13.333	80	6
180.900	191.864	13.400	67	5
182.250	193.295	13.500	54	4
183.600	194.727	13.600	68	5

Table 25. Pixel Rate Selection *(6 of 6)*

Pixel Clock Rate (MHz), L = 0		**M/N**	**M**	**N**
w/Reference Crystal =				
13.50 MHz	**14.31818 MHz**			
185.625	196.875	13.750	55	4
186.300	197.591	13.800	69	5
189.000	200.455	14.000	56	4
191.700	203.318	14.200	71	5
192.375	204.034	14.250	57	4
194.400	206.182	14.400	72	5
195.750	207.614	14.500	58	4
197.100	209.045	14.600	73	5
199.125	211.193	14.750	59	4
199.800	211.909	14.800	74	5
202.500	214.773	15.000	60	4
205.200	217.636	15.200	76	5
205.875	218.352	15.250	61	4
207.900	220.500	15.400	77	5
209.250	221.932	15.500	62	4
210.600	223.364	15.600	78	5
212.625	225.511	15.750	63	4
213.300	226.227	15.800	79	5
216.000	229.091	16.000	64	4
219.375	232.670	16.250	65	4
222.750	236.250	16.500	66	4
226.125	239.830	16.750	67	4
239.625	N/A	17.750	71	4

Table 26. GPCLK PLL Programming Table*(1 of 7)*

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
N/A	10.7386	30	5	3
N/A	10.9176	61	10	3
N/A	10.9375	55	9	3
N/A	10.9624	49	8	3
N/A	10.9943	43	7	3
N/A	11.0369	37	6	3
N/A	11.0966	31	5	3
N/A	11.1364	56	9	3
N/A	11.1861	25	4	3
N/A	11.25	44	7	3
10.6313	11.2756	63	10	3
10.6875	11.3352	38	6	3
10.7578	11.4098	51	8	3
10.8	11.4545	32	5	3
10.8482	11.5057	45	7	3
10.875	11.5341	58	9	3
10.9688	11.6335	26	4	3
11.0625	11.733	59	9	3
11.0893	11.7614	46	7	3
11.1375	11.8125	33	5	3
11.1797	11.8572	53	8	3
11.25	11.9318	40	6	3
11.3304	12.017	47	7	3
11.3906	12.081	27	4	3
11.4375	12.1307	61	9	3
11.475	12.1705	34	5	3
11.5313	12.2301	41	6	3
11.5714	12.2727	48	7	3
11.6016	12.3047	55	8	3
11.625	12.3295	62	9	3
11.8125	12.5284	28	4	3

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
12.0234	12.7521	57	8	3
12.0536	12.7841	50	7	3
12.0938	12.8267	43	6	3
12.15	12.8864	36	5	3
12.2344	12.9759	29	4	3
12.2946	13.0398	51	7	3
12.375	13.125	44	6	3
12.4453	13.1996	59	8	3
12.4875	13.2443	37	5	3
12.5357	13.2955	52	7	3
12.6563	13.4233	30	4	3
12.7768	13.5511	53	7	3
12.825	13.6023	38	5	3
12.8672	13.647	61	8	3
12.9375	13.7216	46	6	3
13.0179	13.8068	54	7	3
13.0781	13.8707	31	4	3
13.1625	13.9602	39	5	3
13.2188	14.0199	47	6	3
13.2589	14.0625	55	7	3
13.2891	14.0945	63	8	3
13.5	14.3182	32	4	3
13.7411	14.5739	57	7	3
13.7813	14.6165	49	6	3
13.8375	14.6761	41	5	3
13.9219	14.7656	33	4	3
13.9821	14.8295	58	7	3
14.0625	14.9148	50	6	3
14.175	15.0341	42	5	3
14.2232	15.0852	59	7	3
14.3438	15.2131	34	4	3

Table 26. GPCLK PLL Programming Table*(2 of 7)*

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
14.4643	15.3409	60	7	3
14.5125	15.392	43	5	3
14.625	15.5114	52	6	3
14.7054	15.5966	61	7	3
14.7656	15.6605	35	4	3
14.85	15.75	44	5	3
14.9063	15.8097	53	6	3
14.9464	15.8523	62	7	3
15.1875	16.108	36	4	3
15.4688	16.4062	55	6	3
15.525	16.4659	46	5	3
15.6094	16.5554	37	4	3
15.75	16.7045	56	6	3
15.8625	16.8239	47	5	3
16.0313	17.0028	38	4	3
16.2	17.1818	48	5	3
16.3125	17.3011	58	6	3
16.4531	17.4503	39	4	3
16.5375	17.5398	49	5	3
16.5938	17.5994	59	6	3
16.875	17.8977	40	4	3
17.1563	18.196	61	6	3
17.2125	18.2557	51	5	3
17.2969	18.3452	41	4	3
17.4375	18.4943	62	6	3
17.55	18.6136	52	5	3
17.7188	18.7926	42	4	3
17.8875	18.9716	53	5	3
18.1406	19.2401	43	4	3
18.225	19.3295	54	5	3
18.5625	19.6875	44	4	3

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
18.9	20.0455	56	5	3
18.9844	20.1349	45	4	3
19.2375	20.4034	57	5	3
19.4063	20.5824	46	4	3
19.575	20.7614	58	5	3
19.8281	21.0298	47	4	3
19.9125	21.1193	59	5	3
20.25	N/A	48	4	3
20.5875	N/A	61	5	3
20.6719	N/A	49	4	3
20.925	N/A	62	5	3
21.0938	N/A	50	4	3
N/A	21.4773	30	5	2
N/A	21.8352	61	10	2
N/A	21.875	55	9	2
N/A	21.9247	49	8	2
N/A	21.9886	43	7	2
N/A	22.0739	37	6	2
N/A	22.1932	31	5	2
N/A	22.2727	56	9	2
N/A	22.3722	25	4	2
N/A	22.5	44	7	2
21.2625	22.5511	63	10	2
21.375	22.6705	38	6	2
21.5156	22.8196	51	8	2
21.6	22.9091	32	5	2
21.6964	23.0114	45	7	2
21.75	23.0682	58	9	2
21.9375	23.267	26	4	2
22.125	23.4659	59	9	2
22.1786	23.5227	46	7	2

Table 26. GPCLK PLL Programming Table*(3 of 7)*

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
22.275	23.625	33	5	2
22.3594	23.7145	53	8	2
22.5	23.8636	40	6	2
22.6607	24.0341	47	7	2
22.7813	24.1619	27	4	2
22.875	24.2614	61	9	2
22.95	24.3409	34	5	2
23.0625	24.4602	41	6	2
23.1429	24.5455	48	7	2
23.2031	24.6094	55	8	2
23.25	24.6591	62	9	2
23.625	25.0568	28	4	2
24.0469	25.5043	57	8	2
24.1071	25.5682	50	7	2
24.1875	25.6534	43	6	2
24.3	25.7727	36	5	2
24.4688	25.9517	29	4	2
24.5893	26.0795	51	7	2
24.75	26.25	44	6	2
24.8906	26.3991	59	8	2
24.975	26.4886	37	5	2
25.0714	26.5909	52	7	2
25.3125	26.8466	30	4	2
25.5536	27.1023	53	7	2
25.65	27.2045	38	5	2
25.7344	27.294	61	8	2
25.875	27.4432	46	6	2
26.0357	27.6136	54	7	2
26.1563	27.7415	31	4	2
26.325	27.9205	39	5	2
26.4375	28.0398	47	6	2

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
26.5179	28.125	55	7	2
26.5781	28.1889	63	8	2
27	28.6364	32	4	2
27.4821	29.1477	57	7	2
27.5625	29.233	49	6	2
27.675	29.3523	41	5	2
27.8438	29.5312	33	4	2
27.9643	29.6591	58	7	2
28.125	29.8295	50	6	2
28.35	30.0682	42	5	2
28.4464	30.1705	59	7	2
28.6875	30.4261	34	4	2
28.9286	30.6818	60	7	2
29.025	30.7841	43	5	2
29.25	31.0227	52	6	2
29.4107	31.1932	61	7	2
29.5313	31.321	35	4	2
29.7	31.5	44	5	2
29.8125	31.6193	53	6	2
29.8929	31.7045	62	7	2
30.375	32.2159	36	4	2
30.9375	32.8125	55	6	2
31.05	32.9318	46	5	2
31.2188	33.1108	37	4	2
31.5	33.4091	56	6	2
31.725	33.6477	47	5	2
32.0625	34.0057	38	4	2
32.4	34.3636	48	5	2
32.625	34.6023	58	6	2
32.9063	34.9006	39	4	2
33.075	35.0795	49	5	2

Table 26. GPCLK PLL Programming Table*(4 of 7)*

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
33.1875	35.1989	59	6	2
33.75	35.7955	40	4	2
34.3125	36.392	61	6	2
34.425	36.5114	51	5	2
34.5938	36.6903	41	4	2
34.875	36.9886	62	6	2
35.1	37.2273	52	5	2
35.4375	37.5852	42	4	2
35.775	37.9432	53	5	2
36.2813	38.4801	43	4	2
36.45	38.6591	54	5	2
37.125	39.375	44	4	2
37.8	40.0909	56	5	2
37.9688	40.2699	45	4	2
38.475	40.8068	57	5	2
38.8125	41.1648	46	4	2
39.15	41.5227	58	5	2
39.6563	42.0597	47	4	2
39.825	42.2386	59	5	2
40.5	N/A	48	4	2
41.175	N/A	61	5	2
41.3438	N/A	49	4	2
41.85	N/A	62	5	2
42.1875	N/A	50	4	2
N/A	42.9545	30	5	1
N/A	43.6704	61	10	1
N/A	43.75	55	9	1
N/A	43.8494	49	8	1
N/A	43.9773	43	7	1
N/A	44.1477	37	6	1
N/A	44.3864	31	5	1

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
N/A	44.5454	56	9	1
N/A	44.7443	25	4	1
N/A	45	44	7	1
42.525	45.1023	63	10	1
42.75	45.3409	38	6	1
43.0313	45.6392	51	8	1
43.2	45.8182	32	5	1
43.3929	46.0227	45	7	1
43.5	46.1364	58	9	1
43.875	46.5341	26	4	1
44.25	46.9318	59	9	1
44.3571	47.0454	46	7	1
44.55	47.25	33	5	1
44.7188	47.429	53	8	1
45	47.7273	40	6	1
45.3214	48.0682	47	7	1
45.5625	48.3239	27	4	1
45.75	48.5227	61	9	1
45.9	48.6818	34	5	1
46.125	48.9204	41	6	1
46.2857	49.0909	48	7	1
46.4063	49.2187	55	8	1
46.5	49.3182	62	9	1
47.25	50.1136	28	4	1
48.0938	51.0085	57	8	1
48.2143	51.1364	50	7	1
48.375	51.3068	43	6	1
48.6	51.5454	36	5	1
48.9375	51.9034	29	4	1
49.1786	52.1591	51	7	1
49.5	52.5	44	6	1

Table 26. GPCLK PLL Programming Table*(5 of 7)*

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
49.7813	52.7983	59	8	1
49.95	52.9773	37	5	1
50.1429	53.1818	52	7	1
50.625	53.6932	30	4	1
51.1071	54.2045	53	7	1
51.3	54.4091	38	5	1
51.4688	54.5881	61	8	1
51.75	54.8864	46	6	1
52.0714	55.2273	54	7	1
52.3125	55.4829	31	4	1
52.65	55.8409	39	5	1
52.875	56.0795	47	6	1
53.0357	56.25	55	7	1
53.1563	56.3778	63	8	1
54	57.2727	32	4	1
54.9643	58.2954	57	7	1
55.125	58.4659	49	6	1
55.35	58.7045	41	5	1
55.6875	59.0625	33	4	1
55.9286	59.3182	58	7	1
56.25	59.6591	50	6	1
56.7	60.1364	42	5	1
56.8929	60.3409	59	7	1
57.375	60.8523	34	4	1
57.8571	61.3636	60	7	1
58.05	61.5682	43	5	1
58.5	62.0454	52	6	1
58.8214	62.3864	61	7	1
59.0625	62.642	35	4	1
59.4	63	44	5	1
59.625	63.2386	53	6	1

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
59.7857	63.4091	62	7	1
60.75	64.4318	36	4	1
61.875	65.625	55	6	1
62.1	65.8636	46	5	1
62.4375	66.2216	37	4	1
63	66.8182	56	6	1
63.45	67.2954	47	5	1
64.125	68.0114	38	4	1
64.8	68.7273	48	5	1
65.25	69.2045	58	6	1
65.8125	69.8011	39	4	1
66.15	70.1591	49	5	1
66.375	70.3977	59	6	1
67.5	71.5909	40	4	1
68.625	72.7841	61	6	1
68.85	73.0227	51	5	1
69.1875	73.3807	41	4	1
69.75	73.9773	62	6	1
70.2	74.4545	52	5	1
70.875	75.1704	42	4	1
71.55	75.8864	53	5	1
72.5625	76.9602	43	4	1
72.9	77.3182	54	5	1
74.25	78.75	44	4	1
75.6	80.1818	56	5	1
75.9375	80.5398	45	4	1
76.95	81.6136	57	5	1
77.625	82.3295	46	4	1
78.3	83.0454	58	5	1
79.3125	84.1193	47	4	1
79.65	84.4773	59	5	1

Table 26. GPCLK PLL Programming Table*(6 of 7)*

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
81	N/A	48	4	1
82.35	N/A	61	5	1
82.6875	N/A	49	4	1
83.7	N/A	62	5	1
84.375	N/A	50	4	1
N/A	85.9091	30	5	0
N/A	87.3409	61	10	0
N/A	87.5	55	9	0
N/A	87.6989	49	8	0
N/A	87.9545	43	7	0
N/A	88.2954	37	6	0
N/A	88.7727	31	5	0
N/A	89.0909	56	9	0
N/A	89.4886	25	4	0
N/A	90	44	7	0
85.05	90.2045	63	10	0
85.5	90.6818	38	6	0
86.0625	91.2784	51	8	0
86.4	91.6364	32	5	0
86.7857	92.0454	45	7	0
87	92.2727	58	9	0
87.75	93.0682	26	4	0
88.5	93.8636	59	9	0
88.7143	94.0909	46	7	0
89.1	94.5	33	5	0
89.4375	94.8579	53	8	0
90	95.4545	40	6	0
90.6429	96.1364	47	7	0
91.125	96.6477	27	4	0
91.5	97.0454	61	9	0
91.8	97.3636	34	5	0

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
92.25	97.8409	41	6	0
92.5714	98.1818	48	7	0
92.8125	98.4375	55	8	0
93	98.6364	62	9	0
94.5	100.2273	28	4	0
96.1875	102.017	57	8	0
96.4286	102.2727	50	7	0
96.75	102.6136	43	6	0
97.2	103.0909	36	5	0
97.875	103.8068	29	4	0
98.3571	104.3182	51	7	0
99	105	44	6	0
99.5625	105.5966	59	8	0
99.9	105.9545	37	5	0
100.2857	106.3636	52	7	0
101.25	107.3864	30	4	0
102.2143	108.4091	53	7	0
102.6	108.8182	38	5	0
102.9375	109.1761	61	8	0
103.5	109.7727	46	6	0
104.1429	110.4545	54	7	0
104.625	110.9659	31	4	0
105.3	111.6818	39	5	0
105.75	112.1591	47	6	0
106.0714	112.5	55	7	0
106.3125	112.7557	63	8	0
108	114.5454	32	4	0
109.9286	116.5909	57	7	0
110.25	116.9318	49	6	0
110.7	117.4091	41	5	0
111.375	118.125	33	4	0

Table 26. GPCLK PLL Programming Table*(7 of 7)*

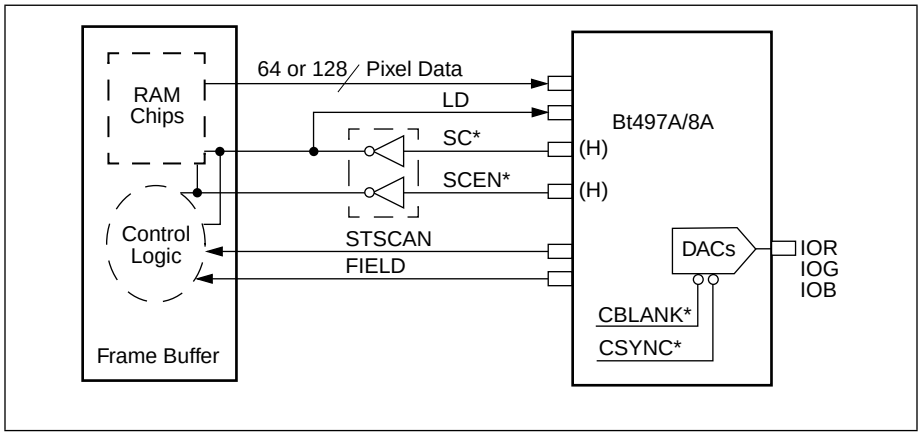
GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
111.8571	118.6363	58	7	0
112.5	119.3182	50	6	0
113.4	120.2727	42	5	0
113.7857	120.6818	59	7	0
114.75	121.7045	34	4	0
115.7143	122.7273	60	7	0
116.1	123.1363	43	5	0
117	124.0909	52	6	0
117.6429	124.7727	61	7	0

GPCLK Rate w/ Crystal =		M	N	L
13.50 MHz	**14.31818 MHz**			
118.125	125.2841	35	4	0
118.8	N/A	44	5	0
119.25	N/A	53	6	0
119.5714	N/A	62	7	0
121.5	N/A	36	4	0
123.7500	N/A	55	6	0
124.2000	N/A	46	5	0
124.8750	N/A	37	4	0

Guide To Frame Buffer Interface

This section clarifies the expected interaction of the Bt497A/8A with its associated frame buffer. Figure 37 illustrates the basic hookup. The frame buffer is simplified into its primary components with respect to the Bt497A/8A. The RAM chips are expected to be standard or specialized Video RAM (VRAM) components. The control logic handles the major addressing control of the RAM chips. As such, the control logic will likely interact with all four of the Bt497A/8A external CRT timing signals. In contrast to previous RAMDAC products from Rockwell, the Bt497A/8A has an on-chip CRT timing generator. Thus, the Bt497A/8A generates its own internal syncing and blanking controls for modulation of the analog RGB outputs, as shown in Figure 37. However, the frame buffer control logic needs some indication of expected timing events in relation to the displayed screen. The Bt497A/8A does provide a digital CSYNC* pin, but it is not expected to contribute to the task of latching the first pixels after BLANK de-assertion.

Figure 37. Frame Buffer Interface for Bt497A/8A-Generated VRAM Serial Clock and Pixel Clock



Control Signals

The following signals have been previously described in this datasheet. The definitions are repeated here with an emphasis on their frame buffer control aspect.

LD–The control input to the Bt497A/8A whose rising edge latches pixel data and internal CRT sync and blank states into the chip data path.

SC*–The Bt497A/8A serial clock output. This is the primary timing reference for all frame buffer control.

SCEN*–Serial Clock Enable (active low). This chip output, when active, tells the RAM chips to continuously output active video pixel data for potential display.

STSCAN–Start-Scan Enable (active high). This chip output alerts the frame buffer control logic, one horizontal retrace in advance, to prepare the next visible scan-line for display.

FIELD–Indicates which field is active for interlaced scanning. This pin is bidirectional in order to synchronize display systems with multiple Bt497A/8A chips. For single RAMDAC systems (and for this discussion) FIELD is an output.

Pixel Data–Represents the frame buffer data which is sent to the Bt497A/8A for display. A single stable occurrence of the pixel data is referred to as a "load group."

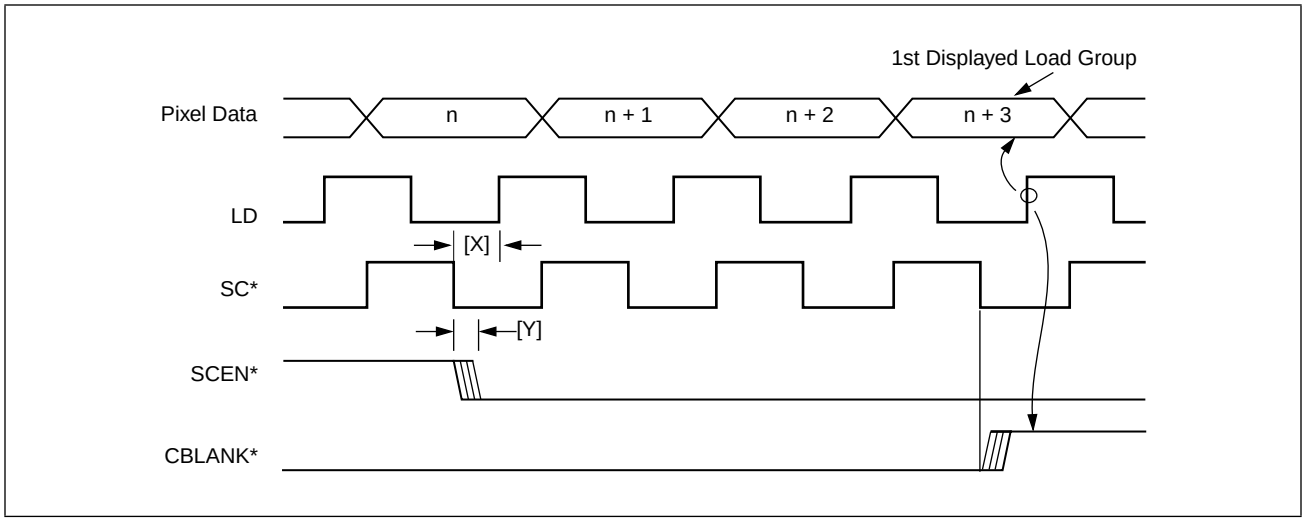
CBLANK*–Composite BLANK, active low. This signal, after pipeline delays, forces the chip DACs to their inactive level allowing the display monitor to perform retraces.

CSYNC*–Composite SYNC, active low. This signal, after pipeline delay, appears on the IOG signal as a special low-current level. It signals the monitor to execute a retrace.

The (H) beside the SC* and SCEN* in Figure 37 indicates that they are "High Drive" outputs, which are expected to be connected to multiple inverter buffers. These buffers are indicated as the single gates in Figure 37, and are required to drive the multiple RAM chips in a high-resolution frame buffer. STSCAN and FIELD are normal drive outputs, whose load in the control logic is expected to be modest.

LD is expected to be inverted from SC* and returned to the Bt497A/8A. In Figure 38, the inverter delay, shown as [X], is given by AC Timing #14. Further, the delay from SC* falling edge to the stable point of SCEN* is shown as [Y]. That value is Timing #13. (The same value applies as well to the delay for STSCAN and FIELD, from SC*.) Finally, the pixel data must be stable around the rising edge of LD at the Bt497A/8A. For corresponding timings see Input Pixel Timing in the AC Electrical and parameters section.

Figure 38. Latching of First Pixels After BLANK



Typical Usage

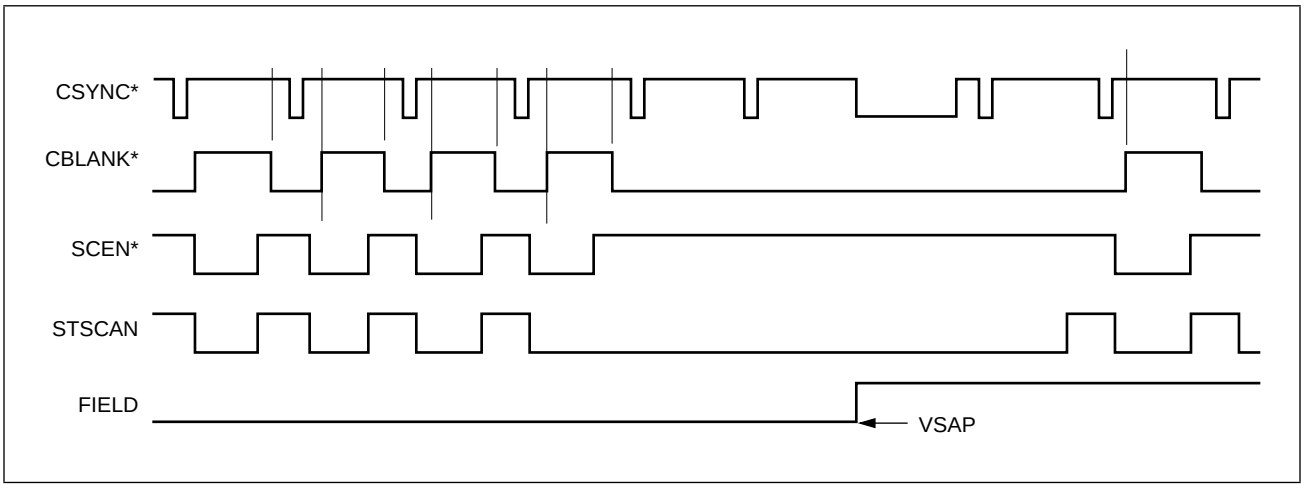
Figure 39 illustrates the above-mentioned signals as they might appear in a simple noninterlaced display system. The waveforms show the last four scan lines of a reference frame followed by a vertical retrace, then followed by the first scan line of the next frame. Note that for illustration purposes, the vertical retrace is greatly shortened from that of a true typical monitor. The SCEN* signal is controlled by programming the Horizontal SCEN Assertion Point (HSCENAP) and the Horizontal SCEN Negation Point (HSCENNP) registers. Program these registers so that the SCEN* edges precede the CBLANK* transitions, as shown in Figure 39.

The STSCAN signal is not controlled by any dedicated registers, as SCEN* is. Instead, STSCAN assertions are a function of two other timings: SCEN* and the separate horizontal and vertical components of CBLANK*, referred to as HBLANK* and VBLANK*, respectively. When STSCAN edges do occur, they are coincident with the values specified for SCEN*. The enable condition for STSCAN pulses is provided indirectly by VBLANK*. Essentially, the first STSCAN pulse of a frame coincides with the HBLANK* event that precedes the first displayed line. The last STSCAN of a frame coincides with the last HBLANK* just before the last displayed line.

The FIELD signal transitions at the point labeled VSAP. That point corresponds to the beginning of the vertical sync interval, and is triggered by the VSAP register value. For noninterlaced displays, the FIELD edges may alert the control logic that the Bt497A/8A is between frames, so the logic should anticipate the top of the screen for its next display sequence. And for interlaced displays, the level of FIELD indicates that, for FIELD = low, the next (or present) field of scan lines are even, while FIELD = high indicates that the odd field is pending (or present).

Depending on the design of the control logic, the STSCAN and FIELD signals may be all that are required as inputs to implement the CRT timing aspect of the logic. The SC* and SCEN* signals (post-buffered) will certainly connect to the RAM chips, but they may be optional as inputs to the control logic.

Figure 39. CRT Signals at Vertical Scale



Latching The First Pixels

A key question for any frame buffer design with the Bt497A/8A is, when to deliver the first pixels to be displayed immediately after the Horizontal Blank transitions to the active-display state. The previous descriptions dealt with the indications for the beginning of a screen from the slower vertical context of the first scan lines of a frame. Figure 38 illustrates how the Bt497A/8A handles the first displayable data that forms the beginning (leftmost, on the screen) pixels of every scan line in a frame. The corresponding pixel data occurrence is referred to as the "first-displayed load group."

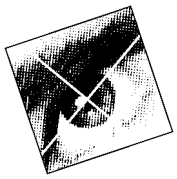
The falling edge of SCEN* is the direct trigger that tells the frame buffer to prepare to output the first load group. Associated with the SCEN* falling edge are the SC* falling edge that released it (SCEN*), and also the load group that is presently stable at that occurrence. That load group is labeled "n" in Figure 38. Typically a frame buffer will take a small number of SC* cycles to produce the first displayed load group after it has received the SCEN* assertion. The n+3 load group is intended for first-display. Thus, the SCEN* and CBLANK* (HBLANK* component) signals are programmed to exhibit a "frame buffer latency" delta of 3 serial clock periods. Note that when the SC* edge releases the CBLANK* rising edge, the next immediate LD rising edge is assumed to latch both the "Blank-is-Off" state and the corresponding first-displayed load group.

Programming Details

The SCEN* signal is controlled by the values in the HSCENAP and the HSCENNP registers. Furthermore, the Horizontal Blank component of CBLANK* is determined by the Horizontal Blank Negation Point (HBNP) and Horizontal Blank Assertion Point (HBAP) registers. Normally, users establish the blank and sync timing points first, based on their monitor, or desired screen characteristics. SCEN* is then set based on the frame buffer latency value. In Figure 38, this latency is 3 serial clock periods. Assuming that the HBLANK* transitions are fixed, the HSCENAP will be programmed to make SCEN* transition 3 serial clocks earlier than the CBLANK* rising edge.

Here it is necessary to mention that the three external control signals, SCEN*, STSCAN, and FIELD, have an extra SC*-based pipeline delay with respect to the internal controls: CBLANK* and CSYNC*. This extra pipeline ensures that the external signals are closely synchronized to the SC* clock output. However, it necessitates an adjustment in programming the SCEN* registers. To achieve the 3-cycle frame buffer latency of the example, the HSCENAP register should be programmed to be 4 less than the HBNP value. In general, if the actual frame buffer latency is 'X' number of serial clock periods, then the programmed delta for the SCEN* registers is X+1 periods less than the corresponding HBLANK* value. The effect for HSCENAP has been described: the same X+1 delta would be seen between the HSCENNP and HBAP values.

The STSCAN and FIELD signals are not timing-critical in the sense that SCEN* is. Therefore, there is no need or concern for programming adjustments to these two signals.



PARAMETRIC INFORMATION

DC Electrical Parameters

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 27. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply, 3.3 V, ± 5%	VAA3	3.14	3.3	3.47	V
Power Supply, 5.0 V, ± 5%	VAA5	4.75	5.0	5.25	V
Ambient Operating Temperature	T_a	0	25	70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.2	1.235	1.26	V
FSADJ Resistor	RSET		140		Ω
Junction Temperature @ 100 LFPM Airflow	T_{jmax}			125	°C
SDA, SCL Pullup Resistor (1)	Rps		1000		Ω
Drawings Pullup Resistor (1)	Rpd		1000		Ω
Notes: (1). Pullup resistors must be terminated at +5 V supply.					

Table 28. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA3 (measured to GND)				5	V
VAA5 (measured to GND)				7	V
Voltage on any Signal Pin (1)		GND –0.5		VAA+0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC	0	Indefinite		

Table 28. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Storage Temperature	TS	–65		+125	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature (5 seconds, 1/4” from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C
SDL, SDA Pullup Resistor(2)	Rps	600			W
Drawing b Pullup Resistor(2)	Rpd	120			W

Notes: (1). This device employs a high-impedance CMOS device on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.
(2). Pullup resistors must be terminated at +5 V supply.

Table 29. DC Characteristics *(1 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs Resolution (each DAC) Accuracy (each DAC) Integral Linearity Error Differential Linearity Error Gray-Scale Error Monotonicity Coding	 IL DL 	 8 	 8 Guaranteed 	 8 ±1 ±1 ±5 	 Bits LSB LSB % Gray Scale Binary
Digital Inputs (except CLOCK and CLOCK*)					
Input High Voltage (non Field)	VIH	2		VAA3 + 0.5	V
Input High Voltage (Field pin)	VIH	2		VAA5 + 0.5	V
Input Low Voltage	VIL	GND		0.8	V
Hysteresis (Field pin)	Vhys		0.3		V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Digital Inputs with Internal Pullups (Pixel Inputs and JTAG Pins)					
Input High Voltage	VIH	2		VAA3 + 0.5	V
Input Low Voltage	VIL	GND		0.8	V
Input High Current (Vin = 2.4 V)	IIH			60	µA
Input Low Current (Vin = 0.4 V)	IIL			–60	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Pixel Clock Inputs (CLOCK and CLOCK*)					
Differential Input Voltage	ΔVIN	0.6			V
Input High Voltage	VKIH	4		VAA5 + 0.5	V
Input Low Voltage	VKIL	GND –0.5		3.4	V
Input High Current (Vin = 4.0 V)	IKIH			5	µA
Input Low Current (Vin = 0.4 V)	IKIL			–5	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		7		pF
Open Drain Pins (SDA, SCL, DRAWING*)					
Input High Voltage	VIH	3.0		VAA5 + 0.5	V
Input Low Voltage	VIL	-0.5		1.5	V
Hysteresis	Vhys		0.3		V
Input Current	Ii	-30		30	µA

Table 29. DC Characteristics *(2 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
Output Low Voltage (Iol = 40 mA Drawing* pin)	Vol			0.4	V
Output Low Voltage (Iol = 8 mA SDL, SDA pin)	Vol			0.4	V
Capacitance	Ci		7	10	pF
Digital Outputs (D[7:0], FIELD, STSCAN, TDO, CSYNC*, VSYNC*)					
Output High Voltage (Ioh = –6.4 mA, non Field)	Voh	2.4		VAA3	V
Output Low Voltage (Iol = 6.4 mA, non Field)	Vol	GND		0.4	V
Output High Voltage (Ioh = –20 mA, Field pin)	Voh	2.4		VAA3	V
Output Low Voltage (Iol = 20 mA, Field pin)	Vol	GND		0.4	V
Three-state Current	Ioz			10	µA
Load Capacitance*(1)*	Co			20	pF
Digital Outputs (SC*, SCEN*, GPCLK)					
Output High Current (Voh = 2.4 V)	Ioh			-16	mA
Output Low Current (Vol = 0.4 V)	Iol			12	mA
Load Capacitance (SC*, SCEN*)*(1)*	Co			30	pF
Load Capacitance (GPCLK)*(1)*	Co			10	pF
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.40		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		100		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		%/% VAA

Notes: (1). Includes board wiring and capacitance at buffer input.

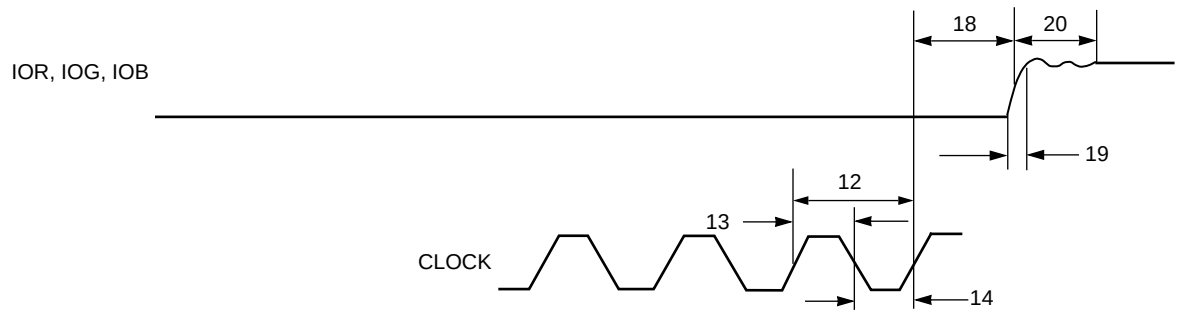
AC Electrical Parameters

Table 30. Analog Output Timing

Parameter	Symbol	160 **MHz Devices (Bt497A)**			**240 MHz Devices (Bt498A)**			Units
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Analog Output Delay (1)			20			20		ns
Analog Output Rise/Fall			1.5			1.5		ns
Analog Output Settling (2)			3.5			3.5		ns
Clock/Data Feedthrough (3)			–28			–28		dB
Glitch Impulse (4)			50			50		pV–sec
Analog Output Skew (5)			0	1		0	1	ns
Pipeline Delay				17			17	Clocks
VAA Supply Current								
IAA3 (6)				TBD			TBD	mA
IAA5 (6)				TBD			TBD	mA
IAA3 (7)				TBD			TBD	mA
IAA5 (7)				TBD			TBD	mA
IAA3 (8)			TBD			TBD		mA
IAA5 (8)			TBD			TBD		mA

Notes: (1). Referenced to ECL clock inputs.
(2). Output settling time measured from 50% point of full-scale transition to output settling within ±1 LSB.
(3). Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74 HC logic. Settling time does not include clock and data feedthrough.
(4). Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.
(5). Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.
(6). VAA3 = 3.47 V, VAA5 = 5.25 V, 0°C, at maximum frequency specified. Pixel pattern alternates one full white pixel (logical ones) and one full black pixel (logical zeros).
(7). VAA3 = 3.47 V, VAA5 = 5.25 V, 70°C, at maximum frequency specified. Pixel pattern alternates four full white pixels (logical ones) and four full black pixels (logical zeros).
(8). VAA3 = 3.30 V, VAA5 = 5.00 V, 25°C, at maximum frequency specified. Pixel pattern alternates four full white pixels (logical ones) and four full black pixels (logical zeros).
9. Worst case pixel patterns may require additional air flow to maintain the junction temperature within its recommended operating limits.
10. Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 140 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. ECL input values are VAA5 – 0.8 to VAA5 – 1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D[7:0] output load ≤ 75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Figure 40. Video Output Timing



Notes: 1. Output delay time is measured from the 50% point of the rising clock edge to the 50% point of full-scale transition.
2. Output settling time is measured from the 50% point of full-scale transition to output settling within ±1 LSB for the Bt497A/8A.
3. Output rise/fall time is measured between the 10% and 90% points of full-scale transition.

Table 31. PLL Clock Generation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Crystal/Oscillator Frequency		10	14.318	24	MHz
Pixel PLL VCO Multiplicand	M_P	24		80	
Pixel PLL VCO Divisor	N_P	4		12	
Pixel PLL M/N Generated Pixel Clock Rate		60		240	MHz
GPCLK PLL VCO Multiplicand	M_G	21		63	
GPCLK PLL VCO Divisor	N_G	4		15	
GPCLK M/N Generated Clock Rate		11		120	MHz
Both PLL M/N Generated Clock Accuracy			99		%
Both PLL M/N Generated Clock Jitter			200		ps
RESET* Active Pulse Width		10			ns
CE* Rise to New SC*/Pixel Clock Rate or GPCLK Rate			3.75		ms

Note: Parameters apply to predivided (i.e., before applying 1/L) pixel clock generation. For frequencies below 100 MHz, it is recommended that $L \geq 2$.

Table 32. MPU Port Timing

Parameter	Symbol	160 **MHz Devices (Bt497A)**			**240 MHz Devices (Bt498A)**			Units
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
R/W, C0, C1, LB* Setup	1	0			0			ns
R/W, C0, C1, LB* Hold	2	15			15			ns
CE* Low Time	4	55			55			ns
CE* High Time	5	25			25			ns
CE* ↓ to Data Driven	6	7			7			ns
CE* ↓ to Data Valid	7			55			55	ns
CE* ↑ to Data Three-stated	8			19			19	ns
Write Data Setup Time	9	10			10			ns
Write Data Hold Time	10	5			5			ns

Figure 41. MPU Read/Write Timing

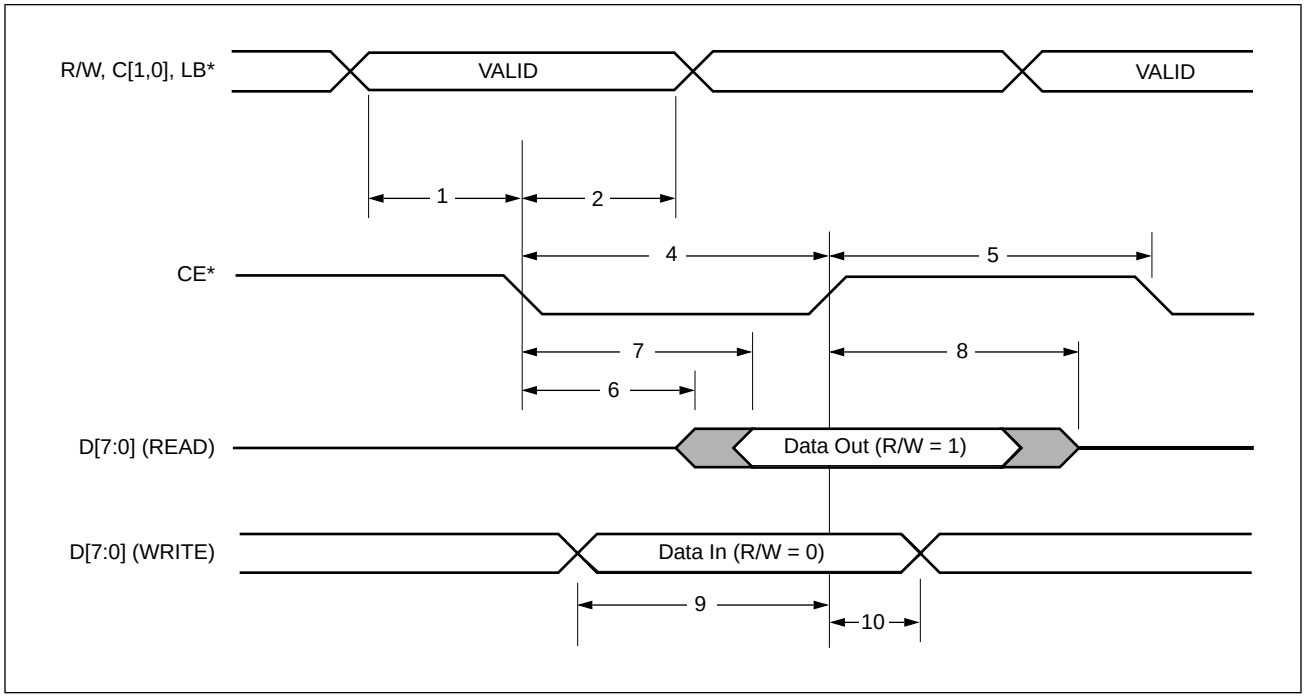


Table 33. Serial Clock Timing

Parameter	Symbol	160 MHz Devices (Bt497A)			240 MHz Devices (Bt498A)			Units
		Min	Typ	Max	Min	Typ	Max	
SC* Cycle Time	11							
2:1 and 4/2:1 formats		12.5			12.5			ns
4:1 and 8/2:1 formats		N/A	N/A	N/A	16.7			ns
SC* Pulse High Duty Cycle	12	45	50	55	45	50	55	%
SC* to SCEN*/STSCAN/FIELD	13	0		5	0		5	ns

Note: SC* duty cycle measured at Vth = 1.65 V, at Co ≤ 30 pF.

Table 34. Pixel and LD Timing

Parameter	Symbol	160 MHz Devices (Bt497A)			240 MHz Devices (Bt498A)			Units
		Min	Typ	Max	Min	Typ	Max	
SC* to LD Delay	14	1		8	1		8	ns
Pixel and Control Setup	15	3			3			ns
Pixel and Control Hold	16	2			2			ns
LD Cycle Time	17							
2:1 and 4/2:1 formats		12.5			12.5			ns
4:1 and 8/2:1 formats					16.7			ns
LD Pulse Width (high or low)								
2:1 and 4/2:1 formats	18	5.7			5.7			ns
4:1 and 8/2:1 formats					7.6			ns

Figure 42. Input Pixel Timing

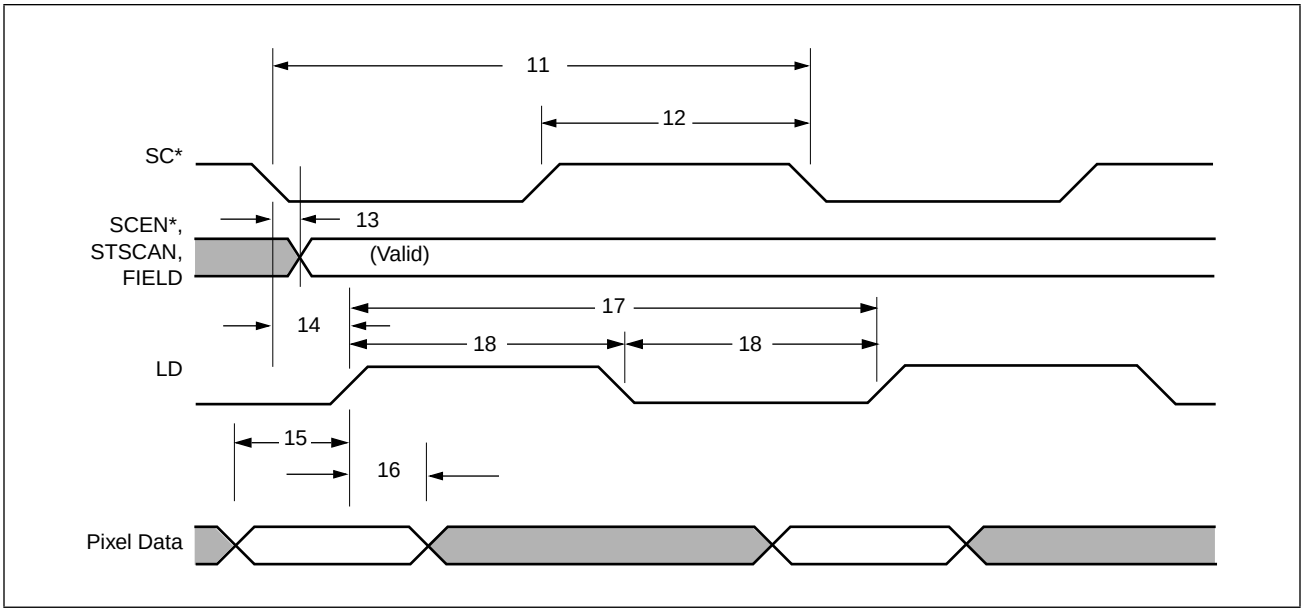


Table 35. JTAG Timing

Parameter	Symbol	160 MHz Devices (Bt497A)			240 MHz Devices (Bt498A)			Units
		Min	Typ	Max	Min	Typ	Max	
TMS, TDI Setup Time	19	8			8			ns
TMS, TDI Hold Time	20	6			6			ns
TCK Low Time	21	20			20			ns
TCK High Time	22	20			20			ns
TCK Asserted to TDO Driven	23	1			1			ns
TCK Asserted to TDO Valid	24			20			20	ns
TCK Negated to TDO three-stated	25			20			20	ns

Figure 43. JTAG Timing

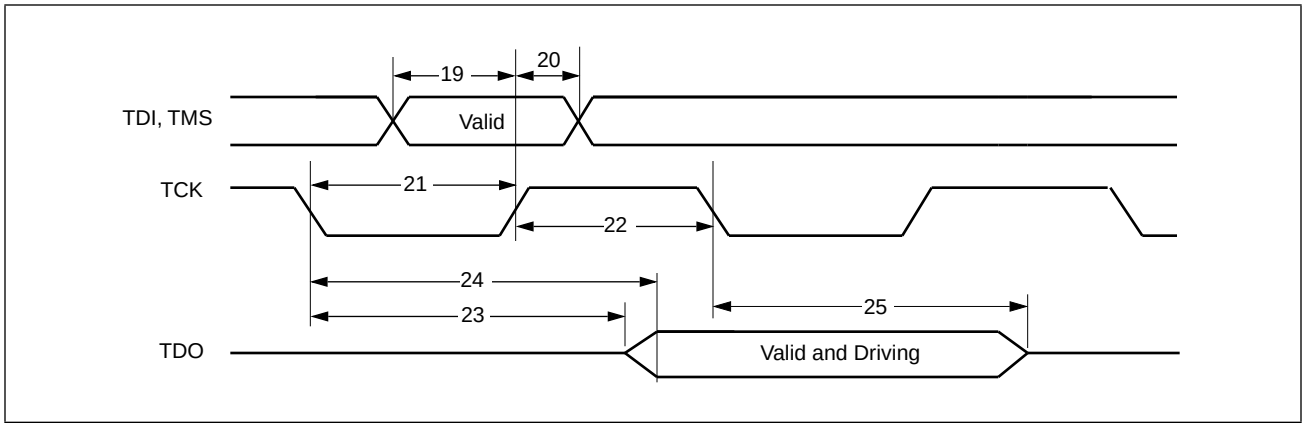
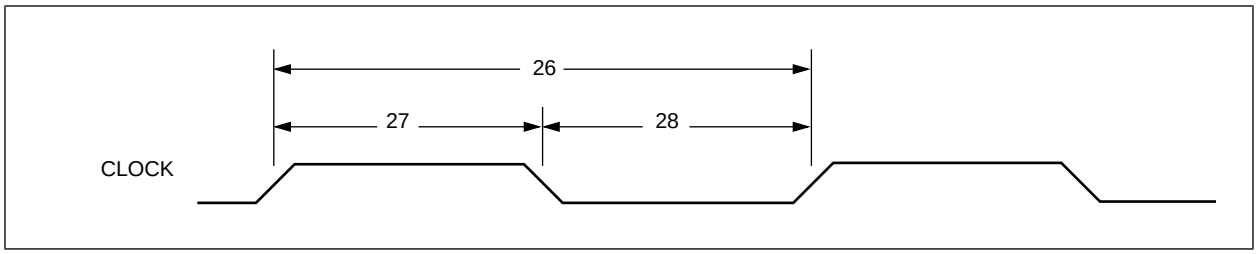


Table 36. Input Clock

Parameter	Symbol	160 MHz Devices (Bt497A)			240 MHz Devices (Bt498A)			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			160			240	MHz
Clock Cycle Time	26			6.25			4.167 ns	ns
Clock Pulse Width High	27	2.8			2			ns
Clock Pulse Width Low	28	2.8			2			ns

Figure 44. ECL Clock Input (PLL Bypassed)

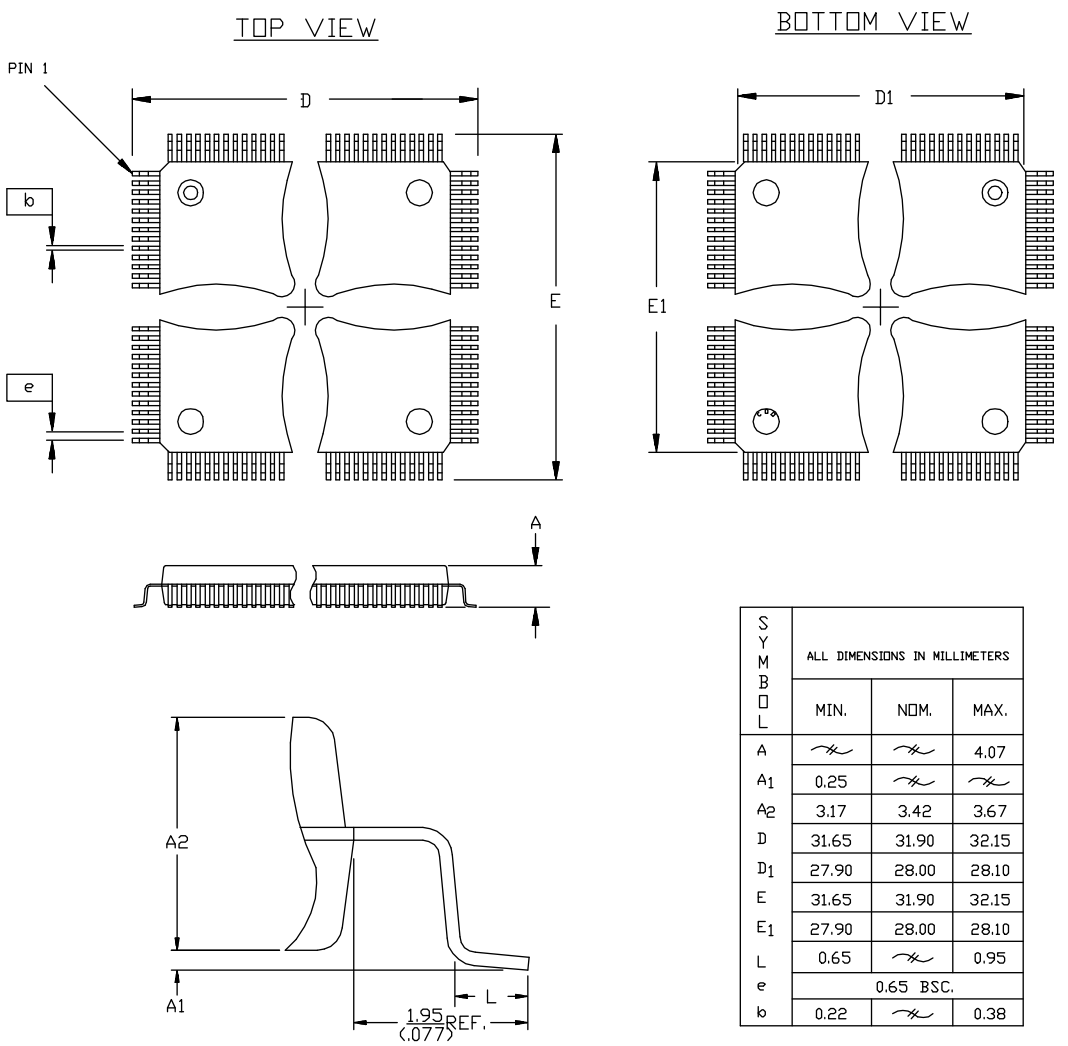


Package Information

Table 37. Package Thermal Resistance

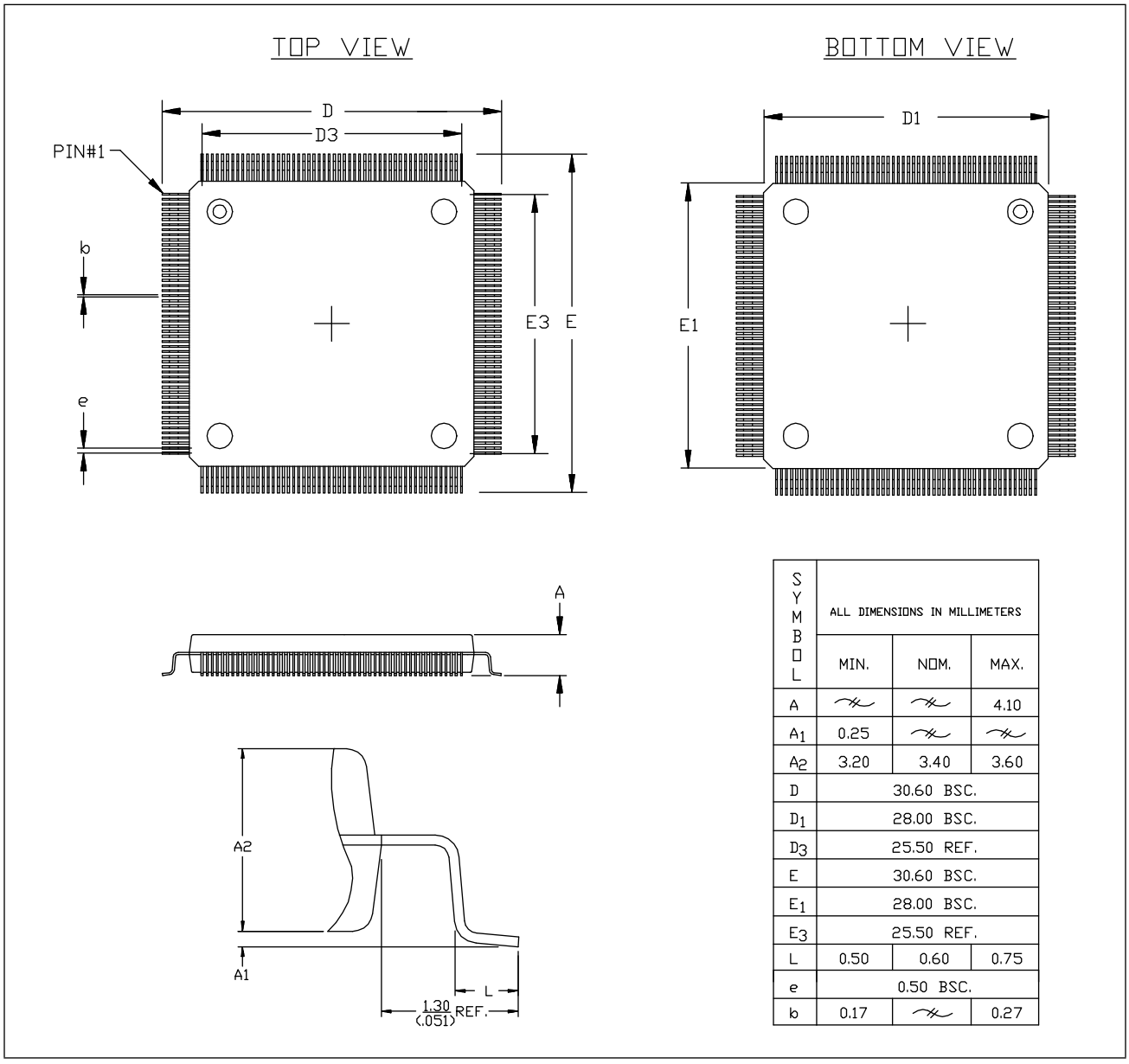
Package	Airflow (Linear Feet Per Minute)					Units
	0	50	100	200	400	
160-Pin Quad Flat Pack	21	19	17	16	14	°C/W
208-Pin Quad Flat Pack	22	20	18	16	14	°C/W

Figure 45. 160-Pin Metric Quad Flatpack (MQFP)



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A			4.07
A_1	0.25		
A_2	3.17	3.42	3.67
D	31.65	31.90	32.15
D_1	27.90	28.00	28.10
E	31.65	31.90	32.15
E_1	27.90	28.00	28.10
L	0.65		0.95
e	0.65 BSC.		
b	0.22		0.38

Figure 46. 208-Pin Metric Quad Flatpack (MQFP)



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A			4.10
A_1	0.25		
A_2	3.20	3.40	3.60
D		30.60 BSC.	
D_1		28.00 BSC.	
D_3		25.50 REF.	
E		30.60 BSC.	
E_1		28.00 BSC.	
E_3		25.50 REF.	
L	0.50	0.60	0.75
e		0.50 BSC.	
b	0.17		0.27

Revision History

Revision	Comments
A	Initial Release.