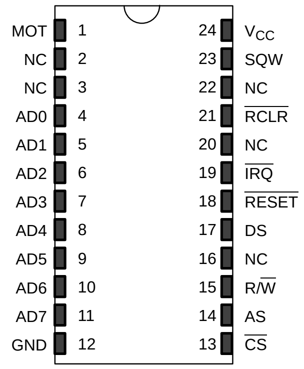
DALLAS SEMICONDUCTOR

DS12887A
Real Time Clock

FEATURES

- Drop–in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818B and DS1287A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self–contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation valid up to 2100
- Binary or BCD representation of time, calendar, and alarm
- 12– or 24–hour clock with AM and PM in 12–hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
  - 14 bytes of clock and control registers
  - 114 bytes of general purpose RAM
- Programmable square wave output signal
- Bus–compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software–maskable and testable
  - Time–of–day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle

PIN ASSIGNMENT



24–PIN ENCAPSULATED PACKAGE

PIN DESCRIPTION

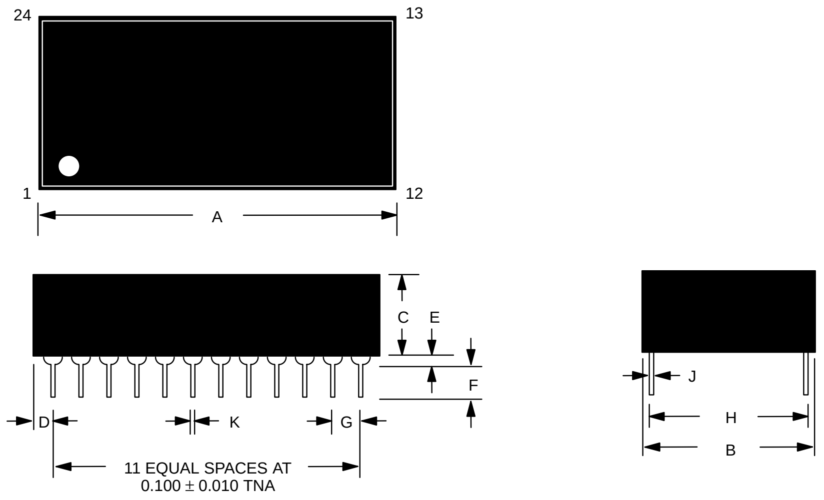
AD0–AD7	–	Multiplexed Address/Data Bus
NC	–	No Connection
MOT	–	Bus Type Selection
$\overline{CS}$	–	Chip Select
AS	–	Address Strobe
R/$\overline{W}$	–	Read/Write Input
DS	–	Data Strobe
$\overline{RESET}$	–	Reset Input
$\overline{IRQ}$	–	Interrupt Request Output
SQW	–	Square Wave Output
V_{CC}	–	+5 Volt Supply
$\overline{RCLR}$	–	RAM Clear
GND	–	Ground

DESCRIPTION

The DS12887A Real Time Clock plus RAM is designed to be a direct replacement for the DS1287A. The DS12887A is identical in form, fit, and function to the DS1287A, and has an additional 64 bytes of general purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. The $\overline{RCLR}$ pin is used to clear (set to logic 1) all 114 bytes of general purpose RAM but does not affect the RAM associated with the real time clock. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic "0" (–0.3 to +0.8 volts) during battery back–up mode when V_{CC} is not applied. The $\overline{RCLR}$ function is designed to be used via human interface (shorting to ground manually or by switch) and not to be driven with external buffers. All other operation, description and specification is identical to the DS12887.

DESCRIPTION

DS12887A REAL TIME CLOCK PLUS RAM



PKG	24–PIN	
DIM	**MIN**	**MAX**
A IN. MM	1.320 33.53	1.335 33.91
B IN. MM	0.675 17.15	0.700 17.78
C IN. MM	0.345 8.76	0.370 9.40
D IN. MM	0.100 2.54	0.130 3.30
E IN. MM	0.015 0.38	0.030 0.76
F IN. MM	0.110 2.79	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.590 14.99	0.630 16.00
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

NOTE: PINS 2, 3, 16, 20 AND 22 ARE MISSING BY DESIGN.

NOTE: THIS DEVICE CANNOT BE STORED OR SHIPPED IN CONDUCTIVE MATERIAL WHICH WILL GIVE A CONTINUITY PATH BETWEEN THE RAM CLEAR PIN AND GROUND.