Preliminary

4M/8M x 36 ECC-on-SIMM w/ Error Lines

Features

- 72-Pin JEDEC-Standard Single In-Line Memory Module
- Performance:

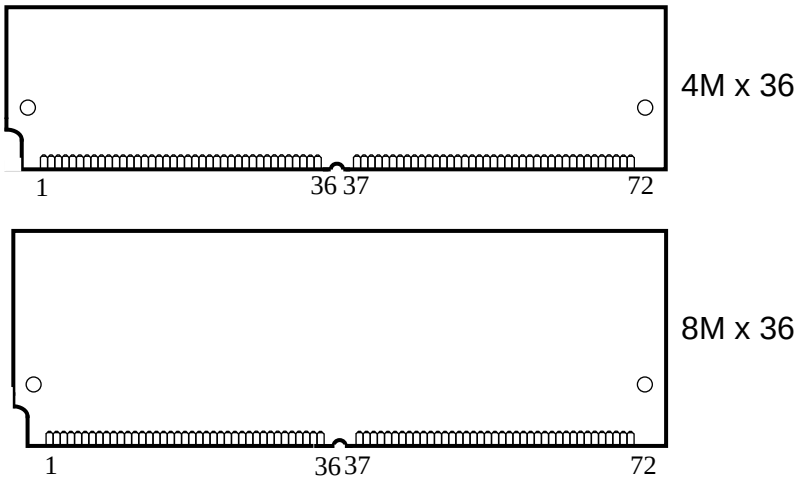
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{AA}	Access Time From Address	35ns
t_{RC}	Cycle Time	130ns
t_{PC}	Fast Page Mode Cycle Time	45ns

- Single-error-correct (SEC) high-speed ECC algorithm
- Single 5.0V ± 0.25V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/11 Addressing (Row/Column)
- Provides ECC and retrofits to standard x36 socket
- Au and Sn/Pb versions available
- Error indicator signals for each byte of data

Description

The IBM11D4490B/IBM11D8490B are 16MB/32MB industry standard 72-pin 4-byte single in-line memory modules (SIMM) that have fully functional, retrofittable and plug-compatible on-board error-correcting-code (ECC). The ECC function is completely self-contained and transparent to the system. The module is manufactured with 4 ECC ASICs and either 12 4M x 4 DRAMs (16MB) or 24 4M x 4 DRAMS (32MB) in SOJ packages. A unique assembly with 6 4M x 4 DRAMs in TSOP and 18 4M x 4 DRAMs in SOJ packages (32MB) is also available. The ECC-on-SIMM module corrects single-bit errors that may occur in any byte of SIMM data. It is recommended for systems that run critical applications but do not have native ECC. This family of SIMMs (4M x 36 and 8M x 36) provides the memory reliability required by these applications with no performance penalty. An error line is activated whenever a single-bit error is being corrected during a read cycle, or whenever a multi-bit uncorrectable error is detected.

Card Outline



Pin Description

$\overline{RAS}0$, $\overline{RAS}2$	Row Address Strobe (16MB)
$\overline{RAS}0$ - $\overline{RAS}3$	Row Address Strobe (32MB)
$\overline{CAS}0$ - $\overline{CAS}3$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
$\overline{ERROR}0$ - $\overline{ERROR}3$	Error Lines
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	25	DQ24	49	DQ9
2	DQ0	26	DQ7	50	DQ27
3	DQ18	27	DQ25	51	DQ10
4	DQ1	28	A7	52	DQ28
5	DQ19	29	$\overline{ERROR}0$	53	DQ11
6	DQ2	30	V_{CC}	54	DQ29
7	DQ20	31	A8	55	DQ12
8	DQ3	32	A9	56	DQ30
9	DQ21	33	$\overline{RAS}3$ (1)	57	DQ13
10	V_{CC}	34	$\overline{RAS}2$	58	DQ31
11	NC	35	PQ26	59	V_{CC}
12	A0	36	PQ8	60	DQ32
13	A1	37	PQ17	61	DQ14
14	A2	38	PQ35	62	DQ33
15	A3	39	V_{SS}	63	DQ15
16	A4	40	$\overline{CAS}0$	64	DQ34
17	A5	41	$\overline{CAS}2$	65	DQ16
18	A6	42	$\overline{CAS}3$	66	$\overline{ERROR}2$
19	A10	43	$\overline{CAS}1$	67	PD1
20	DQ4	44	$\overline{RAS}0$	68	PD2
21	DQ22	45	$\overline{RAS}1$ (1)	69	PD3
22	DQ5	46	$\overline{ERROR}1$	70	PD4
23	DQ23	47	$\overline{WE}$	71	$\overline{ERROR}3$
24	DQ6	48	NC	72	V_{SS}

1 - RAS1 and RAS3 are “NC” on 16MB SIMM

Ordering Information

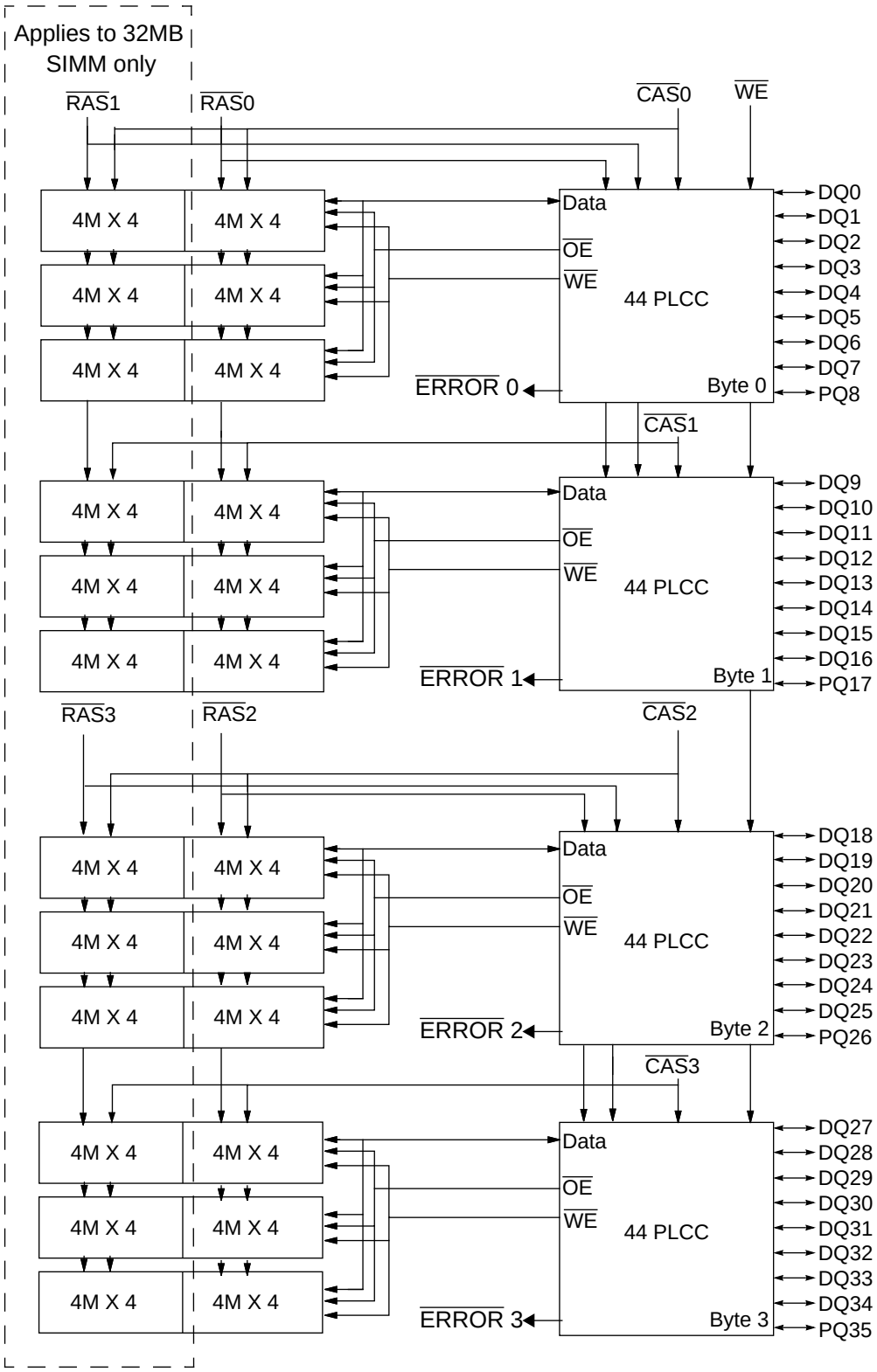
Part Number	Organization	Speed	Addr.	Leads	Dimensions	DRAM-Package	Notes
IBM11D4490BB-70	4M x 36	70ns	11/11	Sn/Pb	4.25” x 1.04” x .397”	SOJ	1
IBM11E4490BB-70				Au			
IBM11D4490BD-70				Sn/Pb			
IBM11E4490BD-70				Au			
IBM11D8490BD-70	8M x 36			Sn/Pb	4.25” x 1.40” x .397”	SOJ	1
IBM11E8490BD-70				Au		TSOP/SOJ	1, 2

Ordering Information

Part Number	Organization	Speed	Addr.	Leads	Dimensions	DRAM-Package	Notes

1. DRAM package designator appended to speed portion of partnumber on assemblies beginning with DRAM die rev E.
2. This assembly consists of 6 TSOP and 18 SOJ DRAMs

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	Error Line	All DQ, PQ bits	Notes
Standby	H	X	X	X	X		High Impedance	
Read	L	L	H	Row	Col		Valid Data Out	
Early-Write	L	L	L	Row	Col		Valid Data In	
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col		Valid Data Out	
Subsequent Cycles	L	H→L	H	N/A	Col		Valid Data Out	
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col		Valid Data In	
Subsequent Cycles	L	H→L	L	N/A	Col		Valid Data In	
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A		High Impedance	
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X		High Impedance	
Error during Read	X	L	H	X	X	L	Data Out	1
Error during Write	X	L	L	X	X	L	Data In	2

1. If all PQ's are valid, ECC has successfully corrected single bit error, DQ contains Valid Data Out. If a PQ is invalid, ECC has detected a multi-bit error, DQ's for the corresponding byte contain invalid Data Out.
2. A parity error has been detected on data received from system. A subsequent read of this data will indicate a parity error (PQ invalid). The operation of the error line during a write has not been characterized.

Presence Detect

Pin	4Mx36 (Industry Standard -70)	8Mx36 (Industry Standard -70)	Notes
PD1	V_{ss}	NC	1
PD2	NC	V_{ss}	1
PD3	V_{SS}	V_{SS}	1
PD4	NC	NC	1

1. NC= OPEN, V_{SS} = GND.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.3 to 6.5	V	1
V_{IN}	Input Voltage	-0.3 to V_{CC} + 0.3	V	1
V_{OUT}	Output Voltage	-0.3 to V_{CC} + 0.3	V	1
T_C	Operating Temperature (Case)	0 to +65	°C	1
T_{STG}	Storage Temperature	-40 to +125	°C	1
P_D	Power Dissipation	24	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_C = 0 to 65°C)

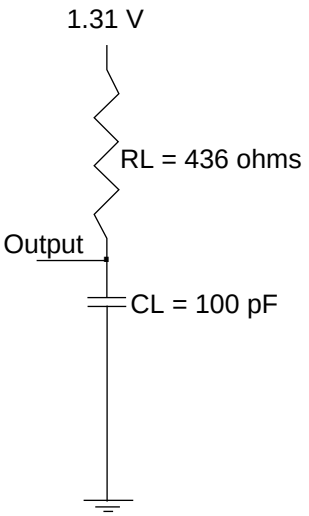
Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

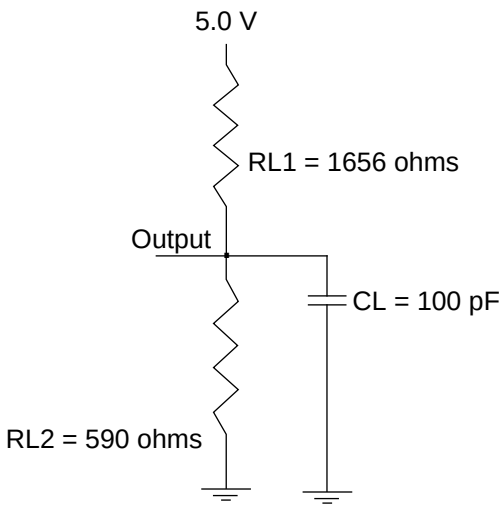
Capacitance (T_C = 0 to +65°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter	4M x 36 Max	8M x 36 Max	Units
C_{I1}	Input Capacitance (A0-A10)	100	161	pF
C_{I2}	Input Capacitance ($\overline{RAS}$)	70	70	pF
C_{I3}	Input Capacitance ($\overline{CAS}$)	50	70	pF
C_{I4}	Input Capacitance ($\overline{WE}$)	35	35	pF
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	12	12	pF
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	12	12	pF
$C_{I/O3}$	Output Capacitance ($\overline{ERROR}$0 - $\overline{ERROR}$3)	12	12	pF

Load Diagram



Load Circuit



Alternate Load Circuit

DC Electrical Characteristics (Tc = 0 to +65°C, V_{CC} = 5.0 ± 0.25V)

Symbol	Parameter		4M x 36 Min	4M x 36 Max	8M x 36 Min	8M x 36 Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-70	—	1080	—	1104	mA	1, 2, 3
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	—	48	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-70	—	1080	—	1104	mA	1, 3, 4
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-70	—	960	—	984	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	12	—	24	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-70	—	1080	—	1104	mA	1, 3, 4
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-460	+460	-460	+460	µA	
		$\overline{CAS}$, $\overline{WE}$	-40	+40	-70	+70		
		Address	-120	+120	-240	+240		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -4mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. When refreshing both banks at once, the refresh current becomes 2160mA.

AC Characteristics (T_C = 0 to +65°C, V_{CC} = 5.0 ± 0.25V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 500ms is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-70		Units
		Min	Max	
t_{WCS}	Write Command Set Up Time	0	—	ns
t_{WCH}	Write Command Hold Time	15	—	ns
t_{WP}	Write Command Pulse Width	15	—	ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	ns
t_{DS}	D_{IN} Setup Time	0	—	ns
t_{DH}	D_{IN} Hold Time	20	—	ns

Read Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	45	ns	1, 2

1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Read Error-Line Functionality Cycle

Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{ERR}	Error access time from $\overline{CAS}$	—	20	ns	1, 2
t_{ECH}	Error Output Hold/Hi-Z	3	20	ns	
t_{ECLZ}	$\overline{CAS}$ to Error Output in Low-Z	0	—	ns	
t_{ERCS}	Error Read Command Setup Time	0	—	ns	
t_{ERCH}	Error Read Command Hold Time	3	—	ns	

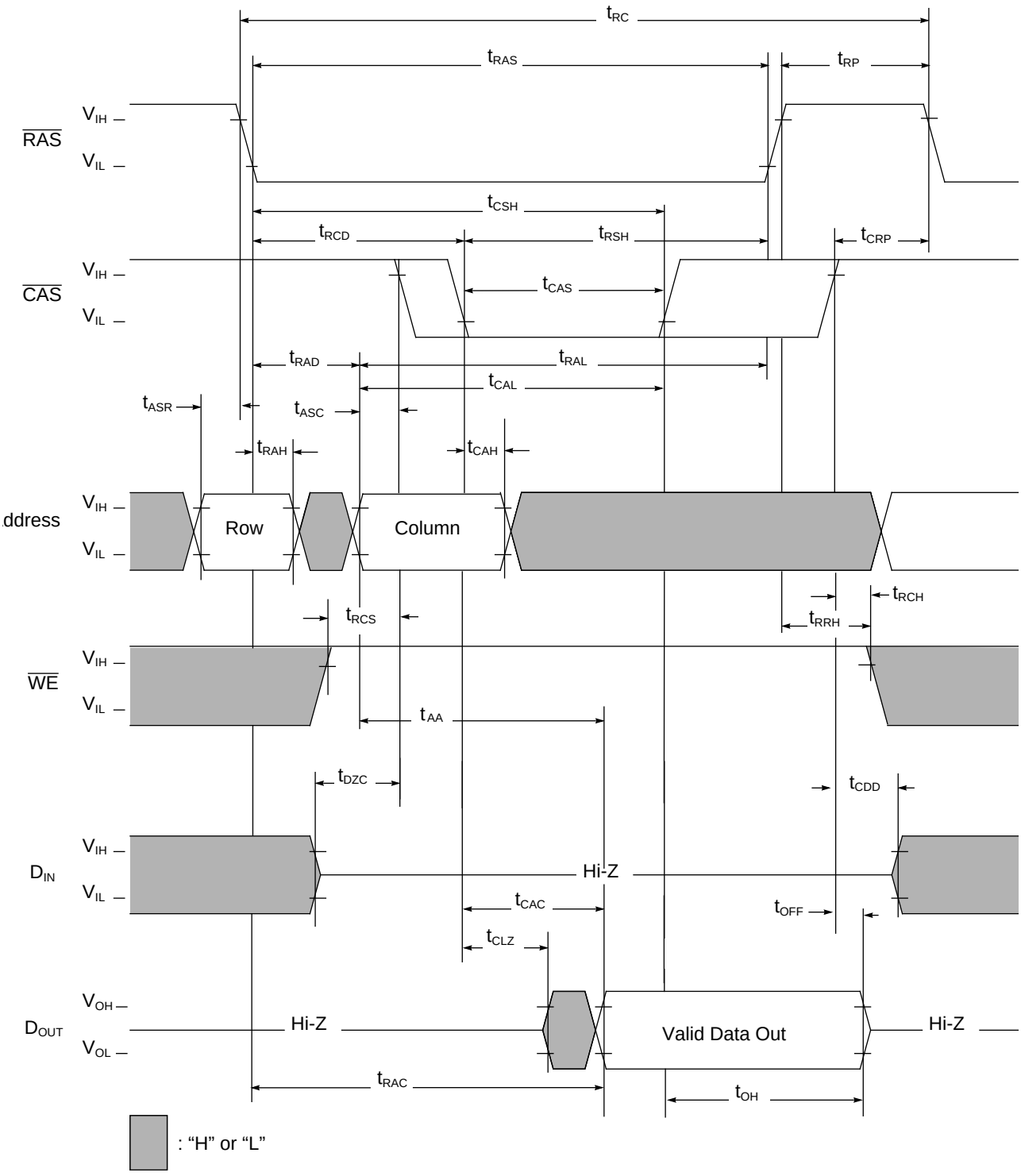
1. $\overline{RAS}$ is a “don’t care”.
2. ADDRESS and DATA are the specified address and read data.

Refresh Cycle

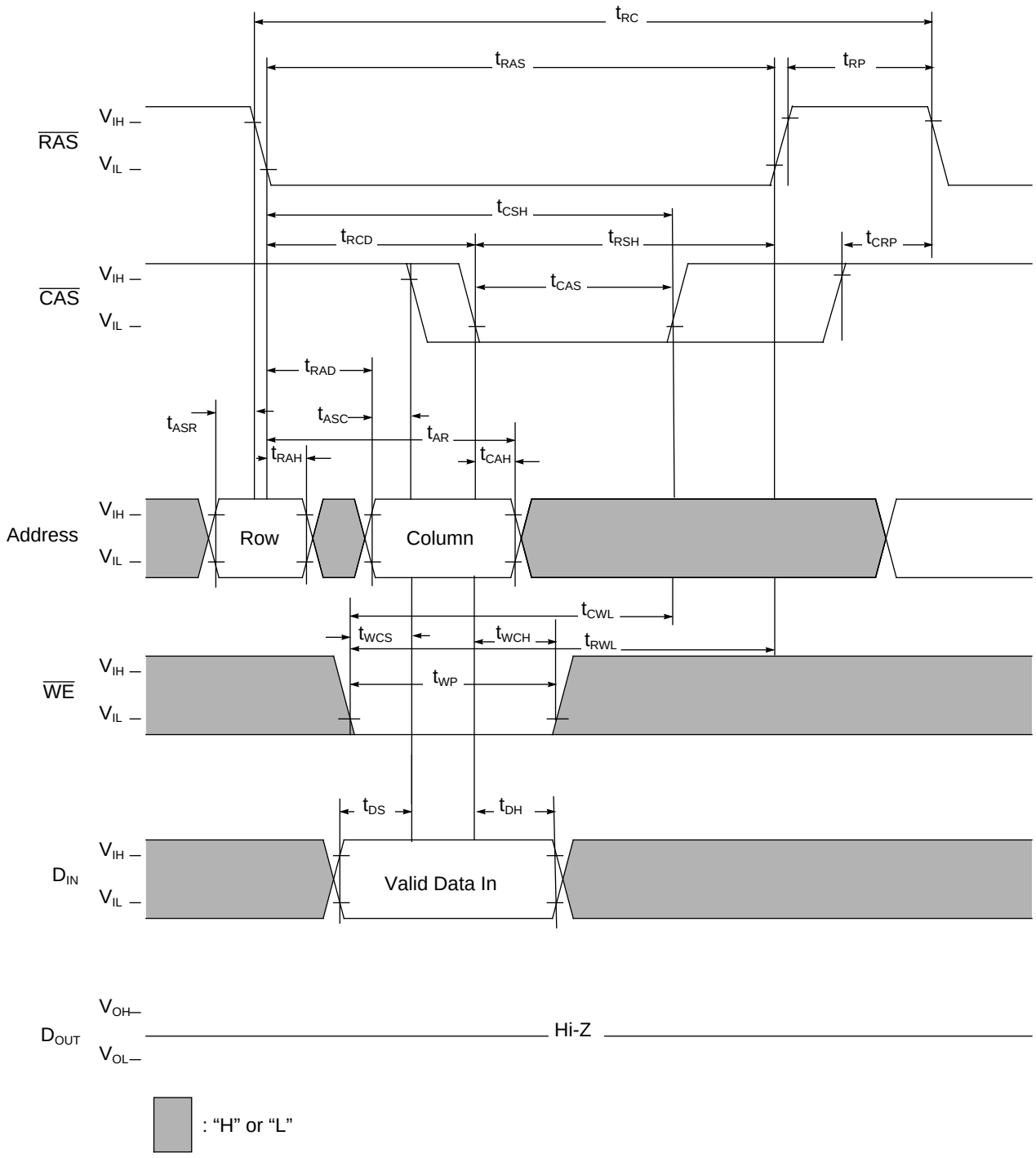
Symbol	Parameter	-70		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	ns	
t_{REF}	Refresh Period	—	32	ms	1

1. 2048 refreshes are required every 32ms. The DC variation in the V_{CC} supply may not exceed 300mV within a refresh interval (32ms).

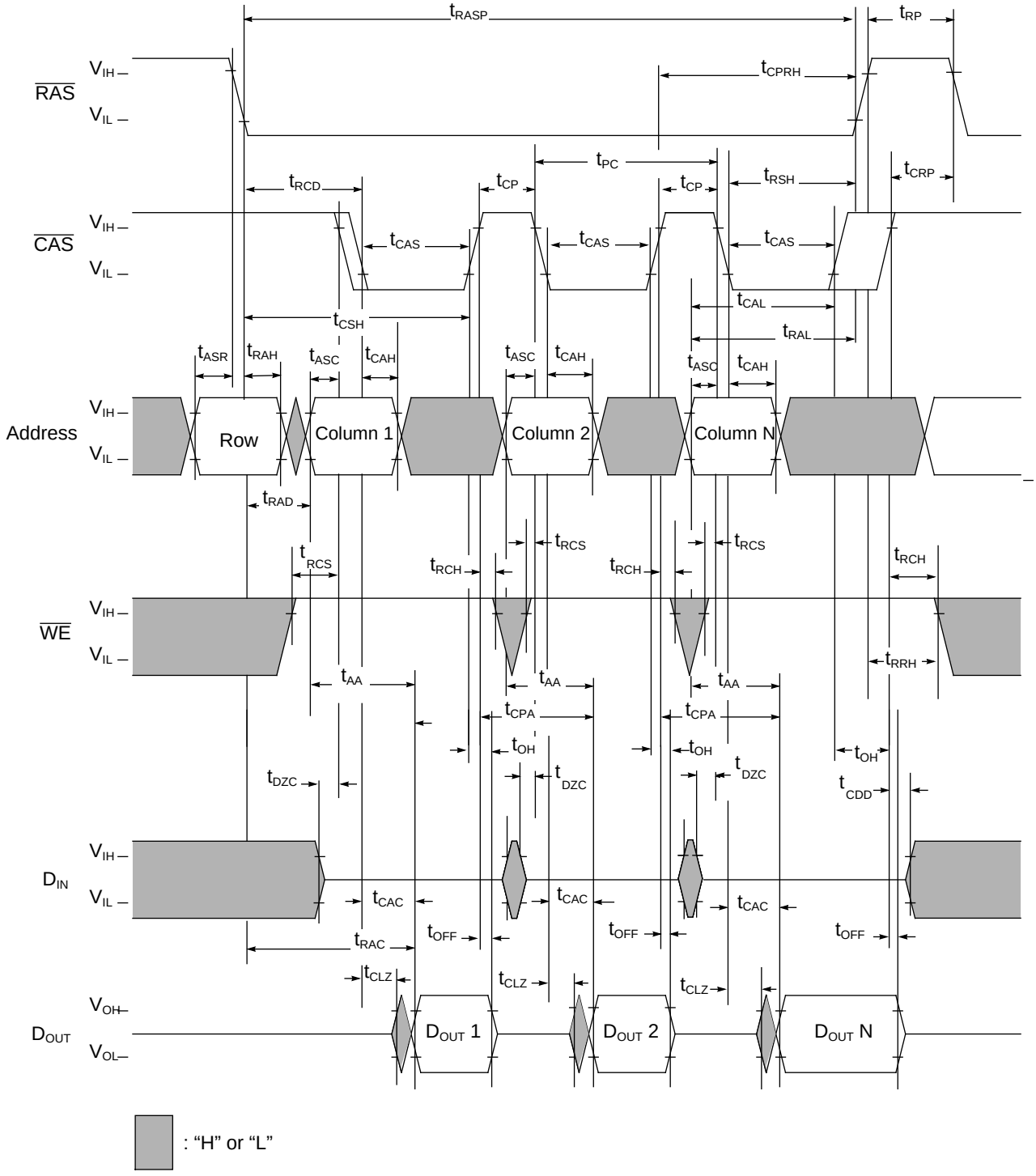
Read



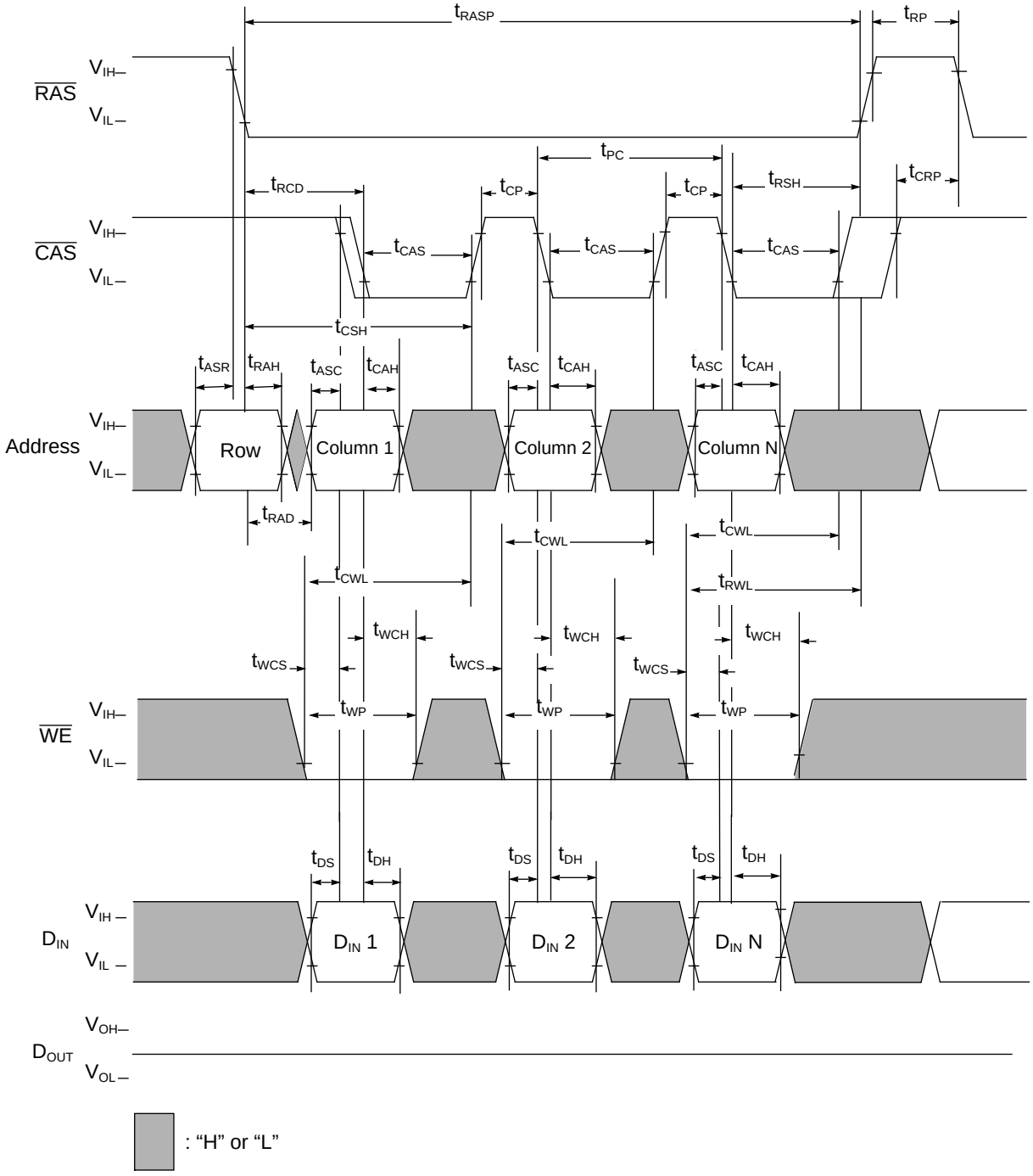
Write Cycle (Early Write)



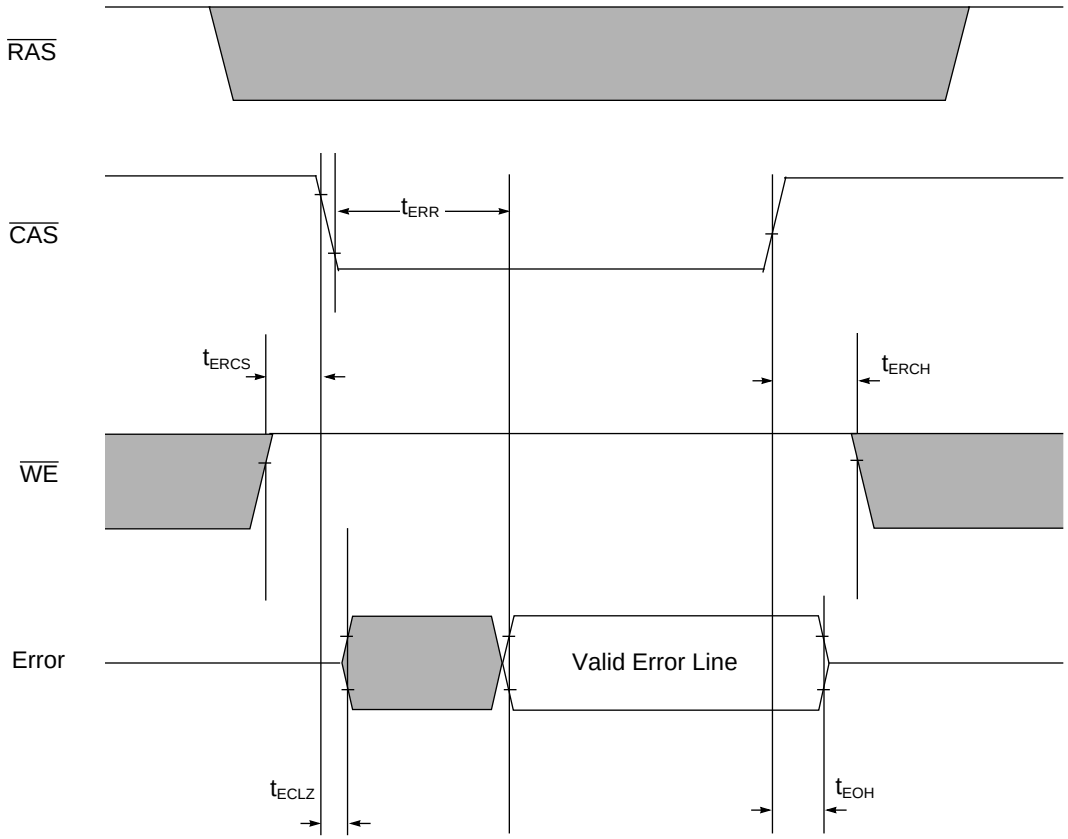
Fast Page Mode Read Cycle



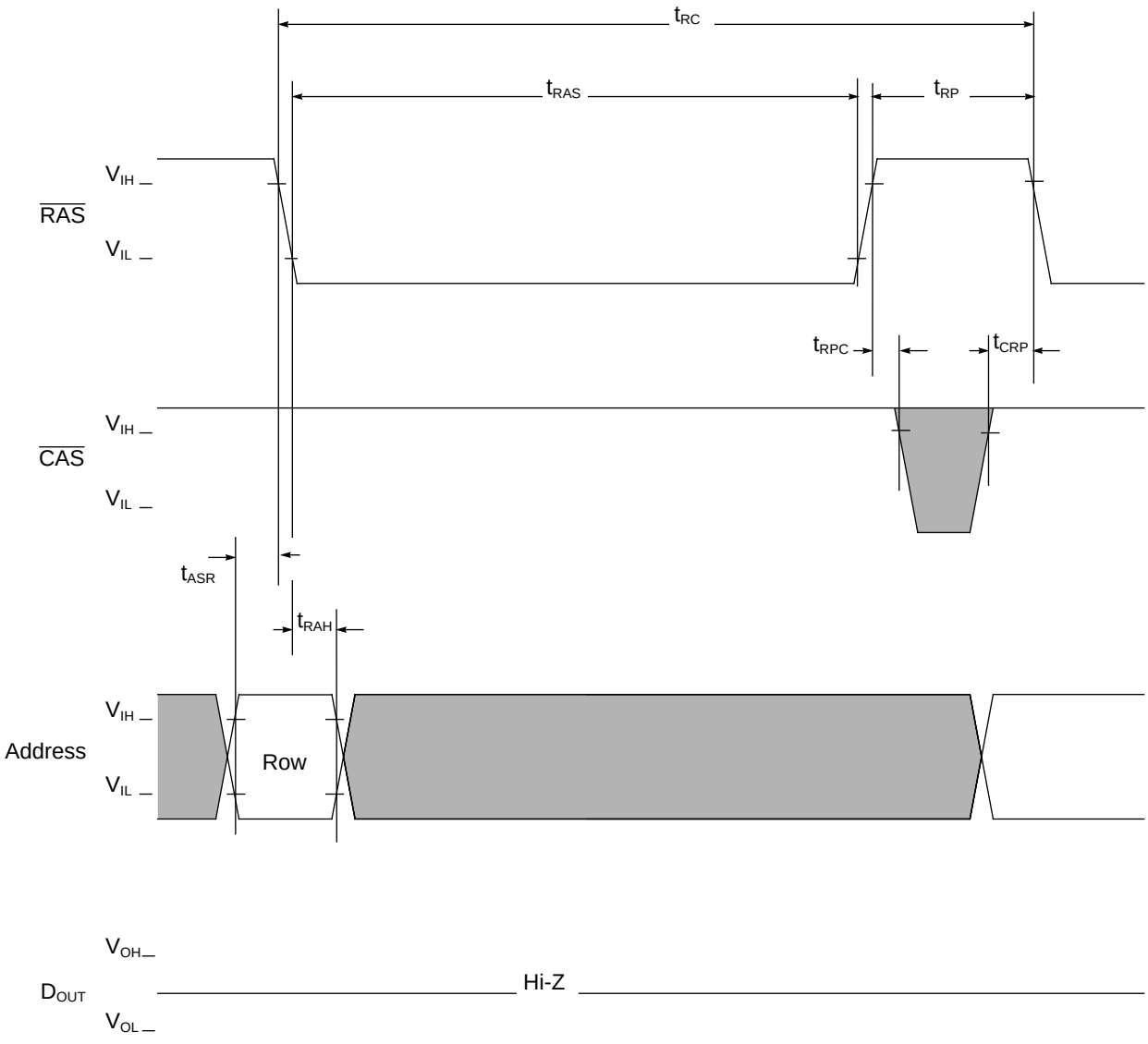
Fast Page Mode Write Cycle



Read Error-Line Functionality Timing Diagram



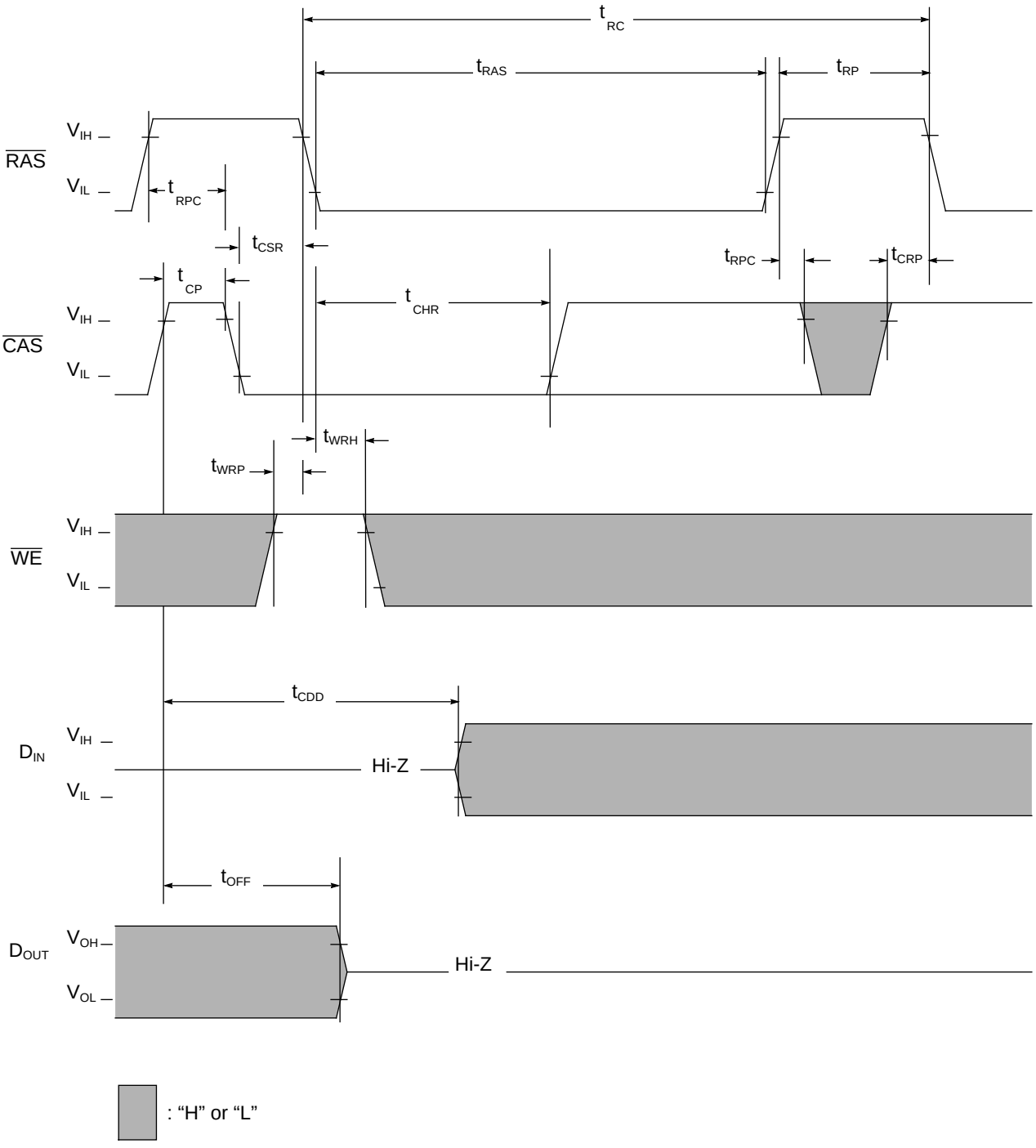
$\overline{RAS}$ Only Refresh Cycle



: “H” or “L”

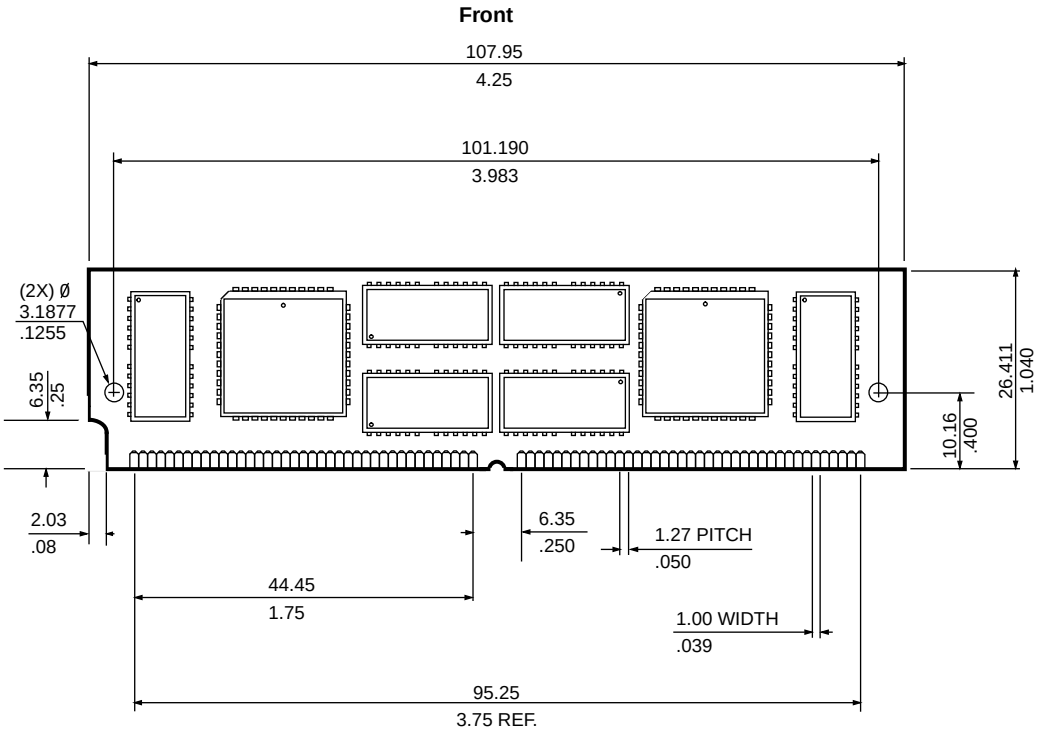
Note: $\overline{WE}$, D_{IN} are “H” or “L”

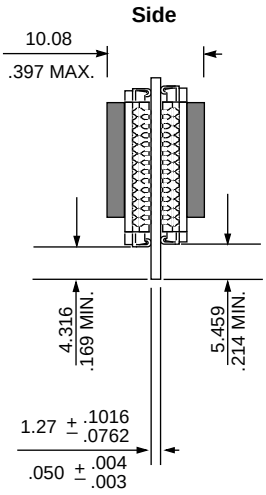
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing (4M x 36)

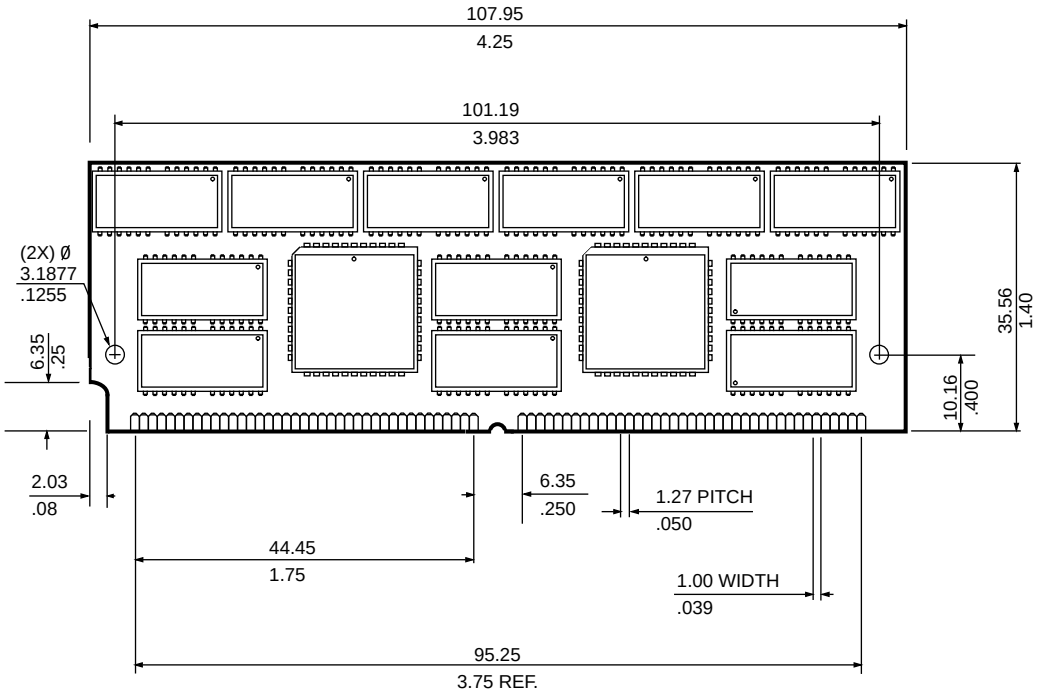




Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

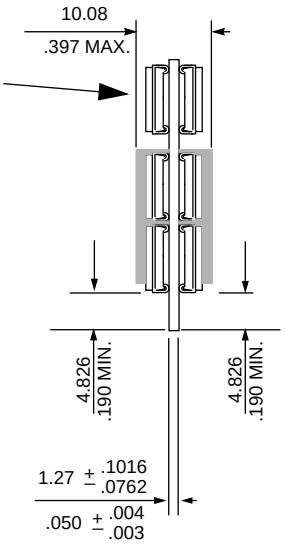
Layout Drawing (8M x 36)

Front



Side

A unique assembly is available with these 6 DRAMs in TSOP and the other 18 in SOJ packages..



Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Revision Log

Rev	Contents of Modification
7/96	Initial release.

For more information contact your IBM Microelectronics sales representative or
visit us on World Wide Web at http://www.chips.ibm.com