Integrated Device Technology, Inc.

256KB AND 512KB SECONDARY CACHE MODULES FOR THE INTEL PENTIUM™ CPU AND INTEL 82430 FAMILY CORE LOGIC PCISETS

PRELIMINARY
IDT7MPV6202/03
IDT7MPV6206/07
IDT7MPV6273/74
IDT7MPV6275/76

FEATURES

- For Intel Pentium CPU-based systems using the Intel 82430 family core logic PCIsets
- Modules are compliant to the Intel (Cache-on-a-Stick) COASt specification version 3.0
- Low-cost, low-profile card edge module with 160 leads
- Uses FCI connector from the CELP2X80SCXXXX family
- Operates with external Pentium CPU speeds up to 66MHz
- Separate 5V (±5%) and 3.3V (+10/-5%) power supplies
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- The 7MPV6273/74/75/76S66M use 10 ohm series resistors on the data lines
- Linear burst option

DESCRIPTION

The IDT7MPV6202/03/06/07/73/74/75/76 modules belong to a family of secondary caches intended for use with Intel Pentium CPU-based systems using the 82430 family core logic PCIsets. Module family members are compliant to the Intel Cache-on-a-Stick (COAST) specification version 3.0.

IDT7MPV6202/03/06/07/73/74 use 32K x 32 pipelined burst RAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. In addition, the IDT7MPV6202/03/73/74 modules use a single 5V 8-bit wide SRAM for the tag, while the IDT7MPV6206/07/75/76 use two 5V 8-bit wide SRAMs to achieve an 11-bit tag width.

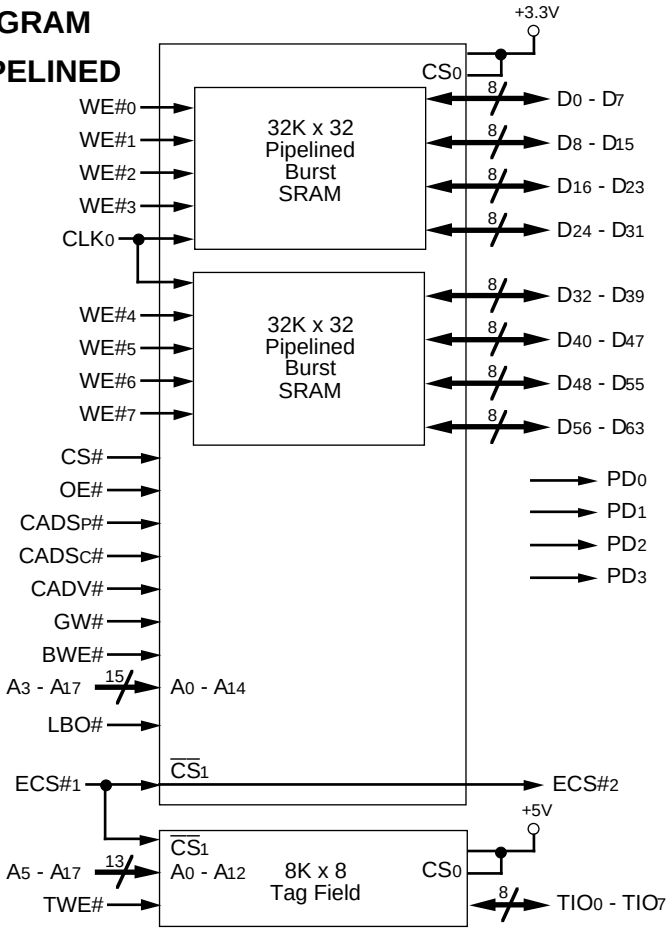
Four PD (presence detect) input pins allow the system to determine the particular cache configuration.

The low profile card edge package allows 160 signal leads to be placed on a package 4.35" long, a maximum of 0.350" thick and a maximum of 1.14" tall.

All inputs and outputs are TTL-compatible and operate from separate 5V (±5%) and 3.3V (+10/-5%) power supplies. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

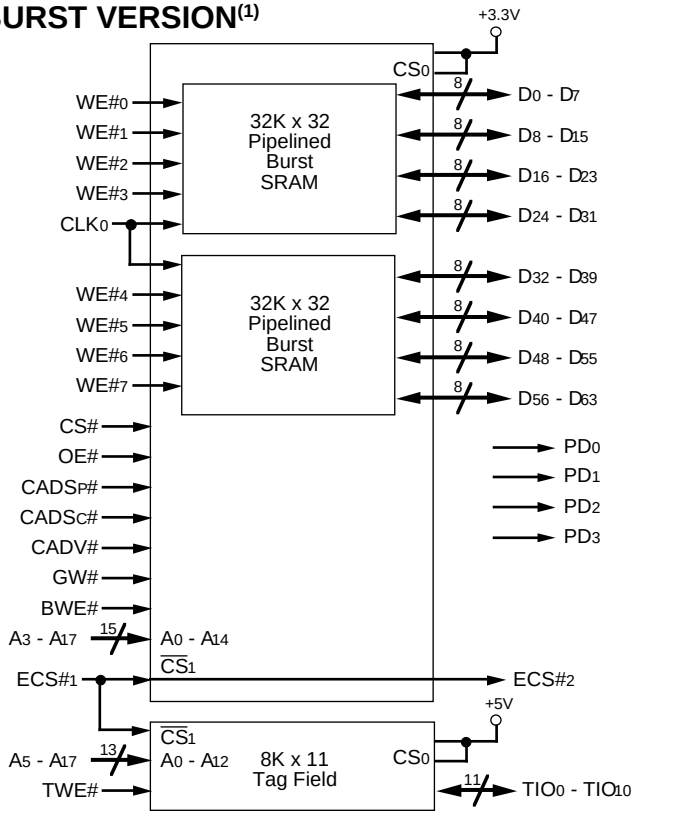
FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6202 – 256KB PIPELINED BURST VERSION



3150 drw 01

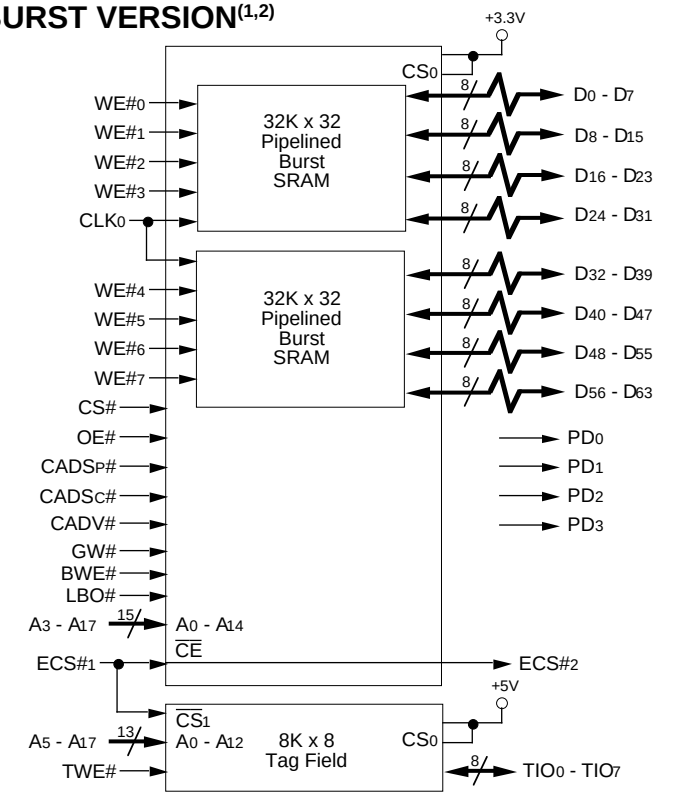
IDT7MPV6206 – 256KB PIPELINED BURST VERSION(1)



3150 drw 03

NOTE:
(1) TIO_{10} is tied to an 8.2k pull down resistor and TIO_{8-9} are tied to 8.2K pull up resistors.

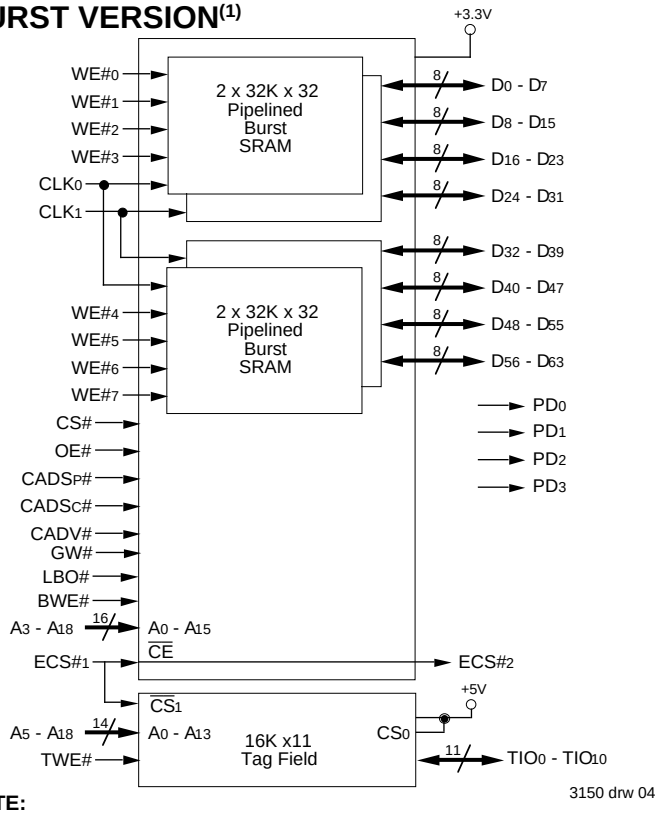
IDT7MPV6273/75 – 256KB PIPELINED BURST VERSION(1,2)



3150 drw 05

NOTES:
(1) Series resistor value of 7MPV6273/74 is 10 ohms.
(2) 7MPV6275 has an 11-bit Tag field like the 7MPV6206.

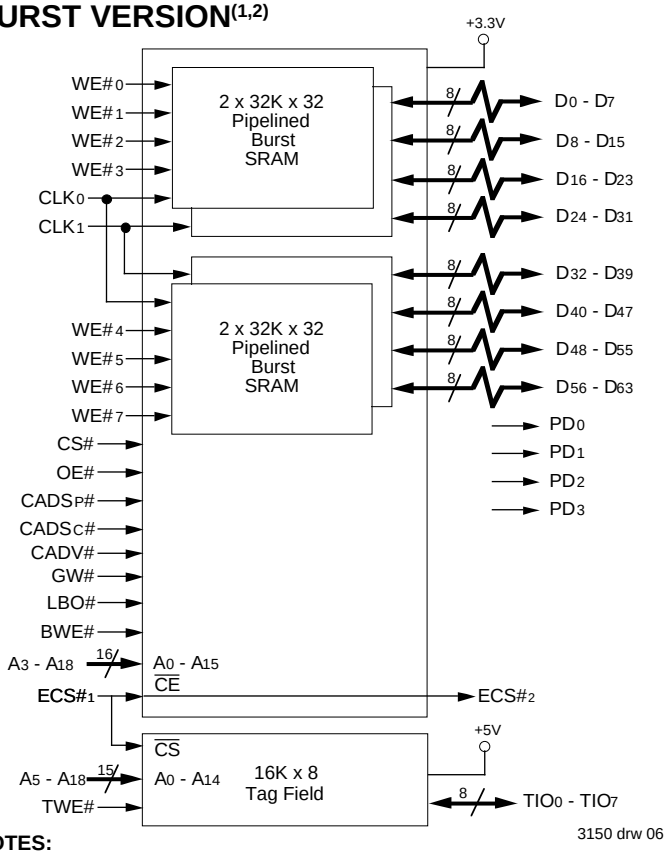
IDT7MPV6207 – 512KB PIPELINED BURST VERSION(1)



3150 drw 04

NOTE:
(1) TIO_{10} is tied to an 8.2k pull down resistor and TIO_{8-9} are tied to 8.2K pull up resistors.

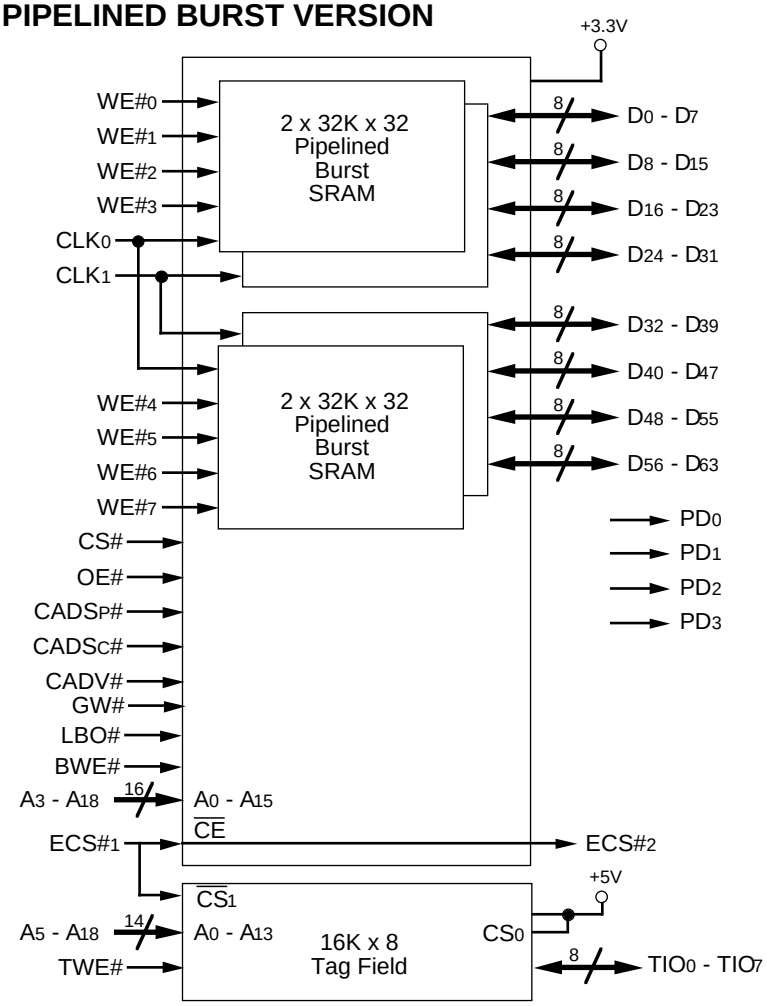
IDT7MPV6274/76 – 512KB PIPELINED BURST VERSION(1,2)



3150 drw 06

NOTES:
(1) LBO# is tied to a 4.7K pull up resistor.
(2) 7MPV6276 has an 11-bit tag field like the 7MPV6207.

IDT7MPV6203 – 512KB PIPELINED BURST VERSION



3150 drw 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC3}	Supply Voltage	3.146	3.3	3.6	V
V_{CC5}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = –1.0V for pulse width less than 5ns, once per cycle.

3150 tbl 01

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Power Plane	Ambient Temperature	GND	Vcc
V_{CC3}	0°C to +70°C	0V	3.3V +10/-5%
V_{CC5}	0°C to +70°C	0V	5.0V ± 5%

3150 tbl 02

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	V
V_{TERM} for V_{CC3}	Terminal Voltage with Respect to GND (V_{CC} terminals only)	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

3150 tbl 03

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN CONFIGURATION(1)

GND	81	1	GND
TIO1	82	2	TIO0
TIO7	83	3	TIO2
TIO5	84	4	TIO6
TIO3	85	5	TIO4
(1) TIO9	86	6	TIO8 (1)
VCC5	87	7	VCC3
(1) TIO10	88	8	TWE#
CADV#	89	9	CADSC#
GND	90	10	GND
COE#	91	11	WE#4
WE#5	92	12	WE#6
WE#7	93	13	WE#0
WE#1	94	14	WE#2
VCC5	95	15	VCC3
WE#3	96	16	CS#
(4) NC	97	17	GW#
NC	98	18	BWE#
GND	99	19	GND
(4) NC	100	20	A3
A4	101	21	A7
A6	102	22	A5
A8	103	23	A11
A10	104	24	A16
VCC5	105	25	VCC3
A17	106	26	A18 (2)
GND	107	27	GND
A9	108	28	A12
A14	109	29	A13
A15	110	30	CADSP#
(4) NC	111	31	ECS#1 (3)
PD0	112	32	ECS#2 (3)
PD2	113	33	PD1
LBO#	114	34	PD3
GND	115	35	GND
CLK0	116	36	CLK1 (2)
GND	117	37	GND
D63	118	38	D62
VCC5	119	39	VCC3
D61	120	40	D60
D59	121	41	D58
D57	122	42	D56
GND	123	43	GND
D55	124	44	D54
D53	125	45	D52
D51	126	46	D50
D49	127	47	D48
GND	128	48	GND
D47	129	49	D46
D45	130	50	D44
D43	131	51	D42
VCC5	132	52	VCC3
D41	133	53	D40
D39	134	54	D38
D37	135	55	D36
GND	136	56	GND
D35	137	57	D34
D33	138	58	D32
D31	139	59	D30
VCC5	140	60	VCC3
D29	141	61	D28
D27	142	62	D26
D25	143	63	D24
GND	144	64	GND
D23	145	65	D22
D21	146	66	D20
D19	147	67	D18
VCC5	148	68	VCC3
D17	149	69	D16
D15	150	70	D14
D13	151	71	D12
GND	152	72	GND
D11	153	73	D10
D9	154	74	D8
D7	155	75	D6
VCC5	156	76	VCC3
D5	167	77	D4
D3	158	78	D2
D1	159	79	D0
GND	160	80	GND

LOW PROFILE CARD EDGE MODULE
TOP VIEW

3150 drw 07

NOTES:
1. These pins are no connects for the IDT7MPV6202/03/73/74.
2. These pins are no connects for the IDT7MPV6202/06/73/75.
3. These pins are connected only for the 256KB module versions. If this module is not used as a 256KB upgrade to an existing 256KB already present in the system, then these pins should be tied to GND.
4. These pins are reserved for Fusion™ memory versions of the COASt module specification.

PIN NAMES

A3 – A18	Address Inputs
D0 – D63	Cache Data Inputs/Outputs
TIO0 – TIO7	Tag Inputs/Outputs
OE#	Cache Data Output Enable Input
TWE#	Tag Write Enable Input
WE#0 – WE#7	Cache Data Write Enable Inputs
CS#	Cache Data Chip Enable Input
CADSC#	Cache Address Status Input
CADSP#	Processor Address Status Input
CADV#	Burst Address Advance
GW#	Global Write Input
BWE#	Byte Write Enable Input
LBO#	Linear Burst Order
ECS#1	Expansion Chip Select Input
ECS#2	Expansion Chip Select Output
CLK0 – CLK1	Clock Inputs
PD0 – PD3	Presence Detect Pins
NC	No Connect
GND	Ground
VCC5	5 Volt Power Supply
VCC3	3.3 Volt Power Supply

3150 tbl 04

PRESENCE DETECT TABLE

PD3	PD2	PD1	PD0	Module
NC	NC	NC	NC	No cache present
NC	GND	NC	NC	IDT7MPV6202/06/73/75
GND	NC	GND	GND	IDT7MPV6203/07/74/76

3150 tbl 05

SRAM ACCESS TIMES

Module Speed	Burst[1]	Tag
66MHz	7.0ns	15ns

3150 tbl 06

NOTE:
1. Burst SRAMs are measured by Clock to Data Out (t_{CD}).

CAPACITANCE[1,2]

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	7MPV6202/06/73/75	7MPV6203/07/74/76	Unit
C_{IN1}	Input Capacitance (Address)	V_{IN} = 0V	20	30	pF
C_{IN2}	Input Capacitance (OE#)	V_{IN} = 0V	15	25	pF
C_{IN3}	Input Capacitance (WE#, TWE#)	V_{IN} = 0V	8	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	10	20	pF

3150 tbl 07

NOTES:
1. These parameters are guaranteed by design but not tested.
2. These parameters are maximum values.

DC ELECTRICAL CHARACTERISTICS

(V_{CC5} = 5.0V ± 5%, V_{CC3} = 3.3V +10/-5%, T_A = 0°C to 70°C)

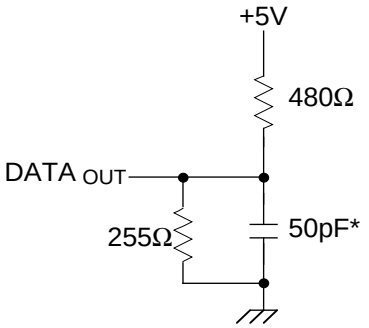
Symbol	Parameter	Test Condition	Min.	'02/06/73/75 Max.	'03/07/74/76 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	30	50	µA
$\|I_{LI}\|$	Input Leakage Current (Data and Control)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	20	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	0.4	V
V_{OH}	Output HighVoltage	I_{OH}= –4mA, V_{CC} = Min.	2.4	—	—	V
I_{CC3}	Operating 3.3V Power Supply Current	V_{CC3} = Max., $\overline{CE} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	500	620	mA
I_{CC5}	Operating 5V Power Supply Current	V_{CC5} = Max., $\overline{CE} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	180	180	mA
I_{SB3}	Standby 3.3V Power Supply Current	V_{CC3} = Max., $\overline{CE} \ge V_{IH}$, f = f_{MAX}, Outputs Open	—	60	120	mA
I_{SB31}	Full Standby 3.3V Power Supply Current	V_{CC3} = Max., $\overline{CE} \ge V_{CC}$ - 0.2V, f = 0, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}$ - 0.2V, Outputs Open	—	30	60	mA

3150 tbl 08

AC TEST CONDITIONS – 5V POWER SUPPLY

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

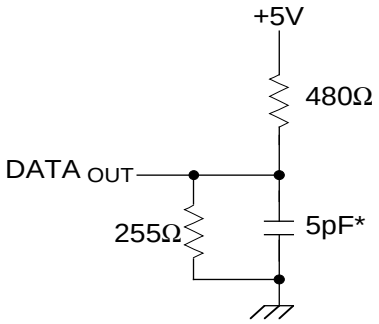
3150 tbl 09



*including scope and jig capacitances

Figure 1. Output Load

3150 drw 08



*including scope and jig capacitances

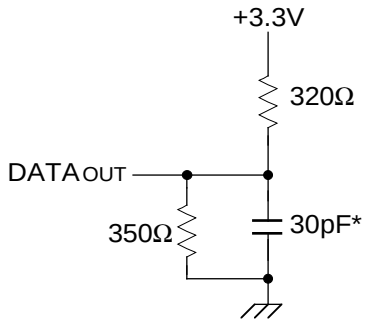
Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

3150 drw 09

AC TEST CONDITIONS – 3.3V POWER SUPPLY

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 3 and 4

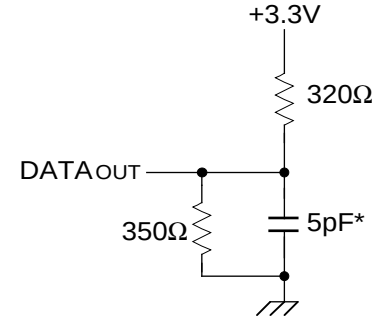
3150 tbl 10



*including scope and jig capacitances

Figure 3. Output Load

3150 drw 10

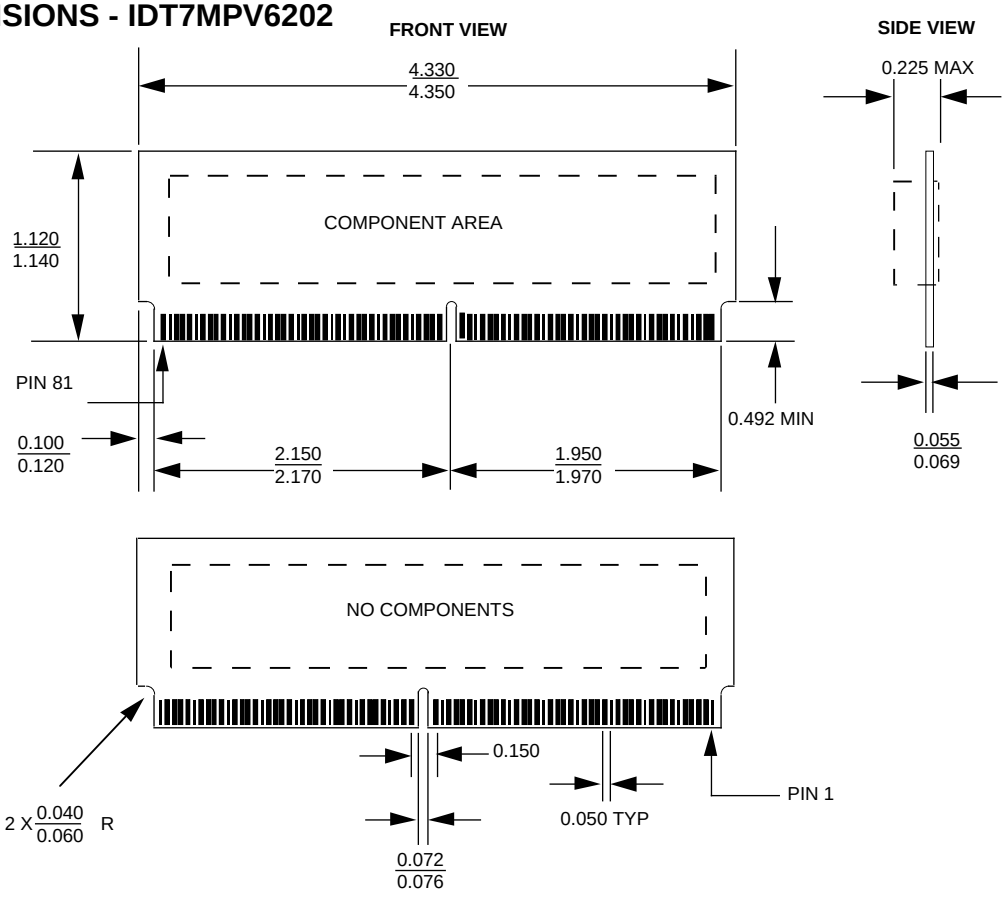


*including scope and jig capacitances

Figure 4. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

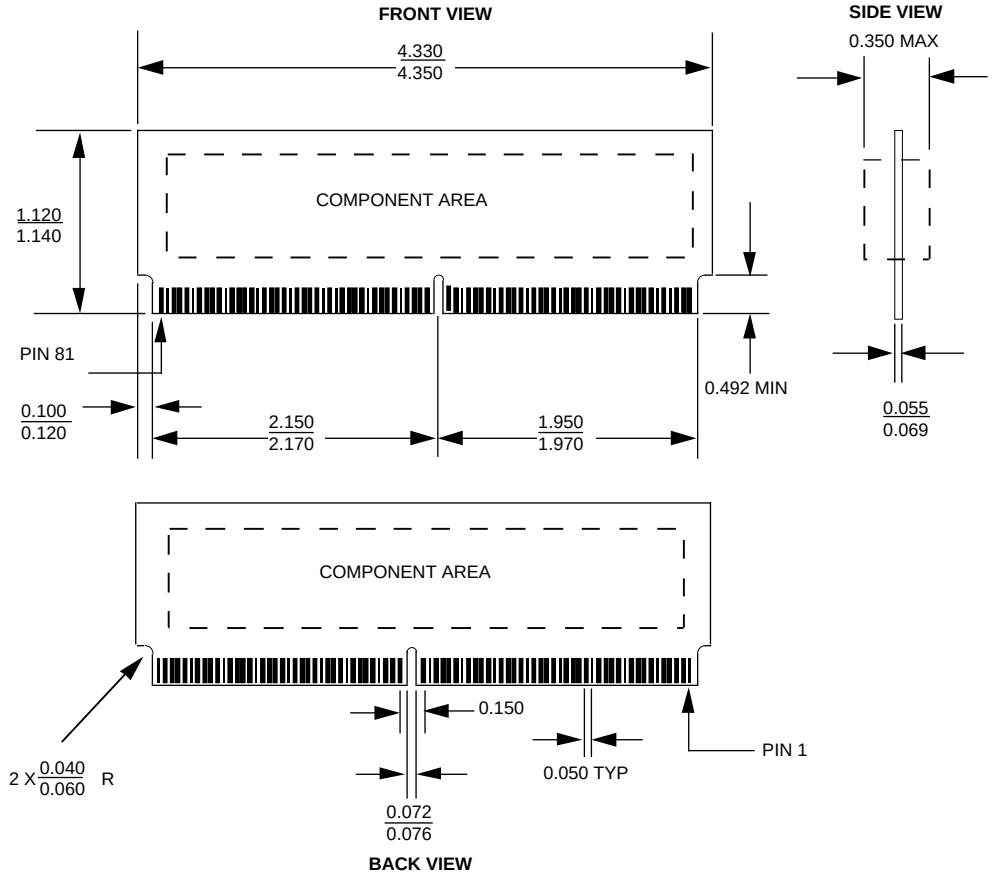
3150 drw 11

PACKAGE DIMENSIONS - IDT7MPV6202



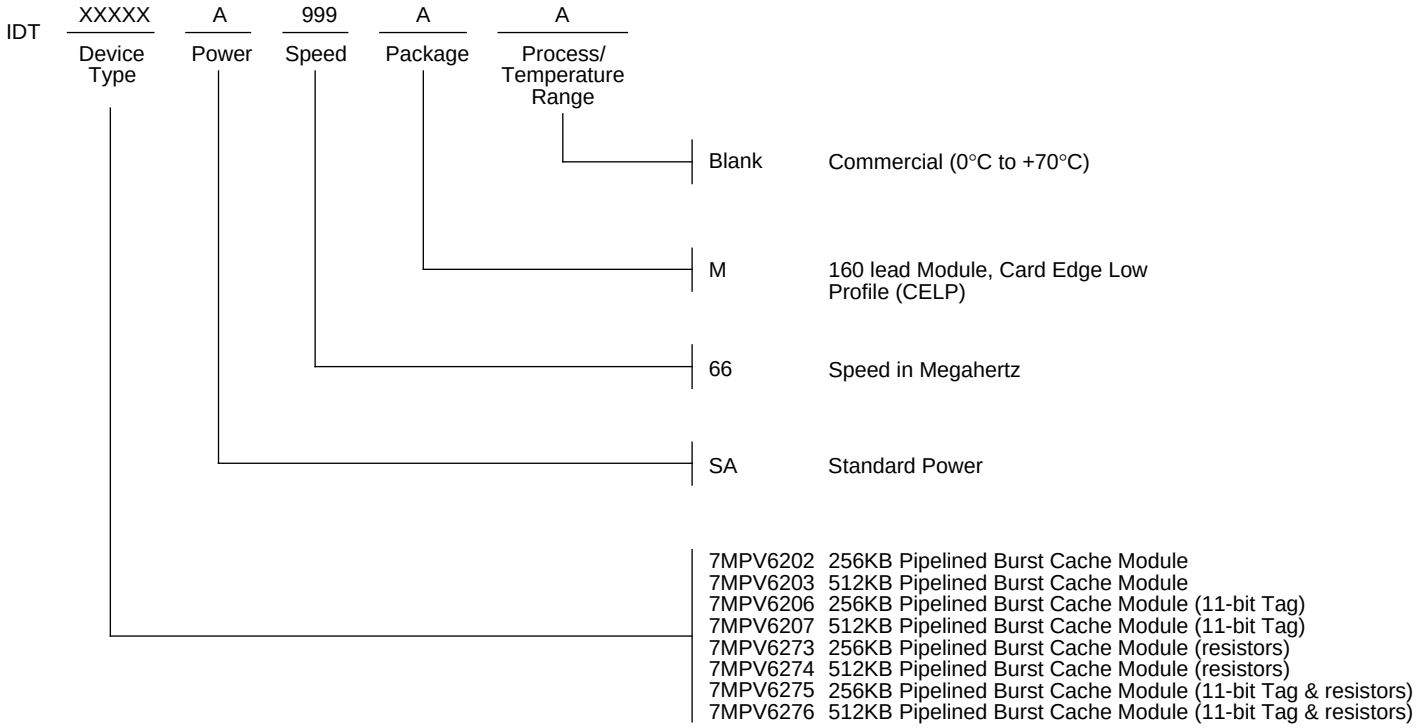
3150 drw 12

IDT7MPV6203/06/07/73/74/75/76



3150 drw 13

ORDERING INFORMATION



3150 drw 14