

DRAM

256K x 4 DRAM

STANDARD OR LOW POWER,
EXTENDED REFRESH

FEATURES

- 512-cycle refresh in 8ms (MT4C4256) or 64ms (MT4C4256 L)
- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V $\pm 10\%$ power supply
- Low power, 0.8mW standby; 175mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ (CBR), HIDDEN and Extended (MT4C4256 L only)
- Low CMOS Standby Current, 200 μ A maximum (MT4C4256 L)

OPTIONS

- Timing

60ns access	-6
70ns access	-7
80ns access	-8
- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z
- Version

512-cycle refresh in 8 ms	None
512-cycle refresh in 64 ms	L
- Part Number Example: MT4C4256DJ-7 L

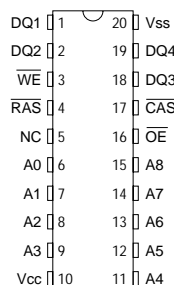
MARKING

GENERAL DESCRIPTION

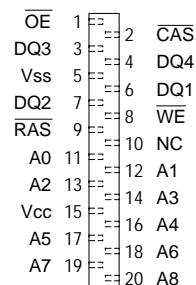
The MT4C4256(L) is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{\text{RAS}}$ is used to latch the first 9 bits and $\overline{\text{CAS}}$ the latter 9 bits. READ and WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW

PIN ASSIGNMENT (Top View)

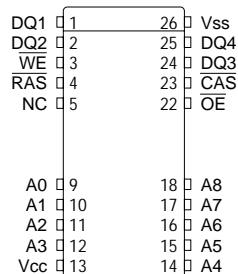
20-Pin DIP (DA-2)



20-Pin ZIP (DB-1)



20/26-Pin SOJ (DC-1)



prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{\text{WE}}$ and OE.

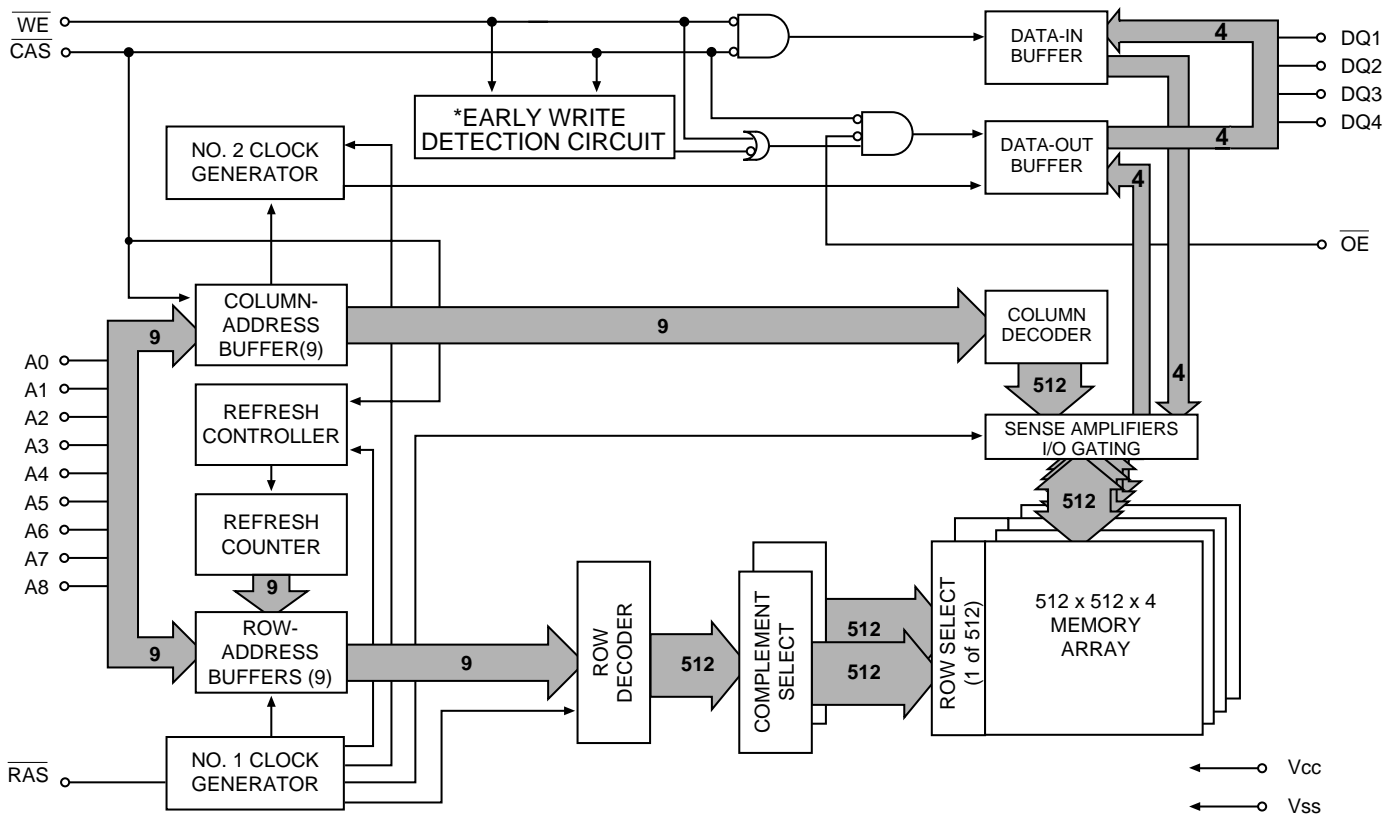
FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-

in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE cycle.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct

state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ REFRESH cycle ($\overline{\text{RAS}}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{\text{RAS}}$ addresses (A0-A8) are executed at least every 8ms for the MT4C4256 and every 64ms for the MT4C4256 L, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{\text{RAS}}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{\text{CAS}}$ goes LOW prior to $\overline{\text{WE}}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		\overline{RAS}	\overline{CAS}	\overline{WE}	\overline{OE}	ADDRESSES		DATA-IN/OUT
						t _R	t _C	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
\overline{RAS} ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	X	X	X	X	High-Z
Extended Refresh (MT4C4256 L only)		H→L	L	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V _{SS}	-1V to +7V
Operating Temperature, T _A (ambient)	0°C to +70°C
Storage Temperature (plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

 (Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V _{IH}	2.4	V _{CC} +1	V	
Input Low (Logic 0) Voltage, all inputs	V _{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ 6.5V (All other pins not under test = 0V)	I _I	-2	2	μA	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V)	I _{OZ}	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -5mA)	V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 4.2mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX			UNITS	NOTES
			-6	-7	-8		
STANDBY CURRENT: (TTL) (R _{AS} = C _{AS} = V _{IH})		I _{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) (R _{AS} = C _{AS} = V _{CC} -0.2V)	MT4C4256	I _{CC2}	1	1	1	mA	
	MT4C4256 L	I _{CC2}	200	200	200	μA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (R _{AS} , C _{AS} , Single Address Cycling: t _{RC} = t _{RC} [MIN])		I _{CC3}	90	80	70	mA	3, 4, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current (R _{AS} = V _{IL} , C _{AS} , Address Cycling: t _{PC} = t _{PC} [MIN])		I _{CC4}	70	60	50	mA	3, 4, 29
REFRESH CURRENT: R _{AS} ONLY Average power supply current (R _{AS} Cycling, C _{AS} = V _{IH} : t _{RC} = t _{RC} [MIN])		I _{CC5}	90	80	70	mA	3, 29
REFRESH CURRENT: CBR Average power supply current (R _{AS} , C _{AS} , Address Cycling: t _{RC} = t _{RC} [MIN])		I _{CC6}	90	80	70	mA	3, 5
REFRESH CURRENT: Extended Average power supply current during Extended Refresh: C _{AS} = 0.2V or CBR cycling; R _{AS} = t _{RAS} (MIN) to 1μs; WE, A0-A8 and D _{IN} = V _{CC} -0.2V or 0.2V (D _{IN} may be left open); t _{RC} = 125μs (512 rows at 125μs = 64ms)	MT4C4256 L	I _{CC7}	200	200	200	μA	3, 5, 27

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C _{I1}		5	pF	2
Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	C _{I2}		7	pF	2
Input/Output Capacitance: DQ	C _{I0}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t ^{RC}	110		130		150		ns	
READ WRITE cycle time	t ^{RWC}	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t ^{PC}	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t ^{PRWC}	90		95		100		ns	
Access time from $\overline{\text{RAS}}$	t ^{RAC}		60		70		80	ns	14
Access time from $\overline{\text{CAS}}$	t ^{CAC}		20		20		20	ns	15
Output Enable	t ^{OE}		20		20		20	ns	
Access time from column-address	t ^{AA}		30		35		40	ns	
Access time from $\overline{\text{CAS}}$ precharge	t ^{CPA}		35		40		45	ns	
$\overline{\text{RAS}}$ pulse width	t ^{RAS}	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	t ^{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ hold time	t ^{RSH}	20		20		20		ns	
$\overline{\text{RAS}}$ precharge time	t ^{RP}	40		50		60		ns	
$\overline{\text{CAS}}$ pulse width	t ^{CAS}	20	100,000	20	100,000	20	100,000	ns	
$\overline{\text{CAS}}$ hold time	t ^{CSH}	60		70		80		ns	
$\overline{\text{CAS}}$ precharge time	t ^{CPN}	10		10		10		ns	16
$\overline{\text{CAS}}$ precharge time (FAST PAGE MODE)	t ^{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t ^{RCD}	20	40	20	50	20	60	ns	17
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t ^{CRP}	5		5		5		ns	
Row-address setup time	t ^{ASR}	0		0		0		ns	
Row-address hold time	t ^{RAH}	10		10		10		ns	
$\overline{\text{RAS}}$ to column-address delay time	t ^{RAD}	15	30	15	35	15	40	ns	18
Column-address setup time	t ^{ASC}	0		0		0		ns	
Column-address hold time	t ^{CAH}	15		15		15		ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	t ^{AR}	45		55		60		ns	
Column-address to $\overline{\text{RAS}}$ lead time	t ^{RAL}	30		35		40		ns	
Read command setup time	t ^{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{\text{CAS}}$)	t ^{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{\text{RAS}}$)	t ^{RRH}	0		0		0		ns	19
$\overline{\text{CAS}}$ to output in Low-Z	t ^{CLZ}	0		0		0		ns	

OBSOLETE


MT4C4256(L)
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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	t_{OFF}	3	20	3	20	3	20	ns	20, 26, 28
Output disable	t_{OD}		15		20		20	ns	26
\overline{WE} command setup time	t_{WCS}	0		0		0		ns	21
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time (referenced to RAS)	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to \overline{RAS} lead time	t_{RWL}	20		20		20		ns	
Write command to \overline{CAS} lead time	t_{CWL}	20		20		20		ns	
Data-in setup time	t_{DS}	0		0		0		ns	22
Data-in hold time	t_{DH}	15		15		15		ns	22
Data-in hold time (referenced to RAS)	t_{DHR}	45		55		60		ns	
\overline{RAS} to \overline{WE} delay time	t_{RWD}	85		100		110		ns	21
Column-address to \overline{WE} delay time	t_{AWD}	60		65		70		ns	21
\overline{CAS} to \overline{WE} delay time	t_{CWD}	40		50		55		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles) MT4C4256 / MT4C4256 L	t_{REF}		8 / 64		8 / 64		8 / 64	ms	
\overline{RAS} to \overline{CAS} precharge time	t_{RPC}	0		0		0		ns	
\overline{CAS} setup time (CBR REFRESH)	t_{CSR}	10		10		10		ns	5
\overline{CAS} hold time (CBR REFRESH)	t_{CHR}	10		15		15		ns	5
\overline{OE} hold time from \overline{WE} during READ-MODIFY-WRITE cycle	t_{OEH}	15		20		20		ns	25
\overline{OE} setup prior to \overline{RAS} during HIDDEN REFRESH cycle	t_{ORD}	0		0		0		ns	24

NOTES

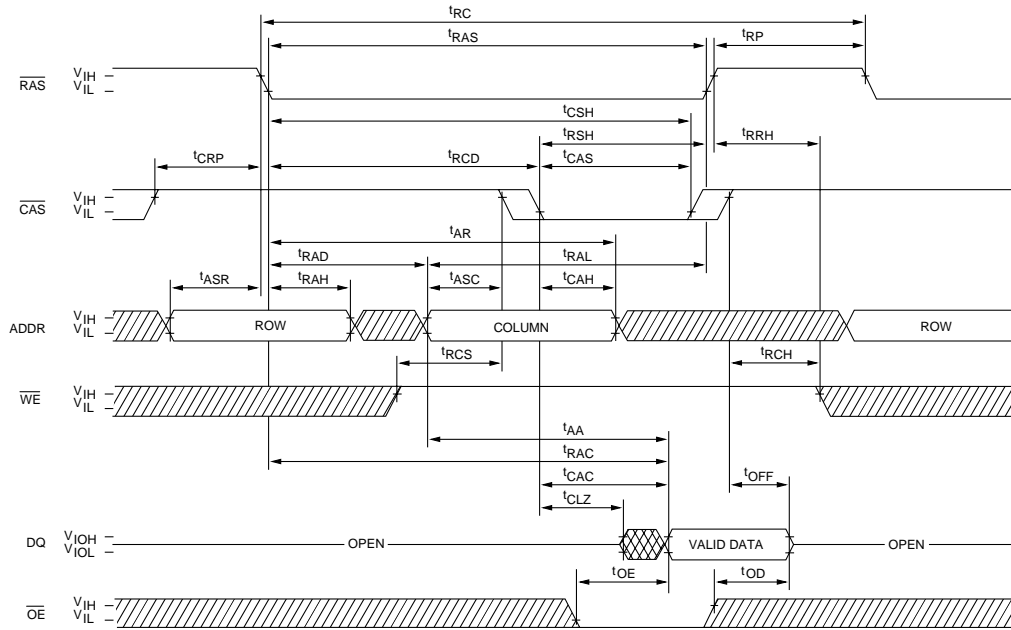
1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = 5V \pm 10\%$; $f = 1 \text{ MHz}$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of $100\mu\text{s}$ is required after power-up followed by any eight $\overline{\text{RAS}}$ cycles before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ${}^t\text{REF}$ refresh requirement is exceeded.
8. AC characteristics assume ${}^tT = 5\text{ns}$.
9. $V_{IH}(\text{MIN})$ and $V_{IL}(\text{MAX})$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}} = V_{IH}$, data output is High-Z.
12. If $\overline{\text{CAS}} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF .
14. Assumes that ${}^t\text{RCD} < {}^t\text{RCD}(\text{MAX})$. If ${}^t\text{RCD}$ is greater than the maximum recommended value shown in this table, ${}^t\text{RAC}$ will increase by the amount that ${}^t\text{RCD}$ exceeds the value shown.
15. Assumes that ${}^t\text{RCD} \geq {}^t\text{RCD}(\text{MAX})$.
16. If CAS is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ${}^t\text{CPN}$.
17. Operation within the ${}^t\text{RCD}(\text{MAX})$ limit ensures that ${}^t\text{RAC}(\text{MAX})$ can be met. ${}^t\text{RCD}(\text{MAX})$ is specified as a reference point only; if ${}^t\text{RCD}$ is greater than the specified ${}^t\text{RCD}(\text{MAX})$ limit, then access time is controlled exclusively by ${}^t\text{CAC}$.
18. Operation within the ${}^t\text{RAD}(\text{MAX})$ limit ensures that ${}^t\text{RAC}(\text{MIN})$ and ${}^t\text{CAC}(\text{MIN})$ can be met. ${}^t\text{RAD}(\text{MAX})$ is specified as a reference point only; if ${}^t\text{RAD}$ is greater than the specified ${}^t\text{RAD}(\text{MAX})$ limit, then access time is controlled exclusively by ${}^t\text{AA}$.
19. Either ${}^t\text{RCH}$ or ${}^t\text{RRH}$ must be satisfied for a READ cycle.
20. ${}^t\text{OFF}(\text{MAX})$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
21. ${}^t\text{WCS}$, ${}^t\text{RWD}$, ${}^t\text{AWD}$ and ${}^t\text{CWD}$ are not restrictive operating parameters. ${}^t\text{WCS}$ applies to EARLY WRITE cycles. ${}^t\text{RWD}$, ${}^t\text{AWD}$ and ${}^t\text{CWD}$ apply to READ-MODIFY-WRITE cycles. If ${}^t\text{WCS} \geq {}^t\text{WCS}(\text{MIN})$, the cycle is an EARLY WRITE cycle, and the data output will remain an open circuit throughout the entire cycle. If ${}^t\text{RWD} \geq {}^t\text{RWD}(\text{MIN})$, ${}^t\text{AWD} \geq {}^t\text{AWD}(\text{MIN})$ and ${}^t\text{CWD} \geq {}^t\text{CWD}(\text{MIN})$, the cycle is a READ-MODIFY-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$ -controlled) cycle. ${}^t\text{WCS}$, ${}^t\text{RWD}$, ${}^t\text{CWD}$ and ${}^t\text{AWD}$ are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}} = \text{LOW}$ and $\overline{\text{OE}} = \text{HIGH}$.
25. LATE WRITE and READ-MODIFY-WRITE cycles must have both ${}^t\text{OD}$ and ${}^t\text{OEH}$ met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{\text{OE}}$ is taken back LOW while $\overline{\text{CAS}}$ remains LOW, the DQs will remain open.
26. The DQs open during READ cycles once ${}^t\text{OD}$ or ${}^t\text{OFF}$ occur. If $\overline{\text{CAS}}$ goes HIGH before $\overline{\text{OE}}$, the DQs will open regardless of the state of $\overline{\text{OE}}$. If $\overline{\text{CAS}}$ stays LOW while $\overline{\text{OE}}$ is brought HIGH, the DQs will open. If $\overline{\text{OE}}$ is brought back LOW ($\overline{\text{CAS}}$ still LOW), the DQs will provide the previously read data.
27. Extended refresh current is reduced as ${}^t\text{RAS}$ is reduced from its maximum specification during the extended refresh cycle.
28. The 3ns minimum is a parameter guaranteed by design.
29. Column-address changed once each cycle.

OBSOLETE

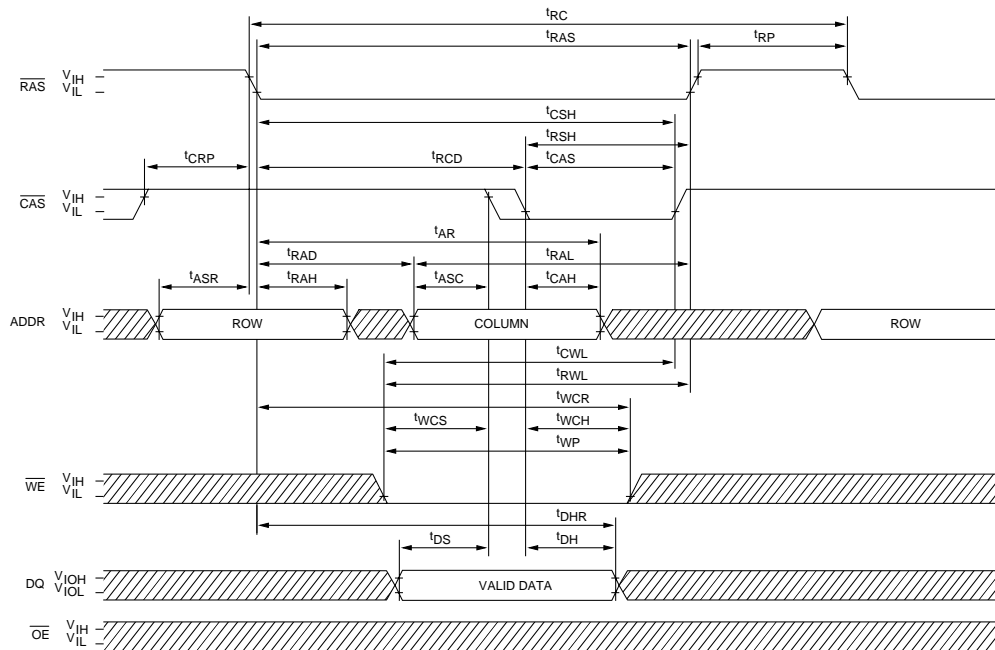


MT4C4256(L)
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READ CYCLE

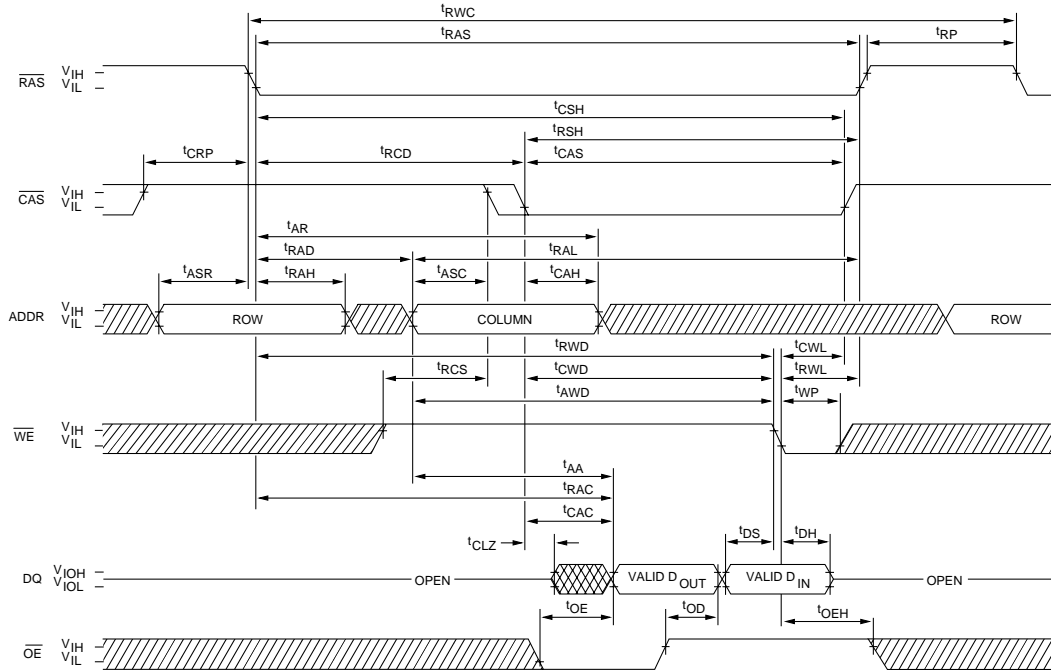


EARLY WRITE CYCLE

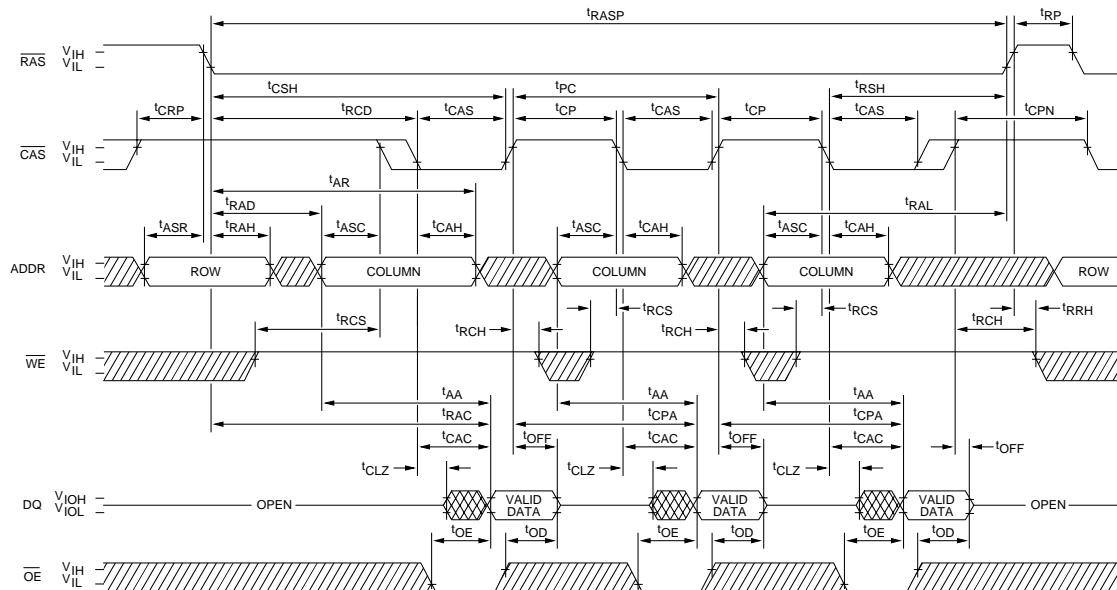


▨ DON'T CARE
▩ UNDEFINED

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)

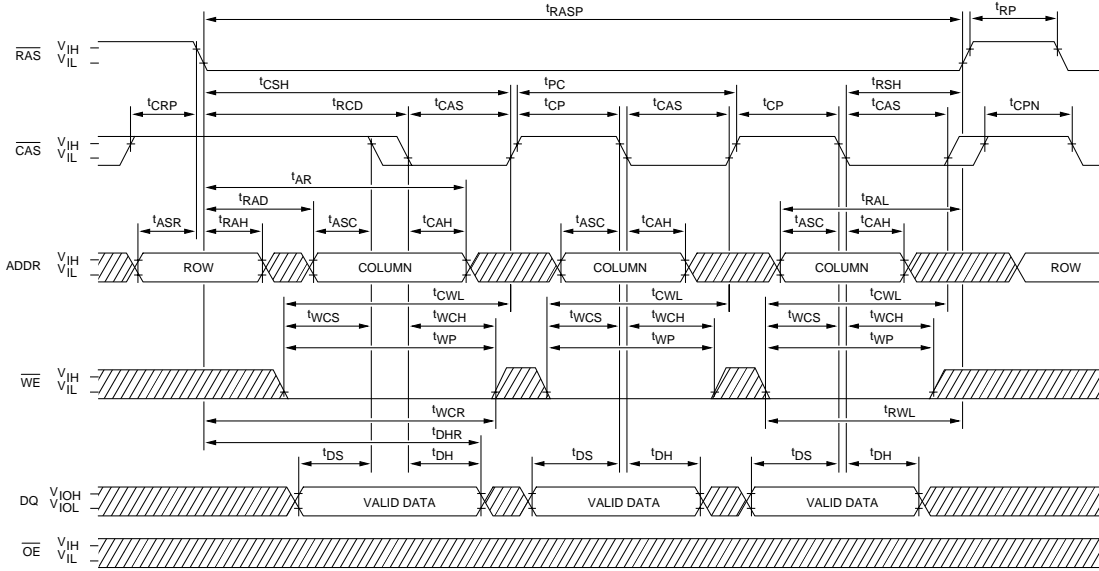


FAST-PAGE-MODE READ CYCLE

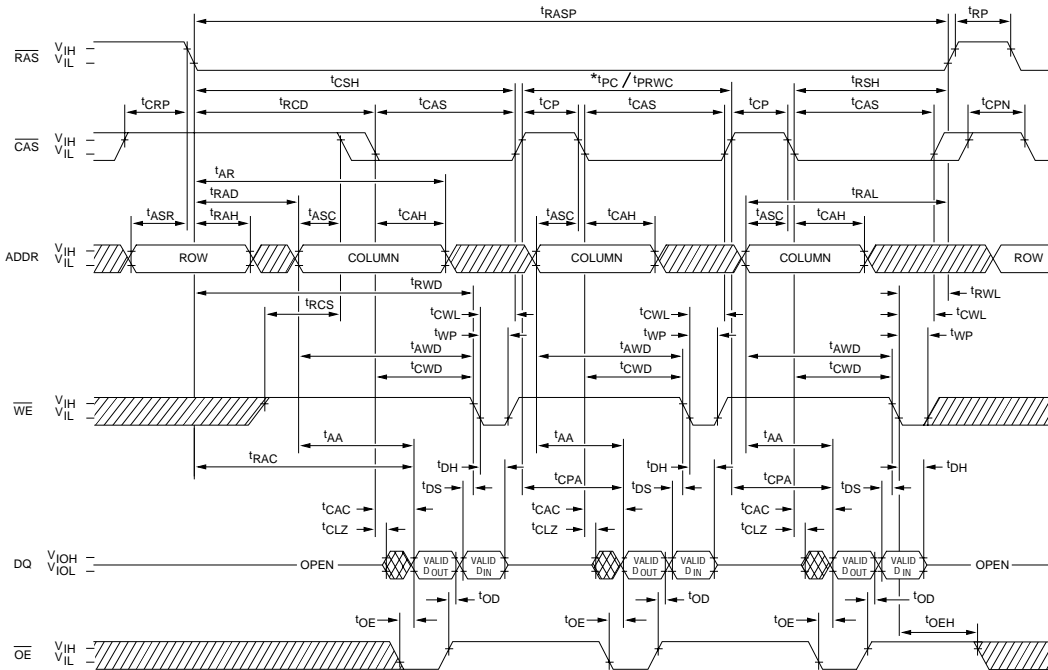


▨ DON'T CARE
▩ UNDEFINED

FAST-PAGE-MODE EARLY-WRITE CYCLE



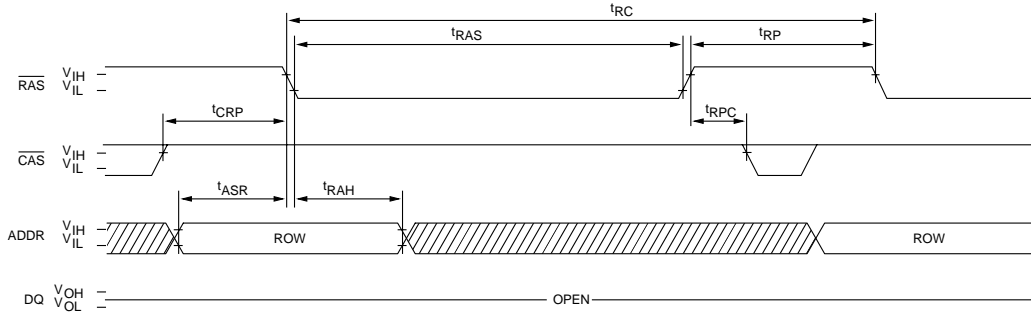
FAST-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE CYCLES)



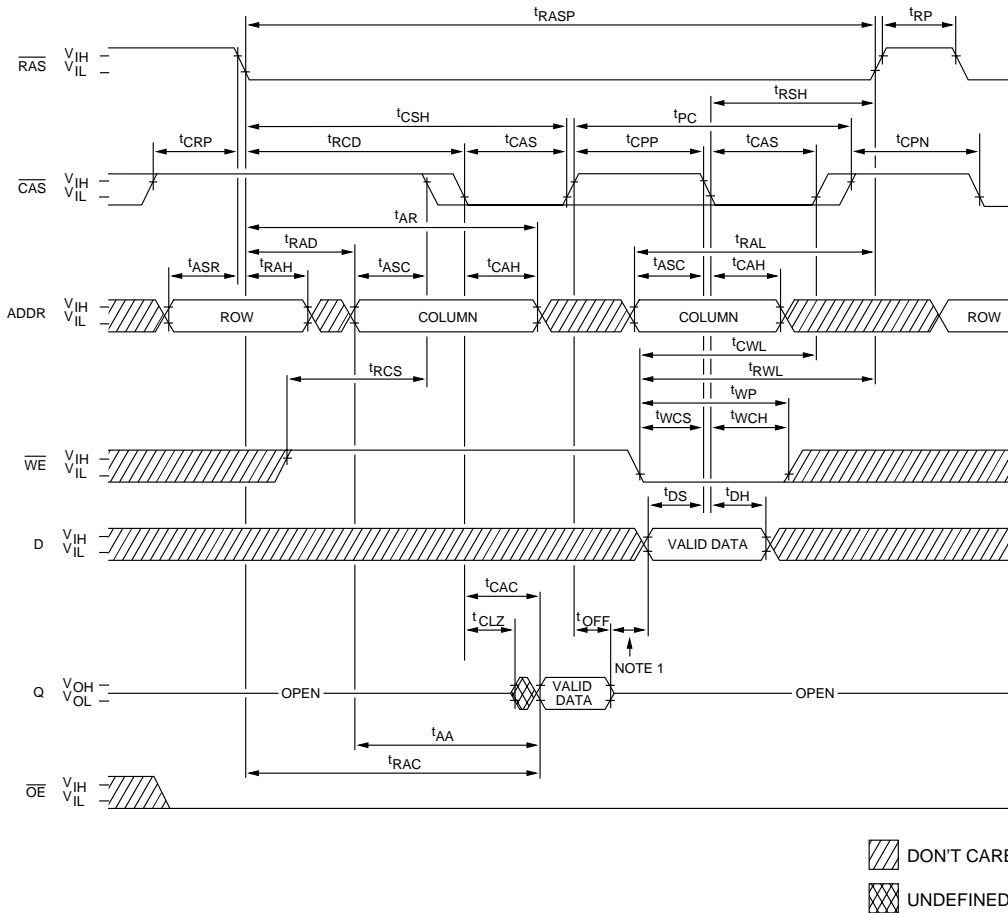
DON'T CARE
 UNDEFINED

* t_{PC} is for LATE WRITE only.

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{\text{WE}}$ = DON'T CARE)

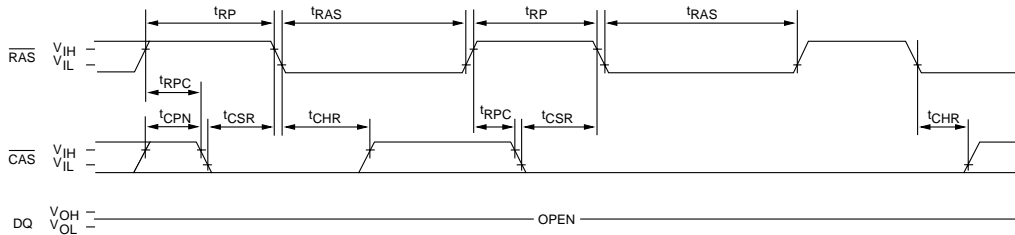


FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

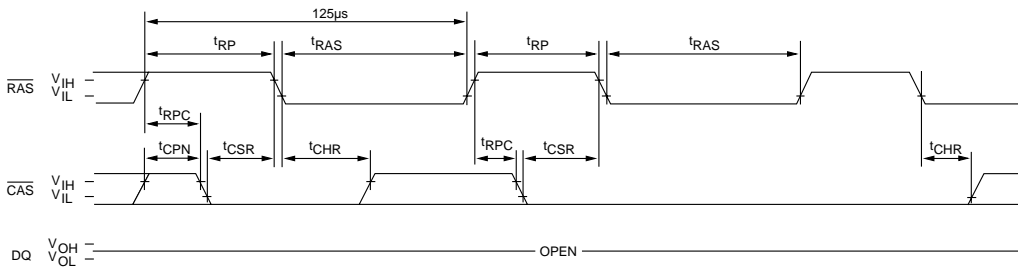


NOTE: 1. Do not drive data prior to tristate: $t_{CPP}(\text{MIN})$ or $t_{CP}(\text{whichever is greater}) + t_{DS}(\text{MIN}) + \text{any guardband}$ between data-out and driving the bus with the new data-in.

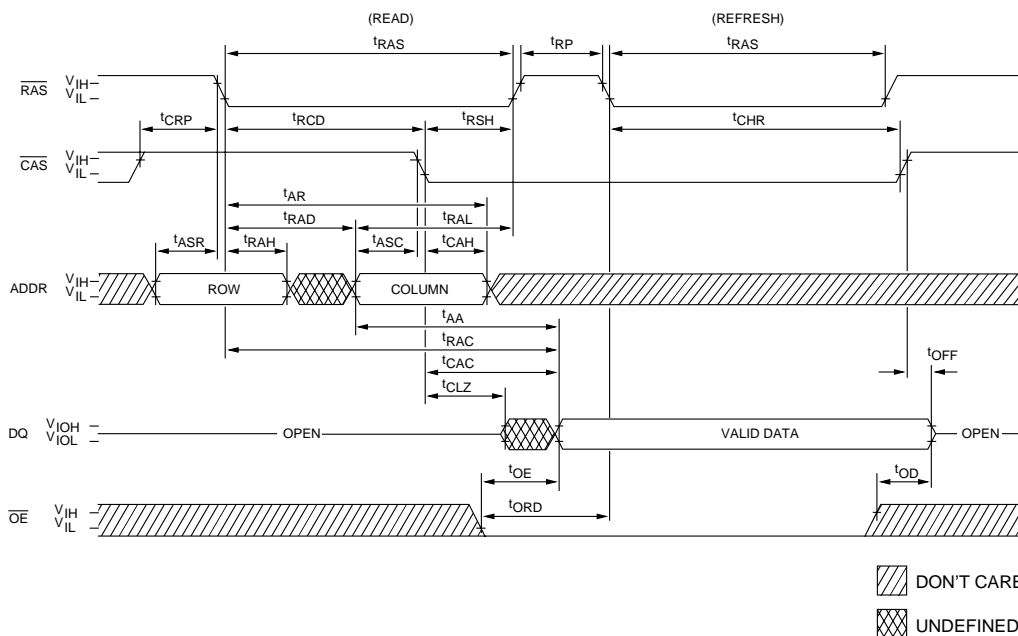
CBR REFRESH CYCLE
(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)



EXTENDED REFRESH CYCLE (MT4C4256 L ONLY)
(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)



HIDDEN REFRESH CYCLE ²⁴
(\overline{WE} = HIGH; \overline{OE} = LOW)

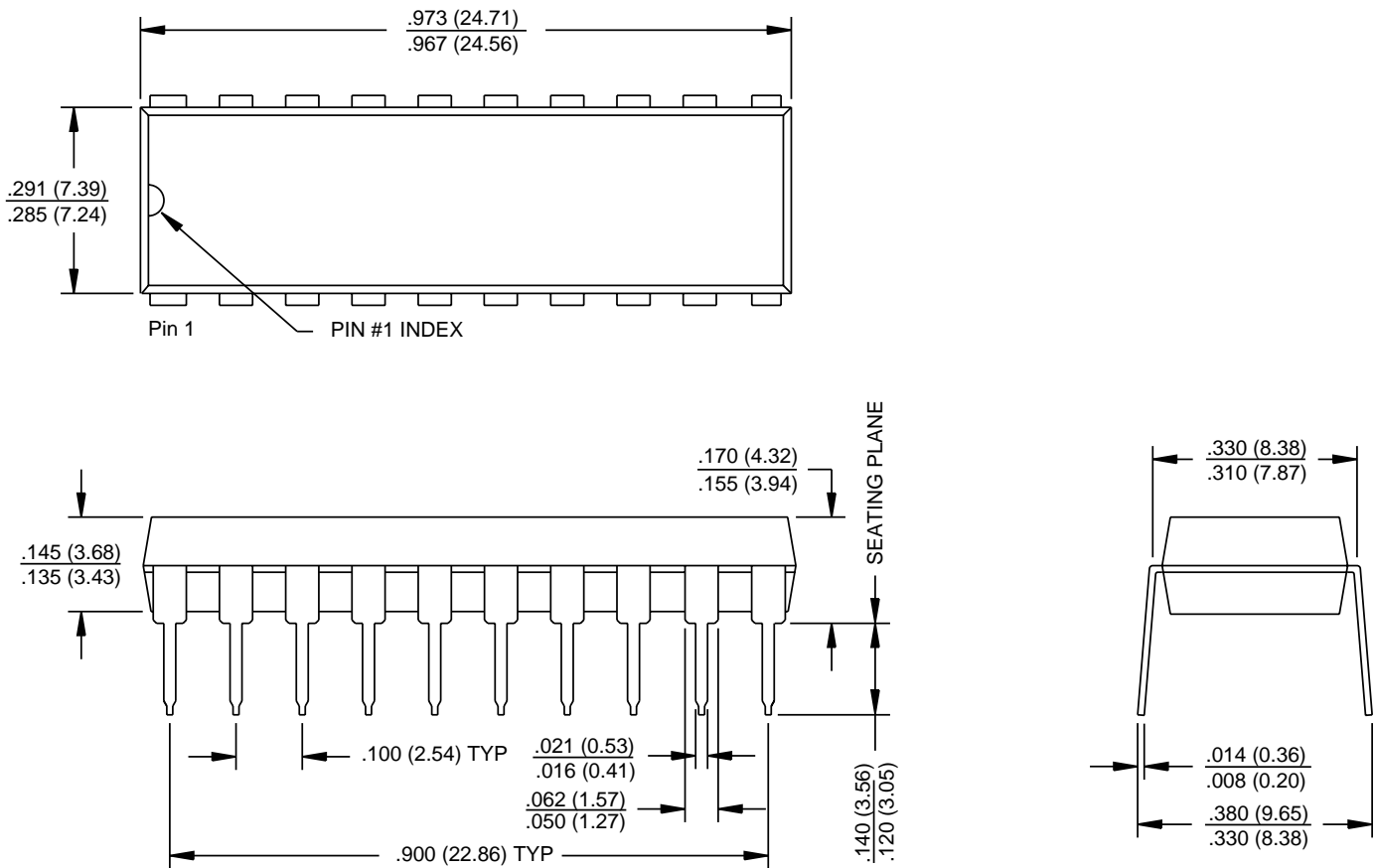


OBSOLETE



MT4C4256(L)
256K x 4 DRAM

20-PIN PLASTIC DIP (300 mil)



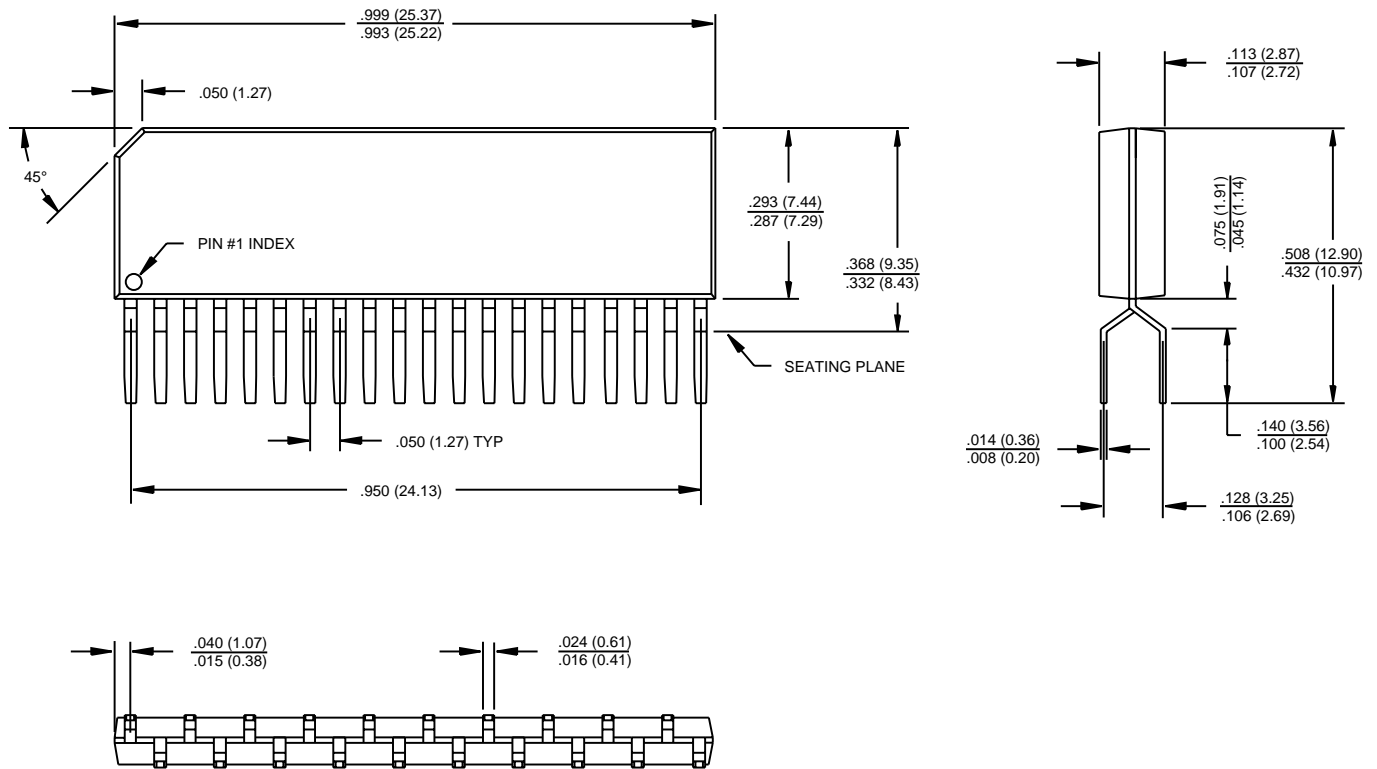
- NOTE:**
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

OBSOLETE

MICRON
SEMICONDUCTOR, INC.

MT4C4256(L)
256K x 4 DRAM

20-PIN PLASTIC ZIP (350 mil)



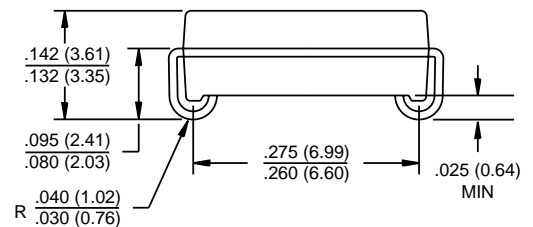
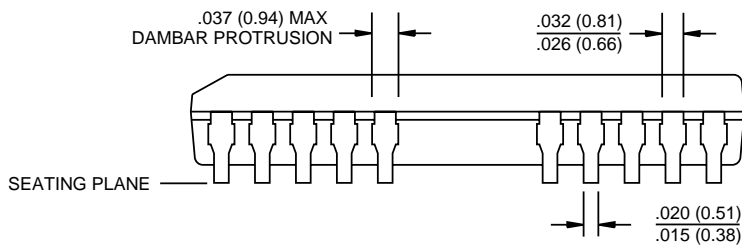
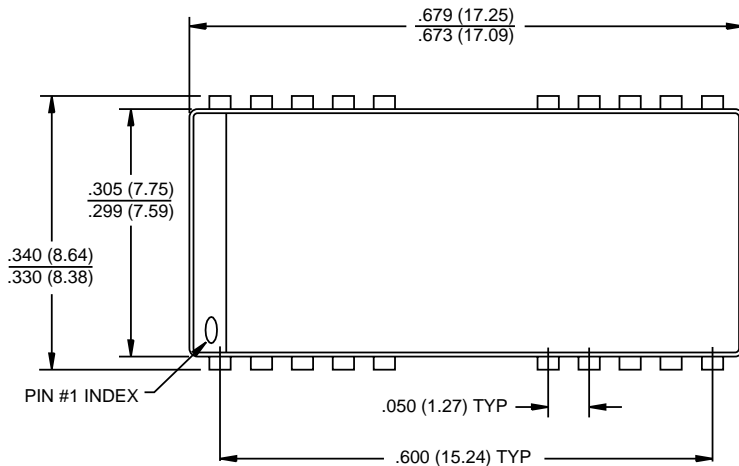
- NOTE:**
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

OBSOLETE

MICRON
SEMICONDUCTOR, INC.

MT4C4256(L)
256K x 4 DRAM

20/26-PIN PLASTIC SOJ (300 mil)



- NOTE:**
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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