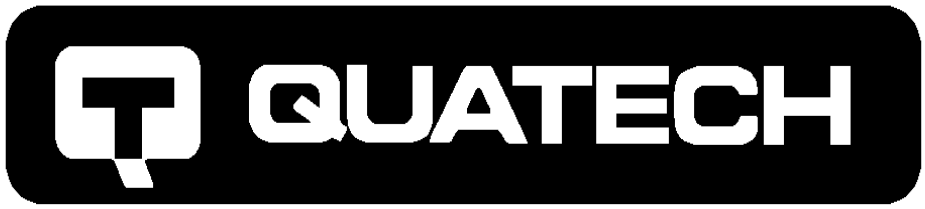

MPA-100
RS-232 SYNCHRONOUS ADAPTER

for ISA compatible machines

INTERFACE CARDS FOR IBM PC/AT AND PS/2

Hardware Reference Guide

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MODEL NUMBER: **MPA-100**

PRODUCT DESCRIPTION: **SINGLE CHANNEL RS-232-D SYNC. COMMUNICATIONS ADAPTER**

SERIAL NUMBER: _____

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Section INTRODUCTION

The Quatech MPA-100 is a single channel, synchronous RS-232 compatible serial communication port for systems utilizing the architecture of the IBM AT personal computer or compatible. The port of the MPA-100 occupies an 8 byte block of I/O address space. The base address of this block may be located anywhere within the available I/O address space in the system.

The MPA-100 is compatible with several serial communications controllers (SCC's). All of the available SCC's can support asynchronous formats, byte-oriented protocols such as IBM Bisync, and bit-oriented protocols such as HDLC and IBM SDLC. The SCC's also offer internal functions such as on-chip baud rate generators, and digital phase-lock loops (DPLL). Refer to the appendices for further information on the SCC being used.

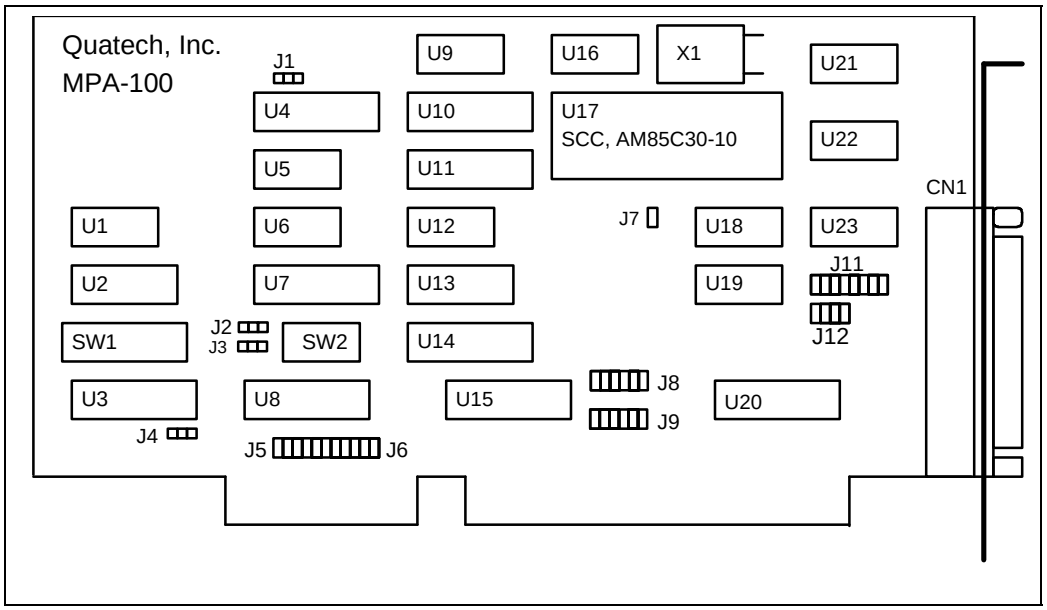
The MPA-100 also supports Direct Memory Access (DMA) and interrupts. DMA channels 1 - 3 can be used for high data transfer rates, while interrupt levels 2 - 7, 10 - 12, and 14 - 15 are available from several interrupt sources.

Section BOARD DESCRIPTION

The MPA-100 communications are controlled by the SCC labeled U17. There are eight jumper blocks on the MPA-100 that allow the user to select such options as bus speed, DMA channels, interrupt levels and driver control. External connections are made through a male D-25 connector labeled CN1 for both DTE and DCE configurations. These configurations are selected via onboard jumper blocks.

On the MPA-100, the driver circuitry consists of two RS-232 drivers and two RS-232 receivers.

Figure 1 MPA-100 board drawing



Section SCC GENERAL INFORMATION

The Serial Communications Controller (SCC) is a dual channel, multi-protocol data communications peripheral. The MPA-100 provides a single channel for communications, however, to provide full DMA capabilities with complete modem control line support, both channels of the SCC can be utilized. The SCC can be software configured to satisfy a wide variety of serial communications applications. Some of its protocol capabilities include:

1) Asynchronous Communications

- 5, 6, 7, or 8 bits per character
- 1, 1-1/2, or 2 stop bits
- Odd, even, or no parity
- Times 1, 16, 32, or 64 x clock modes
- Break generation and detection
- Parity, overrun and framing error detection

2) Byte-oriented Synchronous Communications

- Internal/external character synchronization
- 1 or 2 sync characters in separate registers
- Automatic Cyclic Redundancy Check (CRC) generation/detection

3) SDLC/HDLC (Bit Synchronous) Communications

- Abort sequence generation and checking
- Automatic zero insertion and deletion
- Automatic flag insertion between messages
- Address field recognition
- I-field residue handling
- CRC generation and detection
- SDLC loop mode with EOP recognition/loop entry and exit

4) NRZ, NRZI, or FM encoding/decoding

Accessing the registers

The mode of communication desired is established and monitored through the bit values of the internal read and write registers. The register set of the SCC includes 16 write registers and 9 read registers. These registers only occupy four address locations, which start at the MPA-100's physical base address that is configured via the on board switches. This and all other addresses are referenced from this base address in the form Base + Offset. An example of this is Base + 1 for the SCC Control Port, Channel A.

There are two register locations per SCC channel, a data port and a control port . Accessing the internal SCC registers is a two step process that requires loading a register pointer to perform the addressing to the correct data register. The first step is to write to the control port the operation and address for the appropriate channel. The second step is to either read data from or write data to the control port. The only exception to this rule is when accessing the transmit and receive data buffers. These registers can be accessed with the two step process described or with a single read or write to the data port. The following examples illustrate how to access the internal registers of the SCC. Also, Table 1 describes the read registers and Table 2 describes the write registers for each channel.

The MPA-100 has been designed to assure that all back to back access timing requirements of the SCC are met without the need for any software timing control. The standard of adding jmp $+2 between IO port accesses is not required when accessing the MPA-100.

Example 1: Enabling the transmitter on channel A.

```
mov     dx,base     ; load base address
add     dx,ContA    ; add control reg A offset (1)
mov     al,05H      ; write the register number
out     dx,al
mov     al,08H      ; write the data to the register
out     dx,al
```

Example 2: Monitoring the status of the transmit and receive buffers in RR0 of Channel A. Register 0 is addressed by default if no register number is written to WR0 first.

```
mov     dx,base     ; load base address
add     dx,ContA    ; add control reg A offset (1)
in      ax,dx       ; read the status
```

Example 3: Write data into the transmit buffer of channel A.

```
mov     dx,base     ; load base address
out     dx,al       ; write data in ax to buffer
```

Example 4: Read data from the receive buffer of channel A.

```
mov     dx,base     ; load base address
in      al,dx       ; write data in ax to buffer
```

Table SCC read register description.

RR0	Transmit, Receive buffer statuses and external status
RR1	Special Receive Condition status, residue codes, error conditions
RR2	Modified Channel B interrupt vector and Unmodified Channel A interrupt vector
RR3	Interrupt Pending bits
RR6	LSB of frame byte count register
RR7	MSB of frame byte count and FIFO status register
RR8	Receive buffer
RR10	Miscellaneous status parameters
RR12	Lower byte of baud rate time constant
RR13	Upper byte of baud rate time constant
RR15	External/Status interrupt information

The SCC can perform three basic forms of I/O operations: polling, interrupts, and block transfer. Polling transfers data, without interrupts, by reading the status of RR0 and then reading or writing data to the SCC buffers via CPU port accesses. Interrupts on the SCC can be sourced from the receiver, the transmitter, or External/Status conditions. At the event of an interrupt, Status can be determined, then data can be written to or read from the SCC via CPU port accesses. For block transfer mode, DMA transfers accomplish data transfers from the SCC to memory or from memory to the SCC, interrupting the CPU only when the Block is finished. Further information on these subjects are found in Section 6 Interrupts, and Section 7 Direct Memory Access.

The SCC incorporates additional circuitry supporting serial communications. This circuitry includes clocking options, baud rate generator (BRG), data encoding, and internal loopback. The SCC may be programmed to select one of several sources to provide the transmit and receive clocks. These clocks can be programmed in WR11 to come from the RTXC pin, the TRXC pin, the output of the BRG, or the transmit output

of the DPLL. The MPA-100 uses the TRXC pin for its clock-on-transmit and the RTXC pin for its clock-on-receive. Programming of the clocks should be done before enabling the receiver, transmitter, BRG, or DPLL.

Table SCC write register description.

WR0	Command Register, Register Pointer, CRC initialization, resets for various modes
WR1	Interrupt control, Wait/DMA request control
WR2	Interrupt vector
WR3	Receiver initialization and control
WR4	Transmit/Receive miscellaneous parameters and codes, clock rate, stop bits, parity
WR5	Transmitter initialization and control
WR6	Sync character (1st byte) or SDLC address field
WR7	Sync character (2nd byte) or SDLC Flag
WR7'	Special HDLC Enhancement Register
WR8	Transmit buffer
WR9	Master interrupt control and reset
WR10	Miscellaneous transmitter/receiver control bits, NRZI, NRZ, FM coding, CRC reset
WR11	Clock mode and source control
WR12	Lower byte of baud rate time constant
WR13	Lower byte of baud rate time constant
WR14	Miscellaneous control bits: baud rate generator, DPLL control, auto echo
WR15	External/Status interrupt control

For a complete information regarding the SCC registers please refer to the manufacturer's technical manual for the specific part being used.

Baud Rate Generator Programming

The baud rate generator (hereafter referred to as the BRG) of the SCC consists of a 16-bit down counter, two 8-bit time constant registers, and an output divide-by-two. The time constant for the BRG is programmed into WR12 (least significant byte) and WR13 (most significant byte). The equation relating the baud rate to the time constant is given below while Table 3 shows the time constants associated with a number of popular baud rates when using the standard MPA-100 9.8304 MHz clock.

$$Baud\_Const = \frac{Clock\_Frequency}{2 * Buad\_Rate * Clock\_Mode} -$$

Where:

Clock_Frequency = crystal frequency of 9.8304MHz

Clock_Mode = value programmed in WR4

Baud_Rate = desired baud rate

Table Time constants for common baud rates

Baud Rate	Baud Constant (Hex)
38400	007EH
19200	00FEH
9600	01FEH
4800	03FEH
2400	07FEH
1200	0FFEH
600	1FFEH
300	3FFEH

(for 9.8304 Mhz Clock)

SCC Data Encoding Methods

The SCC provides four different data encoding methods, selected by bits D6 and D5 in WR10. These four include NRZ, NRZI, FM1 and FM0. The SCC also features a digital phase-locked loop (DPLL) that can be programmed to operate in NRZI or FM modes. Also, the SCC contains two features for diagnostic purposes, controlled by bits in WR14. They are local loopback and auto echo.

For further information on these subjects or any others involving the SCC contact the manufacturer of the SCC being used for a complete technical manual.

Section JUMPER BLOCK CONFIGURATIONS

The MPA-100 utilizes seven user-selectable jumper blocks (labeled J1, J3-J9), that allow the user much flexibility when configuring the board. The following section explains the function and setting of each of the jumper blocks on the MPA-100.

J1 8/6 MHz bus Speed configuration Jumper

J1 is a 3 position jumper that configures timing to the SCC for a system bus speed of either 8 MHz or 6 MHz. The board is configured from the factory for a 8 Mhz bus timing.

Table Jumper J1 Selections

Bus Speed	Jumper J1
8 Mhz	1-2
6 Mhz	3-4

J2, J11, and J12 DTE/DCE Configuration Jumpers

The jumper groups J2, J11, and J12 control the DTE/DCE configuration of the MPA-100. The jumper J1 controls important clock characteristics. The jumpers J11 and J12 control the routing of the signals to the DB-25 connector. All three jumper groups must be set exclusively to either DTE fo DCE for correct operation of the MPA=100.

Table Jumper J2 Selections

Board Configuration	Jumper J2
DTE	In
DCE	Out

Table Jumper Block J11 Selections

Board Configuration	Pins
DTE	1-9, 2-10, 3-11, 4-12, 5-13, 6-14, 7-15, 8-16
DCE	1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16

Table Jumper Block J12 Selections

Board Configuration	Pins
DTE	1-5, 2-6, 3-7, 4-8
DCE	1-2, 3-4, 5-6, 7-8

J11 and J12 may be configured for DTE by setting all jumpers vertical on the board and for DCE by setting all jumpers horizontal on the board.

J4 - INTERRUPT CONFIGURATION

J4 is a three pin jumper which determines the configuration for the interrupts. By selecting pins 1 & 2, the user has the ability to share interrupts. The MPA-100 will drive the interrupt onto the bus only when an interrupt occurs. Otherwise, the output is high impedance. If pins 2 & 3 of J1 are selected, then interrupts abide by the IBM specification and cannot be shared. Table 8 summarizes the jumper block selections for J4

Table Jumper Block J4 Selections

Interrupt Function	Pins
Interrupt Sharing	1-2
No Interrupt sharing	2-3

J5 & J6 - INTERRUPT LEVEL SELECTION

Jumper blocks J5 and J6 select the interrupt level that the MPA-100 utilizes. Interrupt levels IRQ2 - IRQ7 reside on J5, while interrupt levels IRQ10 - IRQ12 and IRQ14 - IRQ15 reside on J6. Tables 9 and 10 summarize the jumper block selections for J5 and J6. The IRQ levels are also marked on the MPA-100 silkscreen for easy identification.

Table Jumper block J5 selections.

Interrupt Level	Pins
IRQ2(9)	1-7
IRQ3	2-8
IRQ4	3-9
IRQ5	4-10
IRQ6	5-11
IRQ7	6-12

Table Jumper block J6 selections.

Interrupt Level	Pins
IRQ10	1-6
IRQ11	2-7
IRQ12	3-8
IRQ14	4-9
IRQ15	5-10

J8- DMA CHANNEL ON TRANSMIT SELECTION

J8 Selects the DMA channel to be used for DMA on transmit. Three channels (1 - 3) are available on the MPA-100 for DMA. When selecting a DMA channel, both the DMA acknowledge (DACK) and the DMA request (DRQ) for the appropriate channel need to be selected. Table 11 summarizes the jumper block selections for J8.

Table Jumper block J8 selections.

DMA Channel	Pins
Channel 1	1-7 2-8
Channel 2	3-9 4-10
Channel 3	5-11 6-12

J9 - DMA CHANNEL ON RECEIVE SELECTION

J9 selects the DMA channel to be used for DMA on receive. Threechannels (1 - 3) are available on the MPA-100 for DMA. When selecting a DMA channel, both the DMA acknowledge (DACK) and the DMA request (DRQ) for the appropriate channel need to be selected. Table 12 summarizes the jumper block selections for J9.

Table Jumper block J9 selections.

DMA Channel	Pins
Channel 1	1-7
	2-8
Channel 2	3-9
	4-10
Channel 3	5-11
	6-12

NOTE:
Since it is illegal to perform DMA on transmit and receive on the same DMA channel, jumper blocks J7 and J8 should never have the same pins connected. This could result in damage to the system.

J7 SYNCA to RLEN control

J7 controls the signal path from the RLEN bit in the Communications register to the SYNCA input to the SCC. If J7 is installed the RLEN bit may be used to control the SYNCA pin when the SCC is in external SYNC mode. Note: the RLEN output is still effected when used to control the SYNCA pin.

Table Jumper J7 Selections

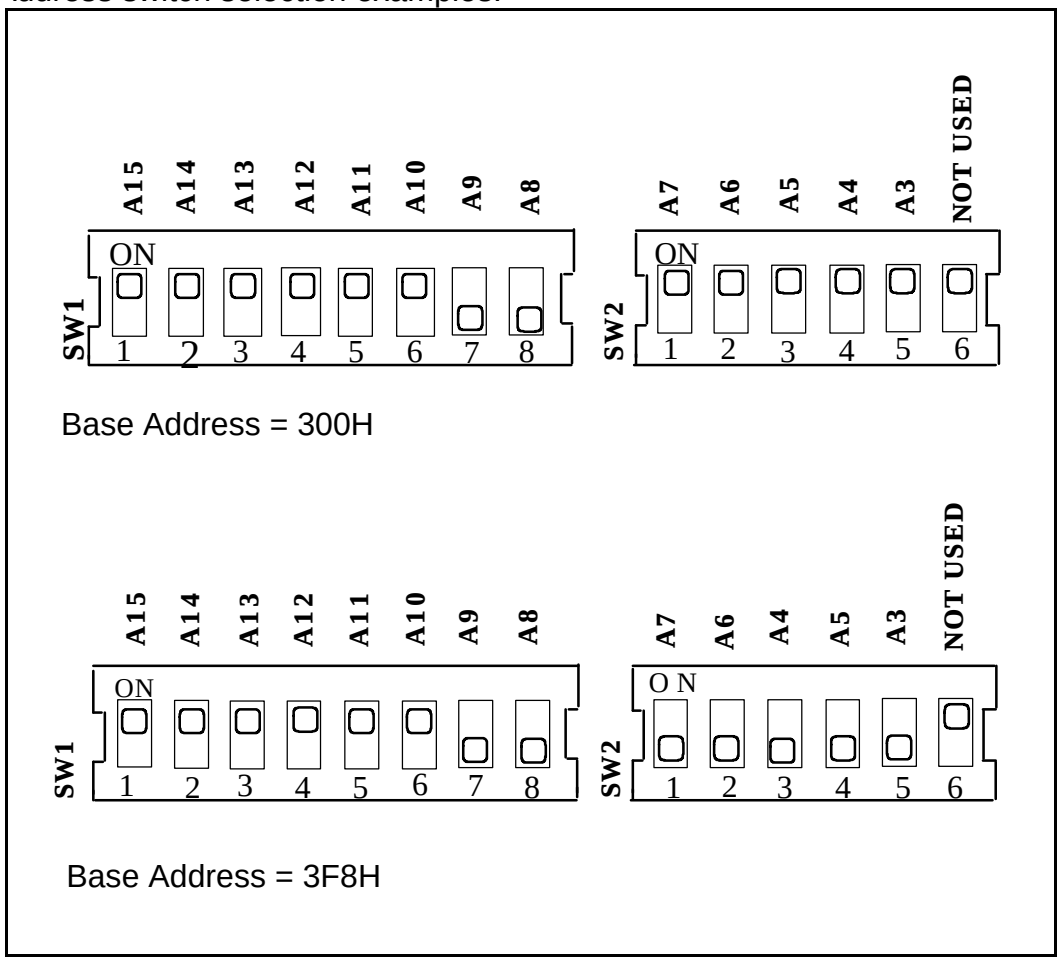
Function	Jumper J1
SYNCA	IN
RLEN	OUT

Section ADDRESSING

The MPA-100 occupies a continuous 8 byte block of I/O addresses. For example, if the base address is set to 300H, then the MPA-100 will occupy address locations 300H-307H. The base address of the MPA-100 may be set to any of the first 64 Kbytes (0 - FFFFH) of available I/O address space through the settings of dip switches SW1 and

SW2. SW1 allows the user to select the higher address signals A15 - A8. SW2 allows the user to select the lower address signals A7 - A3. The sixth position of SW2 is not used and can be ignored. Figure 2 shows some examples of different base addresses.

Figure Address switch selection examples.



The first four bytes, Base+0 through Base+3, of address space on the MPA-100 contain the internal registers of the SCC. The next two locations Base+4 and Base+5 contain the communications register and the configuration register. The last two address port locations are reserved for future use. The entire address range of the MPA-100 is shown in Table 14.

Table MPA-100 Address Assignments

Address	Register Description
Base + 0	SCC Data Port, Channel A
Base + 1	SCC Control Port, Channel A
Base + 2	SCC Data Port, Channel B
Base + 3	SCC Control Port, Channel B
Base + 4	Communications Register
Base + 5	Configuration Register
Base + 6	Reserved
Base + 7	Reserved

Information on the internal registers of the SCC can be found in Section III SCC General Information. The two on-board registers give the user additional options pertaining to DMA, interrupts and the RS-232-D standard for communication. Information on the configuration register and the communications register can be found in Section 7, Configuration Register and Section 9, Communications.

Section INTERRUPTS

The MPA-100 supports eleven interrupt levels: IRQ2 -7, IRQ10 - 12, and IRQ14 - 15. The interrupt level is selected through jumper blocks J5 and J6. The interrupt source is selected by bits D4 and D5 of the configuration register. The MPA-100 has three interrupt sources: interrupt on terminal count, interrupt on test mode, and interrupt from the SCC. Interrupts from the SCC can occur on a number of conditions, depending on which is programmed. These include interrupt on next character received, interrupt on all characters received, interrupt on special condition, interrupt on transmit buffer empty, and interrupt on External/Status (see manufacturers data sheets for more details). Jumper block J4 can be selected to provide for interrupt sharing on the MPA-100.

When using interrupts with the MPA-100, it is required that the applications program have an interrpt service routine (ISR). There are several things that an ISR must do to allow proper system operaion:

1. Do a software interrupt acknowledge to the SCC. This is accomplished by reading the interrupt vector register, status register 2, in channel B of the SCC. The value supplied by this read can also be used to vector to the appropriate part of the ISR.
2. Service the interrupt, IE, read the receiver buffer, write to the transmit buffer etc.
3. Write a Reset Highest Interrupt Under Service (IUS) to the SCC. This is done by writing a 0x38 to the SCC command register.
4. Check for any additional interrutps pending in the SCC and service them.
5. For applications running under DOS, a non-specific End of Interrupt must be submitted to the interrupt controller. For Interrupts 2-7 this is done by writing a 0x20 to port 0x20. For Interrupts 10-12,14 and 15 this is done by writing a 0x20 to 0x60, then a 0x20 to 0x20 (Due to the interrupt controllers being cascaded). Note that this should only be done if it is a requirement of the operating system being used.

For further information on these subjects or any others involving the SCC contact the manufacturer of the SCC being used for a complete technical manual.

Section DIRECT MEMORY ACCESS

Direct Memory Access (DMA) is a way of directly transferring data to and from memory, resulting in high data transfer rates with very low CPU overhead. The MPA-100 provides for DMA transfers on three different DMA channels (1 - 3) which are selected through jumper blocks J6 and J7. Three DMA sources are merged into two DMA request lines (DMATRQ and DMARRQ) on the MPA-100 for simultaneous DMA transfers on two channels. The sources for these requests originate from the SCC and can be programmed for a variety of DMA modes. These modes include DMA request on transmit, DMA request on receive, and DMA request on both transmit and receive.

For DMA request on transmit, the DMA controller should be programmed first for an 8 bit read transfer on the desired channel, but not yet enabled. Then the SCC should be programmed for DMA request on transmit on the desired DMA source. The sources DMA request on transmit are either the W/REQA pin (pin 10) of channel A or the DTR/REQA pin (pin 16) of channel A. The source is then determined by bit D0 of the configuration register. The DTR/REQA pin should only be used for DMA transfers if the user is not strictly adhering to the EIA-530 standard. EIA-530 requires that this pin is used as the Data Terminal Ready (DTR) line and would not be available for DMA. After programming the SCC for DMA , The DMA on the MPA-100 should be enabled by setting bit D2 of the configuration register. Next, the DMA on the SCC should be enabled, and finally, the DMA channel should be unmasked. The DMA controller will write the data in memory to the SCC. When the transmit buffer of the SCC becomes empty, a DMA request will be generated and the data will be transferred.

For DMA request on receive, the DMA controller should be programmed first for an 8 bit write transfer on the desired channel, but not yet enabled. Next, the SCC should be programmed for DMA request on receive on the desired DMA source. The two sources for DMA request on receive are either the W/REQA pin (pin 10) of channel A or the W/REQB pin (pin 30) of channel B. The source is then determined by bit D1 on the configuration register. After programming the SCC for DMA (see appendix for further details), one should enable the DMA on the MPA-100 by setting bit D3 of the configuration register. Then, the DMA on the SCC should be enabled, and finally the DMA controller should be enabled. When a character enters the receive buffer of the SCC, a DMA request is generated. The DMA controller then writes the data from the SCC into memory.

Programming for DMA request on both transmit and receive is simply a combination of the two. There are three possible configurations

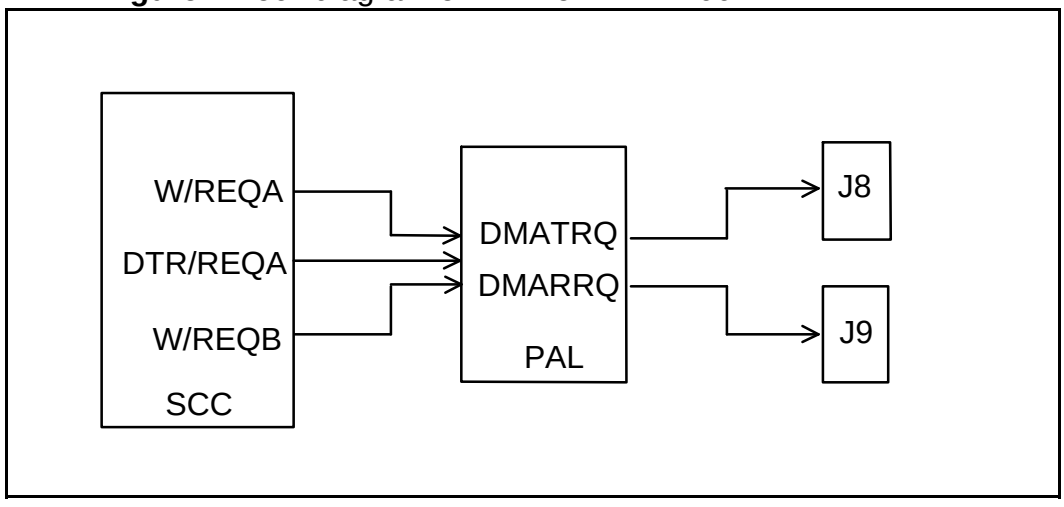
that can be used, depending on the sources selected. The first configuration available uses the W/REQA pin of channel A for DMA request on receive, and the DTR/REQA pin of channel A for DMA request on transmit. This is done by setting bit D0 and clearing bit D1 of the configuration register. The second configuration uses the DTR/REQA pin for DMA request on transmit, and the W/REQB pin for DMA request on receive. This is done by setting both D0 and D1 of the configuration register. The third configuration uses the W/REQA pin of channel A for DMA request on transmit, and the W/REQB pin of channel B for DMA request on receive. This is done by clearing bit D0 and setting bit D1 of the configuration register. Figure 3 shows a block diagram of the DMA circuitry on the MPA-100.

When using the channel A DTR/REQ pin for transmit DMA the SCC must be programmed so that the request release timing of this pin is identical to the WAIT/REQ timing. This is done by setting bit D4 of write register 7 prime.

NOTE:

Even though the W/REQA pin can be used for both DMA request on transmit and receive, obviously it cannot be used for both simultaneously. Therefore, bits D0 and D1 of the configuration register should never be cleared at the same time while bits D2 and D3 are both set. This situation may result in damage to the system.

Figure Block diagram of DMA on MPA-100.



Section CONFIGURATION REGISTER

The MPA-100 is equipped with an on-board register used for configuring the board. This register includes such information as DMA enables and sources, along with interrupt enables and sources. Below is a detailed description of the configuration register. The address of this register is Base+5. Table 15 details the bit definitions of the configuration register.

Table Configuration Register - Read/Write

D7	D6	D5	D4	D3	D2	D1	D0
0	0	INTS1	INTS0	DMREN	DMTEN	RXSRC	TXSRC

D7-D6 Reserved, always 0.

D5-D4 - INTS1, INTS0, INTERRUPT SOURCE AND ENABLE BITS:

These two bits determine the source of the interrupt. The three sources are interrupt on terminal count (INTTC), interrupt from the SCC (INTSCC), and interrupt on Test Mode (INTTM). When the source is set, that interrupt becomes enabled. Below is the mapping for these bits.

INTS1	INTS0	Interrupt
0	0	Interrupts Disabled
0	1	INTTC
1	0	INTSCC
1	1	INTTM

D3 -DMREN, DMA ON RECEIVE ENABLE:

When set (logic 1), this bit enables the DMA on receive on the MPA-100.

D2 -DMTEN, DMA ON TRANSMIT ENABLE:

When set (logic 1), this bit enables the DMA on transmit on the MPA-100.

D1 -RXSRC, DMA ON RECEIVE SOURCE:

When set (logic 1), this bit allows the source for DMA on receive to come from the W/REQB pin of channel B on the SCC. When cleared (logic 0), the source for DMA on receive comes from the W/REQA pin of channel A on the SCC.

D0 -TXSRC, DMA ON TRANSMIT SOURCE:

When set (logic 1), this bit allows the source for DMA on transmit to come from the DTR/REQA pin of channel A on the SCC. When cleared (logic 0), the source for DMA on transmit comes from the W/REQA pin of channel A of the SCC.

Section COMMUNICATIONS

The MPA-100 is equipped with an on-board communications register which gives the user options pertaining to the clocks and testing. The user can specify the source and type of clock to be transmitted or received. Test mode bits pertain only to the DTE versions and can be ignored if using a DCE configured MPA-100. The address of this register is Base+4. Table 16 and the descriptions that follow detail the communications register.

NOTE:
The Local Loopback Test and the Remote Loopback Test cannot be performed simultaneously. Thus, bits D5 and D4 of the communications register should not be set (logic 1) simultaneously.

Table cOMMUNICATIONS Register - Read/Write

D7	D6	D5	D4	D3	D2	D1	D0
TM ST	0	LLEN	RLEN	RCKEN	TCKEN	0	0

D7 -TEST MODE STATUS:

This bit can read the status of the Test Mode signal on a DTE, allowing the user to monitor this signal without generating any interrupts.

D6 - Reserved, always 0.

D5 -LOCAL LOOPBACK ENABLE:

When set (logic 1), this bit allows the DTE to test the functioning of the DTE/DCE interface and the transmit and receive sections of the local DCE. When cleared (logic 0), no testing occurs. This can also be used as a general purpose output.

D4 -REMOTE LOOPBACK ENABLE:

When set (logic 1), this bit allows the DTE to test the transmission path up to and through the remote DCE to the DTE interface and the similar return transmission path. When cleared (logic 0), no testing occurs. If jumper J7 is in place the Remote Loopback is also used to control the Sync input of the

Channel A data receiver. This is useful in situations where it is desired to receive unformatted serial data.

D3 -RECEIVE CLOCK ENABLE (DCE only):

When set (logic 1), this bit allows the DCE to transmit its clock-on-receive (RCLK). When cleared (logic 0), the DCE receives its RCLK. Since a DTE can only receive its RCLK, writing to this bit has no effect on a DTE.

D2 -TRANSMIT CLOCK ENABLE (DTE only):

When set (logic 1), this bit allows the DTE to transmit its clock-on-transmit (TCLK). When cleared (logic 0), the DTE receives its TCLK. Since a DCE can only transmit its TCLK, writing to this bit has no effect on a DCE.

D1 -RECEIVER ENABLE:

This bit should always be programmed to 0.

D0 -TRANSMITTER ENABLE:

This bit should always be programmed to 0.

Section DTE / DCE Configuration Differences

The MPA-100 can beconfigured as either a Data Terminal Equipment (DTE) or a Data Communications Equipment (DCE) configuration.

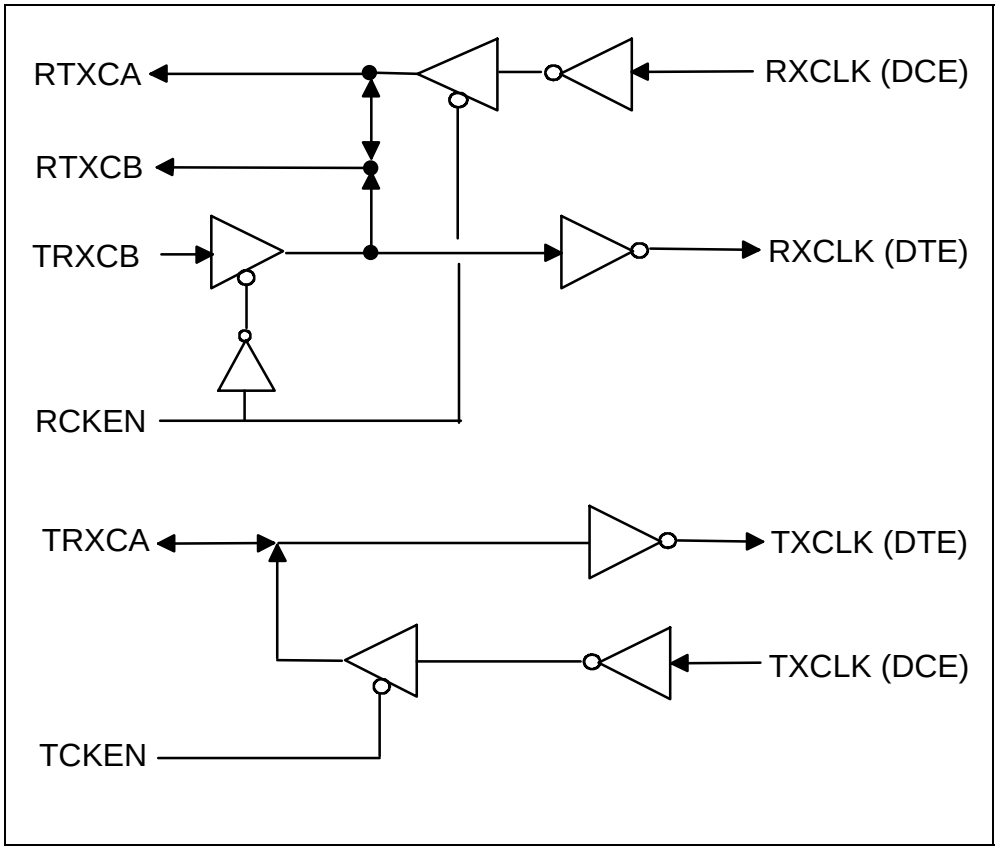
The differences on the MPA-100 between the DTE and the DCE configuration include signal definitions, connector pinout, and clocking options. In order to simplify matters, a section for each configuration summarizes these differences.

DTE CONFIGURATION

The MPA-100 is configured as a DTE by the correct configuration of jumper blocks J2, J11 and J12. See Section 4, Tables 5,6 and 7 (pages 9 and 10) for this configuration information.

The control signals the DTE can generate are the Request To Send (RTS) and Data Terminal Ready (DTR). It can receive the signals Carrier Detect (CD), Clear to Send (CTS), and Data Set Ready (DSR). All the control signals are controlled through channel A of the SCC, with the exception of the DSR signal, which is received on the DCDB pin (pin 21) on channel B. Thus CD is an output for the DTE configuration.

Figure DTE Clock Configuration



The DTE can transmit its clock-on-transmit (TCLK) from the TRXCA pin (pin 14) on channel A of the SCC, receive its TCLK on the same pin (depending on bit D2 of the communications register), or receive its clock-on-receive (RCLK) on the RTXC pins (pin 12 & 28) on channels A & B of the SCC. As per the EIA-232D specification, the DTE can not transmit its receive clock. For clarity, the DTE clock configuration is shown in Figure 4.

The testing signals the DTE can generate are the Local Loopback Test (LL) and the Remote Loopback Test (RL). These signals are

generated from the on-board communications register. When a Test Mode (TM) condition is received, an interrupt can be generated on the DTE. Table 13 summarizes the signals on the DTE.

Table DTE Signals

Signal	Received	Generated	SCC Pin or Register Bit
RTS		X	RTSA pin of SCC
CTS	X		CTSA pin of SCC
DTR		X	DTR/REQ of SCC
DSR	X		DCDB pin of SCC
CD	X		DCDA pin of SCC
TxCLK	X	X	TRXCA pin of SCC
RxCLK	X		RTXC pin of SCC
LL		X	Bit D5 of Comm. Reg
RL		X	Bit D4 of Comm Reg
TM	X		INTM or Bit D7 of Comm Reg

DCE CONFIGURATION

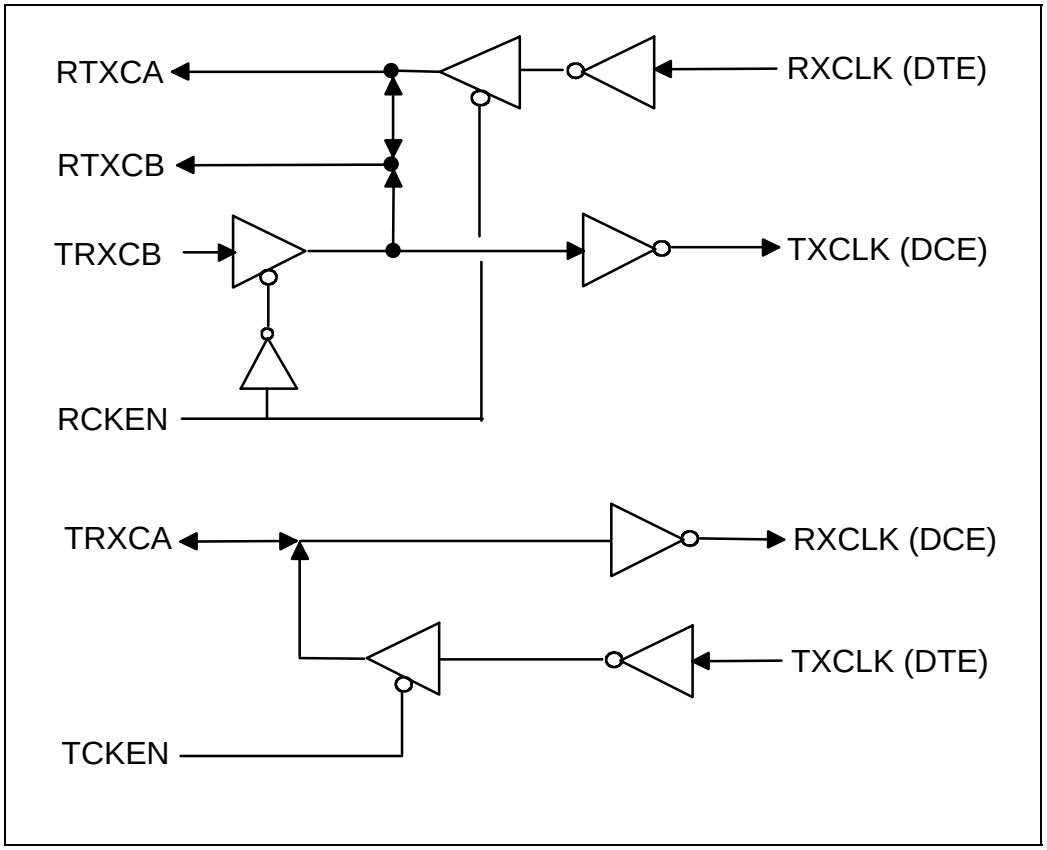
The MPA-100 is configured as a DCE by the correct configuration of jumper blocks J2, J11 and J12. See Section 4, Tables 5,6, and 7 (pages 9 and 10) for this configuration information. It is noted that because the connector used for the DCE configuration is the same as that used for the DTE configuration the MPA-100 does not have a true DCE implimentation. However, the pinout is correct for a one to one wired connection with a DTE.

The RS-232C standard defines each signal with respect to the DTE. These signals still have the same representation for the DCE. The difference on the MPA-100 is that the names given to each of the signals on the DCE connector are interchanged (by jumper blocks J8 and J9), with the exception of a few control signals. For example, pin 2 of the DCE connector is received data, yet the signal is on the transmitted data line.

The control signals the DCE can generate are the Clear to Send (CTS), Carrier Detect (CD), and DCE Ready (DSR). It can receive the signals DTE Ready (DTR) and Ready to Send (RTS). All the control signals are interchanged and controlled through channel A of the SCC, with the exception of the CD signal, which is generated from the DTR/REQB pin (pin 24) on channel B. Thus CD is an input for the DCE configuration.

The DCE can transmit its clock-on-transmit, TxCLK (DCE) from the TRXCB pin (pin 26) on channel B of the SCC, and transmit its clock-on-receive, RxCLK (DCE) from the TRXCA pin (pin 14) on channel B of the SCC(depending on bit D3 of the communications register. Also, it can receive its clock-on-receive, TxCLK (DTE), on RTXCA and RTXCB (pins 12 and 28). As per the EIA-232D specification, the DCE can not receive it's transmit clock. For Clarity, the DCE clock configuration is shown in Figure 5.

Figure DCE Clock Configuration



The test mode signals for the DCE configuration are the same for the DCE and DTE configurations. These signals are Local Loopback (LLBK) and Remote Loopback (RLBK) for outputs and Test Mode (TM) forinput. These signals also remain on the same connector pins.

Table DCE Signals

Signal	Received	Generated	SCC Pin or Register Bit
RTS	X		CTSA pin of SCC
CTS		X	RTSA pin of SCC
DTR	X		DCDA of SCC
DCR		X	DTR/REQA pin of SCC
CD		X	DTR/REQB pin of SCC
TxCLK		X	TRXCA pin of SCC
RxCLK	X	X	RTXC/TRXCB pin of SCC
LL		X	Bit D5 of Comm. Reg
RL		X	Bit D4 of Comm Reg
TM	X		INTM or Bit D7 of Comm Reg

Section EXTERNAL CONNECTIONS

The MPA-100 is designed to meet the RS-232 standard through a D-25 connector. The MPA-100 uses a D-25 short body male connector (labeled CN1) for both the DTE and DCE configurations. Jumper blocks J2, J11, and J12 configure the connector pinout for the desired configuration. Table 19 defines the pinout definitions for both configurations and Figures 6 and 7 illustrate the pin-outs for each of the configurations. The definitions of the interchange circuits according to the RS-232-D standard can be found in Appendix 1, on page 31.

Table Connector Pin Definitions

Pin	DTE	Circuit	DCE	Circuit
1	CGND	-	CGND	-
2	TXD	BA	RXD	BB
3	RXD	BB	TXD	BA
4	RTS	CA	CTS	CB
5	CTS	CB	RTS	CA
6	DSR	CC	DTR	CD
7	DGND	AB	DGND	AB
8	CD (IN)	CF	CD (OUT)	CF
9	N/C		N/C	
10	N/C		N/C	
11	RXCLK (DTE)		RXCLK (DTE)	
12	N/C		N/C	
13	N/C		N/C	
14	N/C		N/C	
15	TXCLK (DCE)	DB	TXCLK (DCE)	DB
16	N/C		N/C	
17	RXCLK (DCE)	DD	RXCLK (DCE)	DD
18	LLBK	LL	LLBK	LL
19	N/C		N/C	
20	DTR	CD	DSR	CC
21	RLBK	RL	RLBK	RL
22	N/C		N/C	
23	N/C		N/C	
24	TXCLK (DTE)	DA	TXCLK (DTE)	DA
25	TEST MODE	TM	TEST MODE	TM

Figure MPA-100 DTE Output Connector Configuration

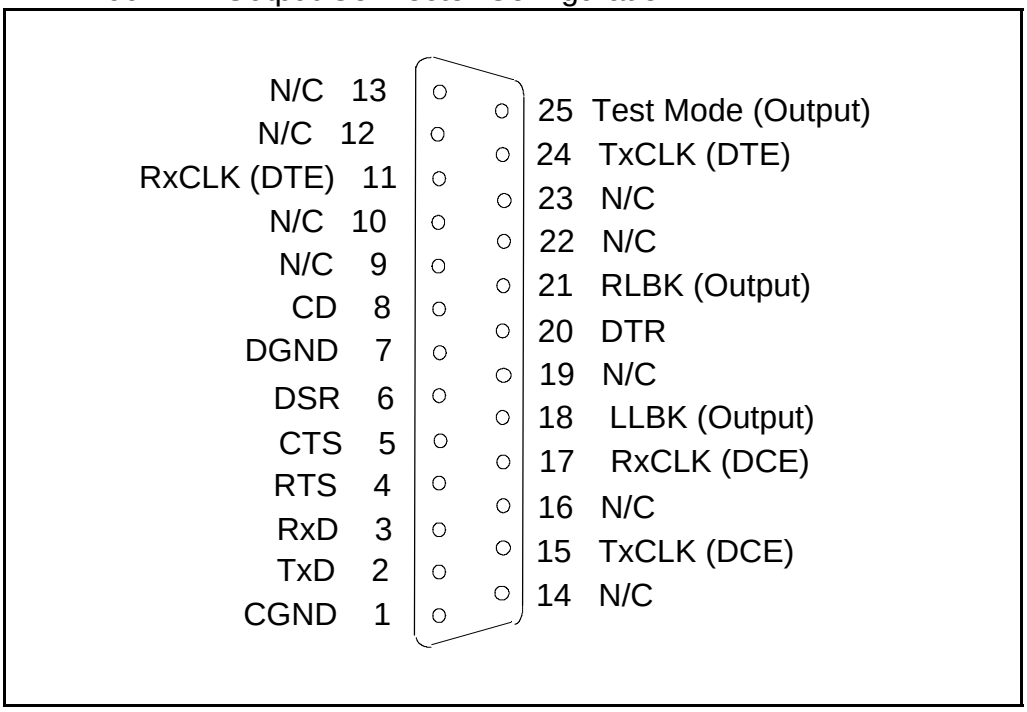
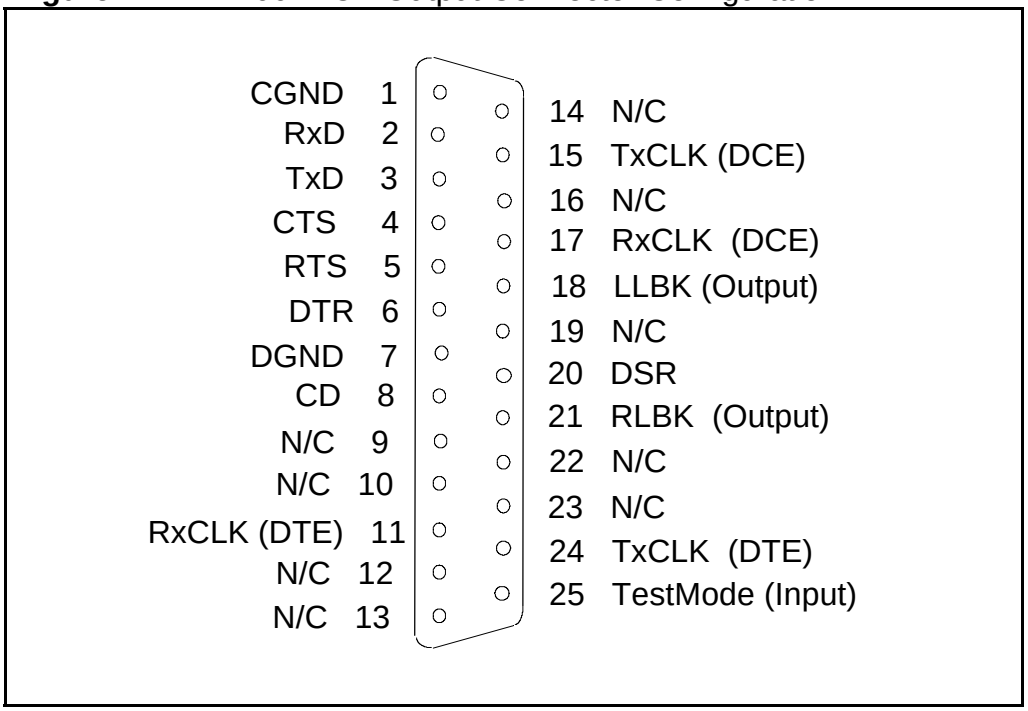


Figure MPA -100 DCE Output Connector Configuration



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Appendix Definition of Interface Signals

CIRCUIT AB - SIGNAL GROUND

- CONNECTOR NOTATION: DGND
- DIRECTION: Not applicable

This conductor directly connects the DTE circuit ground to the DCE circuit ground.

CIRCUIT CC - DCE Ready (Data Set READY)

- CONNECTOR NOTATION: DSR
- DIRECTION: From DCE

This signal indicates the status of the local DCE by reporting to the DTE device that a communication channel has been established.

CIRCUIT BA - TRANSMITTED DATA

- CONNECTOR NOTATION: TXD
- DIRECTION: To DCE

This signal transfers the data generated by the DTE through the communication channel to one or more remote DCE data stations.

CIRCUIT BB - RECEIVED DATA

- CONNECTOR NOTATION: RXD
- DIRECTION: From DCE

This signal transfers the data generated by the DCE, in response to data channel line signals received from a remote DTE data station, to the DTE.

CIRCUIT DA - TRANSMIT Signal ELEMENT TIMING (TxCLK- DTE Source)

CONNECTOR NOTATION: TXCLK (DTE)

DIRECTION: To DCE

This signal, generated by the DTE, provides the DCE with element timing information pertaining to the data transmitted by the DTE. The DCE can use this information for its received data.

CIRCUIT DB - TRANSMIT Signal ELEMENT TIMING (TxClk - DCE Source)

- CONNECTOR NOTATION:TXCLK (DCE)
- DIRECTION: From DCE

This signal, generated by the DCE, provides the DTE with element timing information pertaining to the data transmitted to the DCE. The DCE can use this information for its received data.

CIRCUIT DD - RECEIVER Signal ELEMENT TIMING (RxClk - DCE Source)

- CONNECTOR NOTATION: RXCLK (DCE)
- DIRECTION: From DCE

This signal, generated by the DCE, provides the DTE with element timing information pertaining to the data transmitted by the DCE. The DTE can use this information for its received data.

CIRCUIT CA - REQUEST TO SEND

- CONNECTOR NOTATION: RTS
- DIRECTION: To DCE

This signal controls the data channel transmit function of the local DCE and, on a half-duplex channel, the direction of the data transmission of the local DCE.

CIRCUIT CB - CLEAR TO SEND

- CONNECTOR NOTATION: CTS
- DIRECTION: From DCE

This signal indicates to the DTE whether the DCE is conditioned to transmit data on the communication channel.

CIRCUIT CF - Received Line Signal Detector (CARRIER DETECT)

- CONNECTOR NOTATION: CD
- DIRECTION: From DCE

This signal indicates to the DTE whether the DCE is conditioned to receive data from the communication channel, but does not indicate the relative quality of the data signals being received.

CIRCUIT CD - DTE READY (Data Terminal Ready)

- CONNECTOR NOTATION: DTR
- DIRECTION: To DCE

This signal controls the switching of the DCE to the communication channel. The DTE will generate this signal to prepare the DCE to be connected to or removed from the communication channel.

CIRCUIT LL - LOCAL LOOPBACK

- CONNECTOR NOTATION: LLBK
- DIRECTION: To DCE

This signal provides a means whereby a DTE may check the functioning of the DTE/DCE interface and the transmit and receive sections of the local DCE.

CIRCUIT RL - REMOTE LOOPBACK

- CONNECTOR NOTATION: RLBK
- DIRECTION: To DCE

This signal provides a means whereby a DTE or a facility test center may check the transmission path up to and through the remote DCE to the DTE interface and the similar return transmission path.

CIRCUIT TM - TEST MODE

- CONNECTOR NOTATION: TEST MODE
- DIRECTION: From DCE

This signal indicates to the DTE that the DCE is in a test condition. The DCE generates this signal when it has received a local loopback or remote loopback signal from the DTE.

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Appendix HARDWARE INSTALLATION

The following are the steps required for installing the MPA-100.

1. Set addressing, interrupts, DMA and other configuration jumper blocks.
2. Turn system unit off.
3. Remove system cover as instructed in the computer reference guide.
4. Insert adapter into any vacant 16 bit slot following the guidelines for installation.
5. Replace system cover.

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Appendix SPECIFICATIONS

Bus interface:	IBM AT 16-bit bus	
Controller:	Serial Communications Controller, 10 MHz (determined by user, typically an AMD 85C30).	
Interface:	DTE: male D-25 connector	
Transmit drivers:	RS-232:	MC1488 or compatible
Receive buffers:	RS-232:	MC1489 or compatible
I/O Address range:	0000H - FFFFH	
Interrupt levels: fx	IRQ 2-7, 10-12, 14-15	
DMA levels:	DMA Channel 1, 2, and 3 on transmit and receive.	

Power requirements:

I_{Typ} (mA)	I_{Max} (mA)	Supply Voltage (Volts)
1248	1402	5
25	36	12
25	36	-12

MPA-100 RS-232 SYNCHRONOUS ADAPTER FOR EIA-232-D STANDARD

HARDWARE REFERENCE GUIDE

Revision C, 2/2/93