256K X28C256 32K x 8 Bit

5 Volt, Byte Alterable E²PROM

FEATURES

- **Access Time: 200ns**
- **Simple Byte and Page Write**
  - **Single 5V Supply**
    - **No External High Voltages or V_{PP} Control Circuits**
  - **Self-Timed**
    - **No Erase Before Write**
    - **No Complex Programming Algorithms**
    - **No Overerase Problem**
- **Low Power CMOS:**
  - **Active: 60mA**
  - **Standby: 200µA**
- **Software Data Protection**
  - **Protects Data Against System Level Inadvertent Writes**
- **High Speed Page Write Capability**
- **Highly Reliable Direct Write™ Cell**
  - **Endurance: 100,000 Write Cycles**
  - **Data Retention: 100 Years**
- **Early End of Write Detection**
  - **$\overline{\text{DATA}}$ Polling**
  - **Toggle Bit Polling**

DESCRIPTION

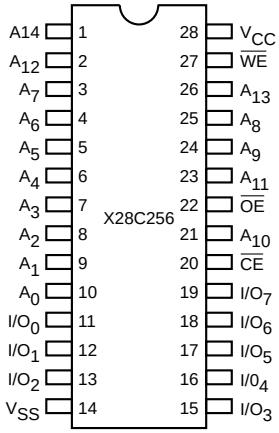
The X28C256 is an 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256 supports a 64-byte page write operation, effectively providing a 78µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features $\overline{\text{DATA}}$ and Toggle Bit Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

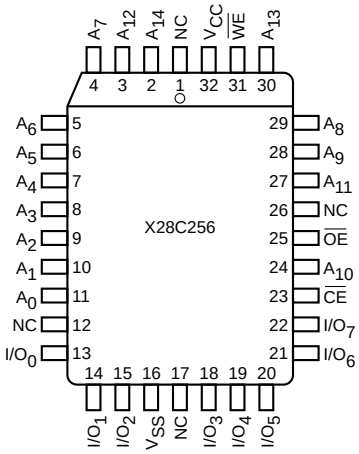
PIN CONFIGURATION

PLASTIC DIP
CERDIP
FLAT PACK
SOIC



3855 FHD F02

LCC
PLCC



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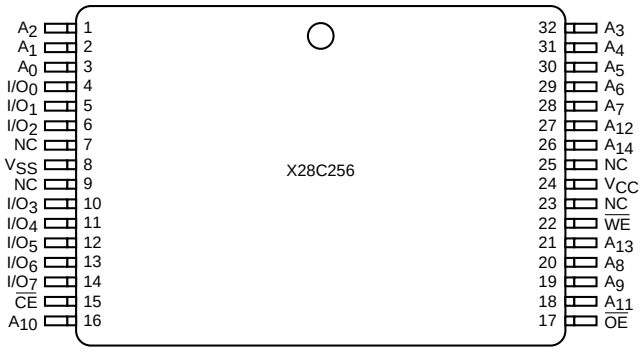
TSOP



3855 ILL F23

PIN DESCRIPTIONS

Addresses (A_0–A_{14})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C256 through the I/O pins.

Write Enable ($\overline{WE}$)

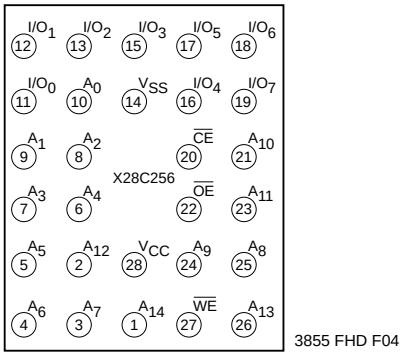
The Write Enable input controls the writing of data to the X28C256.

PIN NAMES

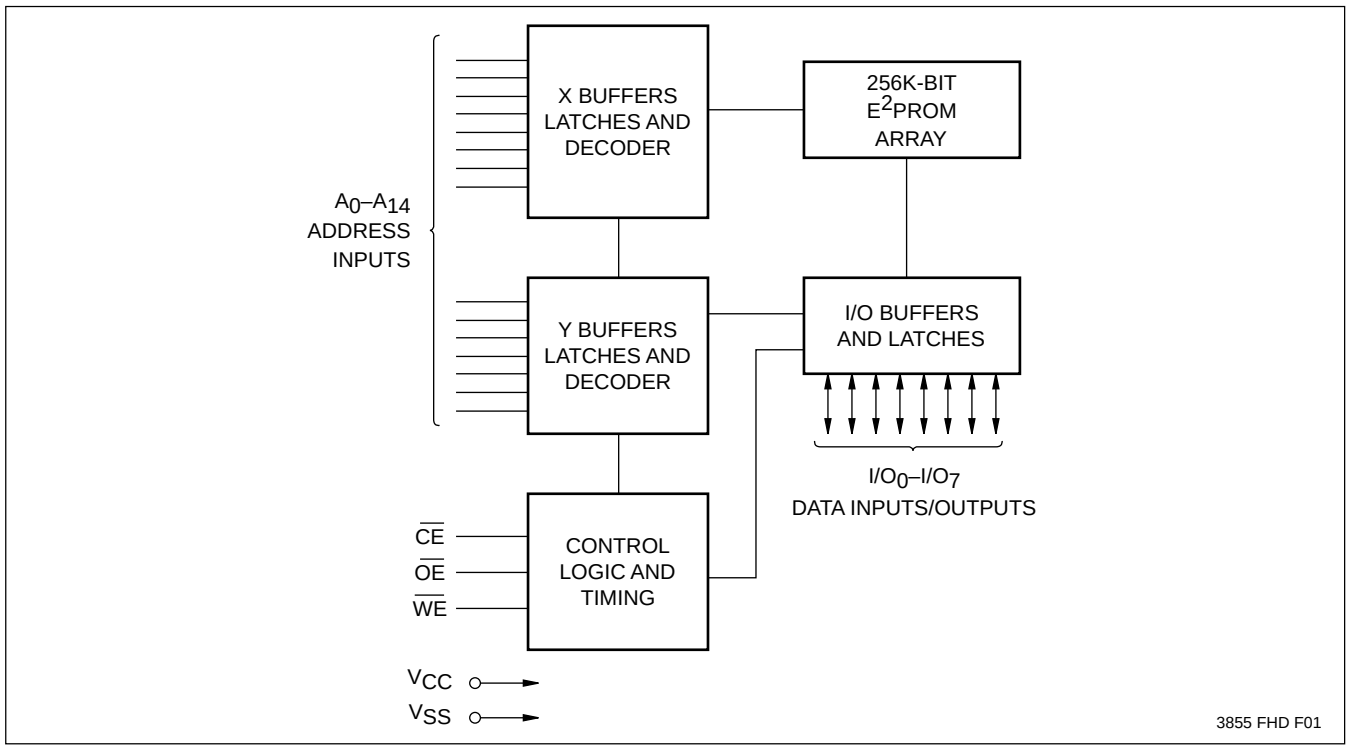
Symbol	Description
A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3855 PGM T01

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28C256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

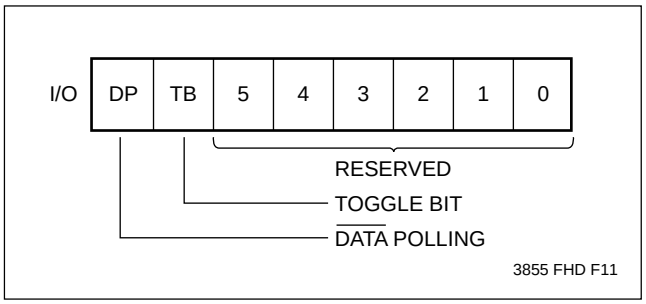
The page write feature of the X28C256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_6 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28C256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C256 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

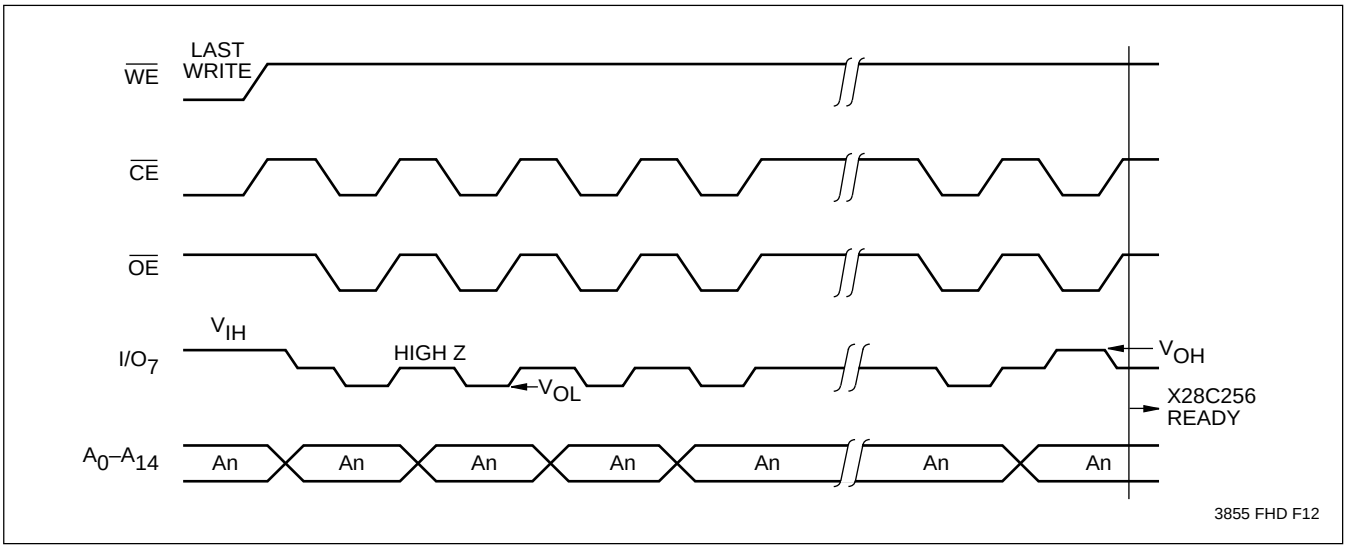
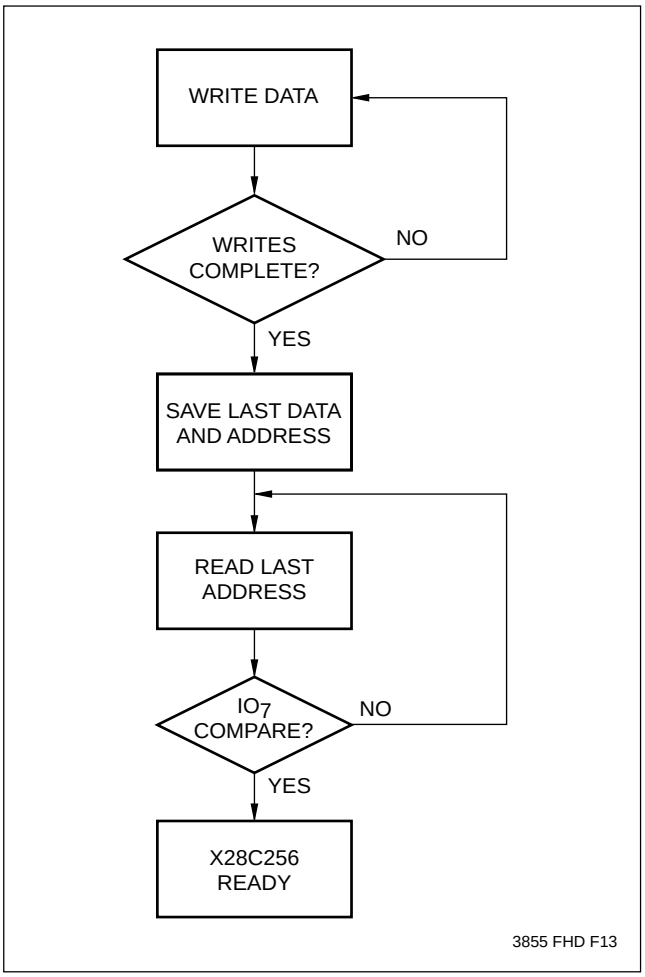


Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28C256. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

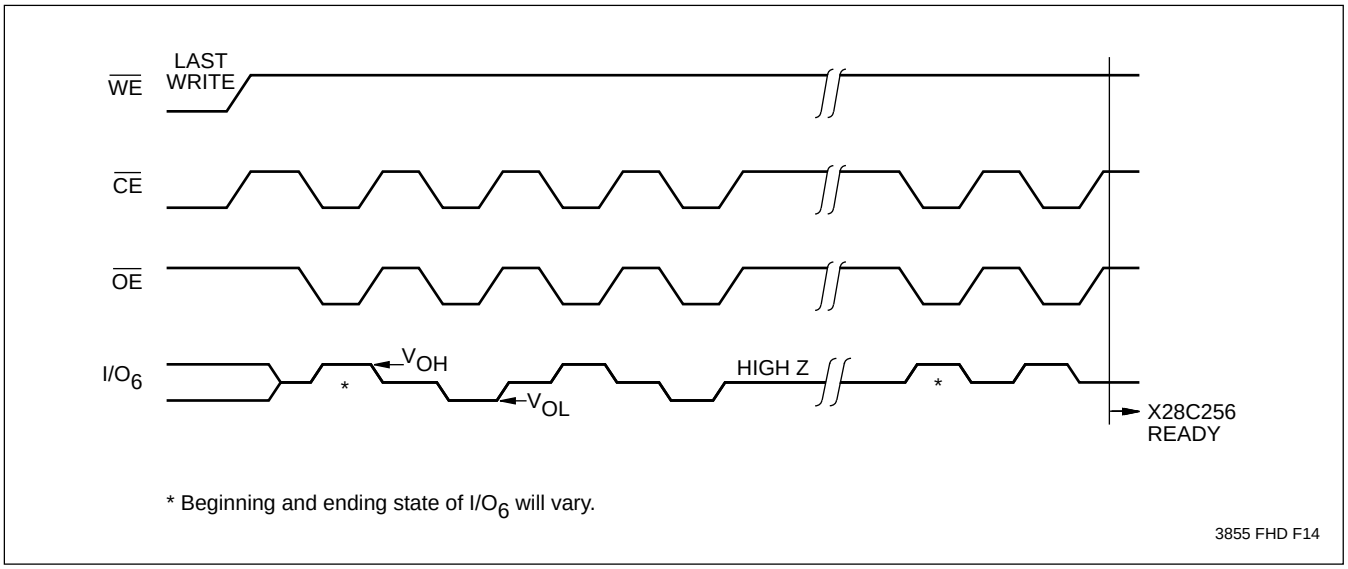
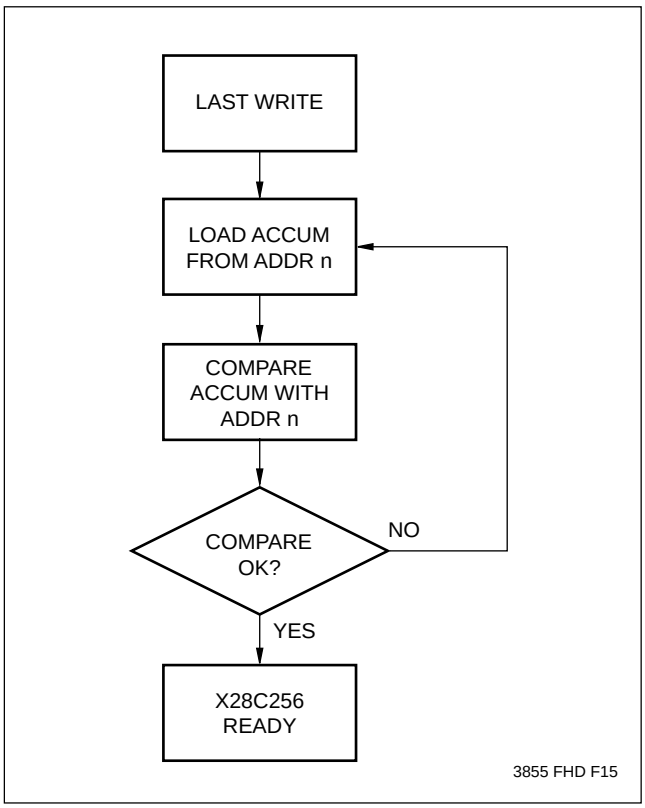


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C256 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C256 provides three hardware features (compatible with X28C64) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 20ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤3.5V typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C256 offers a software controlled data protection feature. The X28C256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

Software Algorithm

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three-byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.* Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

**Note: Once the three-byte sequence is issued it must be followed by a valid byte or page write operation.*

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

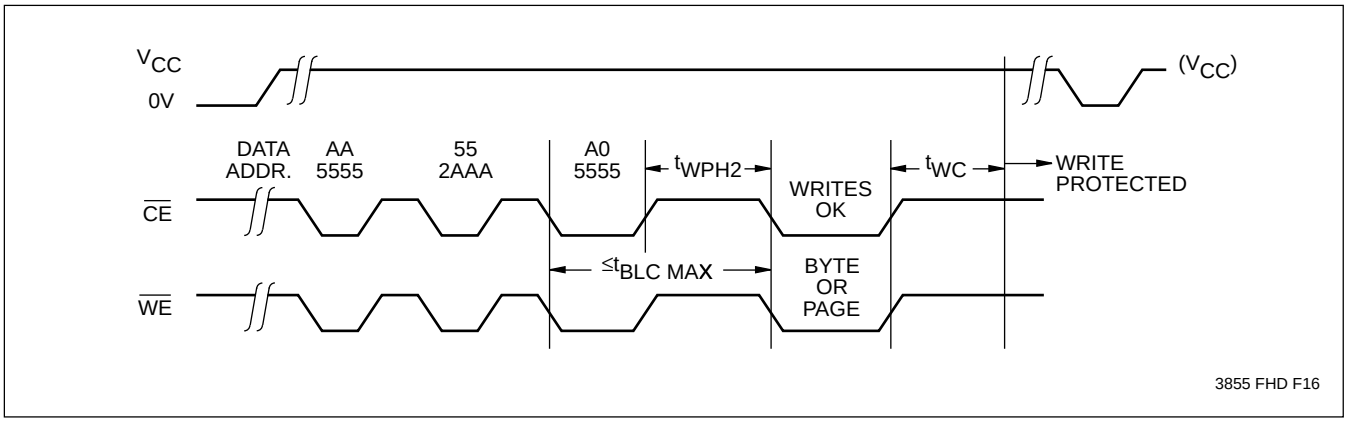
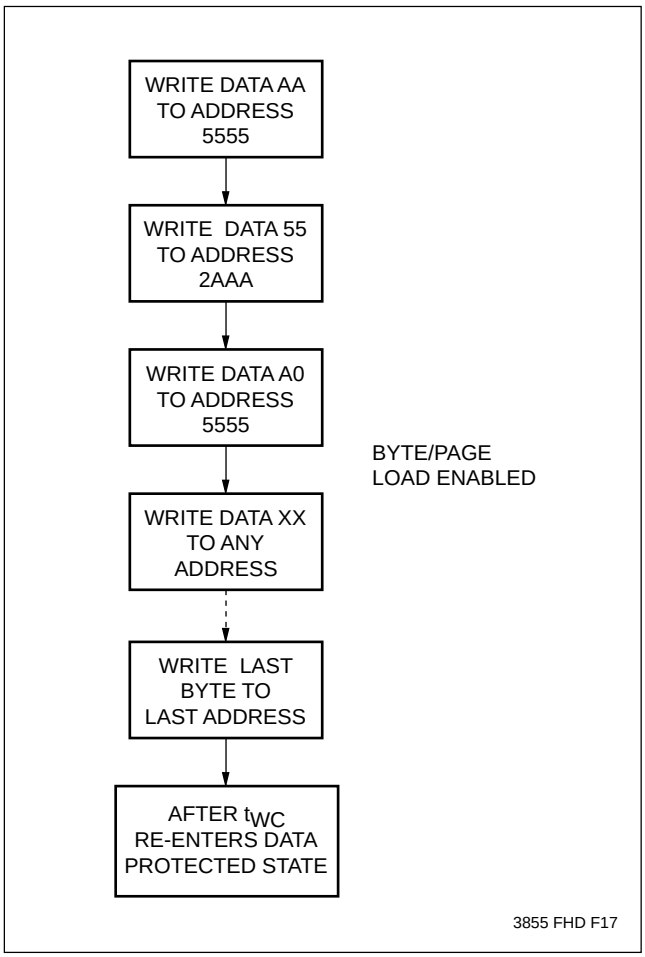


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

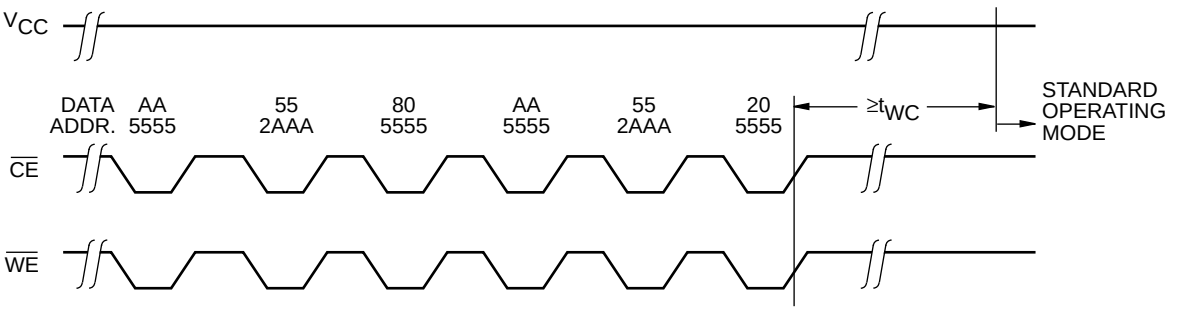
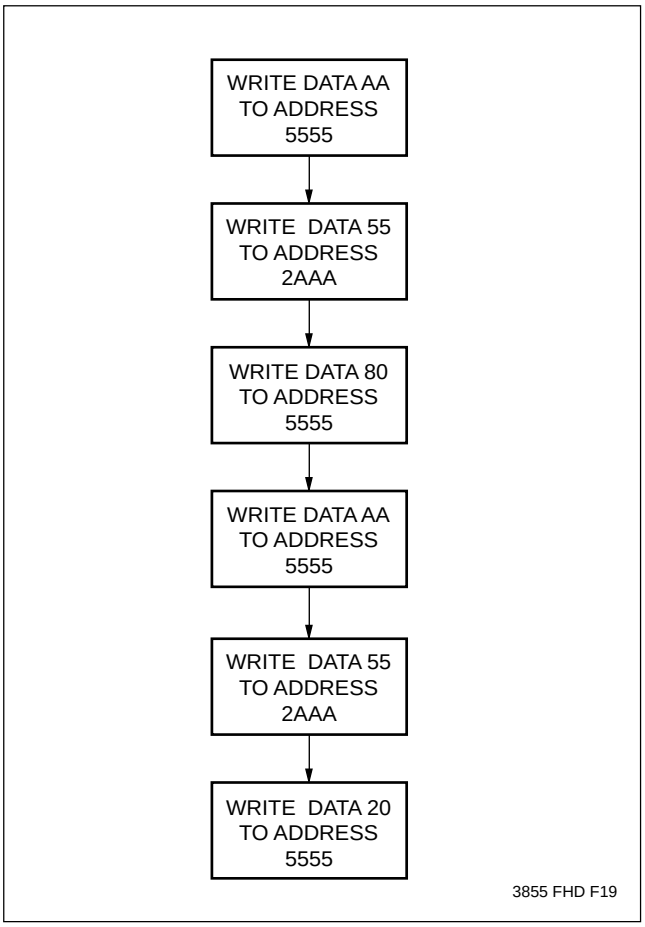


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

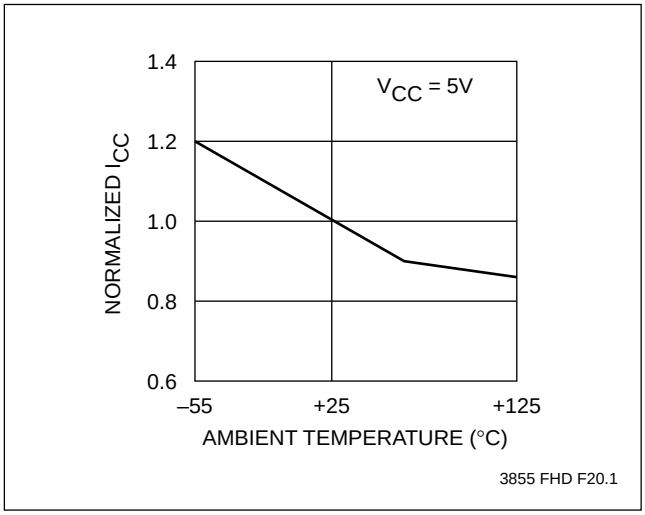
Because the X28C256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

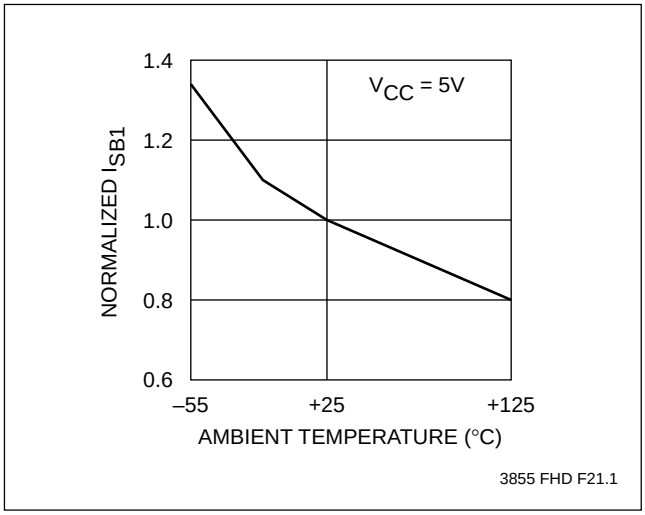
Because the X28C256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X28C256 ..... –10°C to +85°C
- X28C256I, X28C256M ..... –65°C to +135°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... –1V to +7V

D.C. Output Current 5mA

Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3855 PGM T02.1

Supply Voltage	Limits
X28C256	5V ±10%

3855 PGM T03.1

D.C. OPERATING CHARACTERISTICS (over recommended operating conditions, unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)			60	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = .4V/2.4V @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)			2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}(2)	V_{CC} Current (Standby) (CMOS Inputs)		200	500	µA	$\overline{CE}$ = V_{CC} – 0.3V, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC} – 0.3V
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(3)	Input LOW Voltage	–1		0.8	V	
V_{IH}(3)	Input HIGH Voltage	2		V_{CC} + 1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –400µA

3855 PGM T04.2

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage and are not tested
(2) I_{SB2} max. of 200µA available from Xicor. Contact local sales office and reference X28C256 C7125.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Cycles
Data Retention	100	Years

3855 PGM T05.1

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-up to Read Operation	100	µs
t_{PUW}(4)	Power-up to Write Operation	5	ms

3855 PGM T06

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

3855 PGM T07.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3855 PGM T08.1

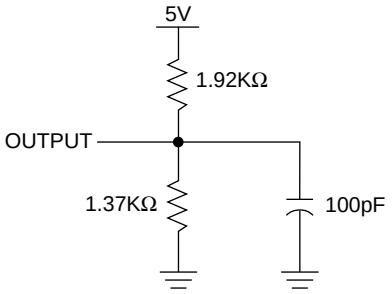
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3855 PGM T09

Note: (4) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



3855 FHD F22.3

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

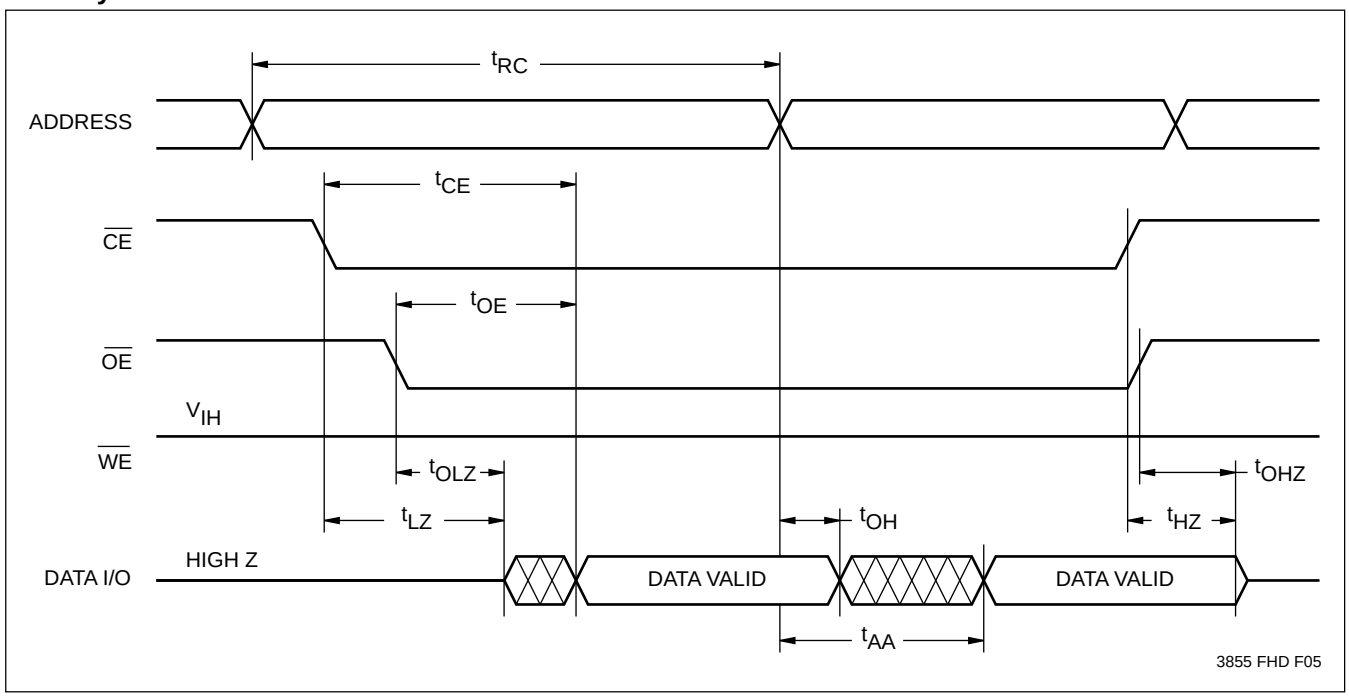
A.C. CHARACTERISTICS (over recommended operating conditions, unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X28C256-20		X28C256-25		X28C256		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	Chip Enable Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
t_{OE}	Output Enable Access Time		80		100		100	ns
t_{LZ}(5)	$\overline{CE}$ LOW to Active Output	0		0		0		ns
t_{OLZ}(5)	$\overline{OE}$ LOW to Active Output	0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ HIGH to High Z Output		50		50		50	ns
t_{OHZ}(5)	$\overline{OE}$ HIGH to High Z Output		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

3855 PGM T10.1

Read Cycle



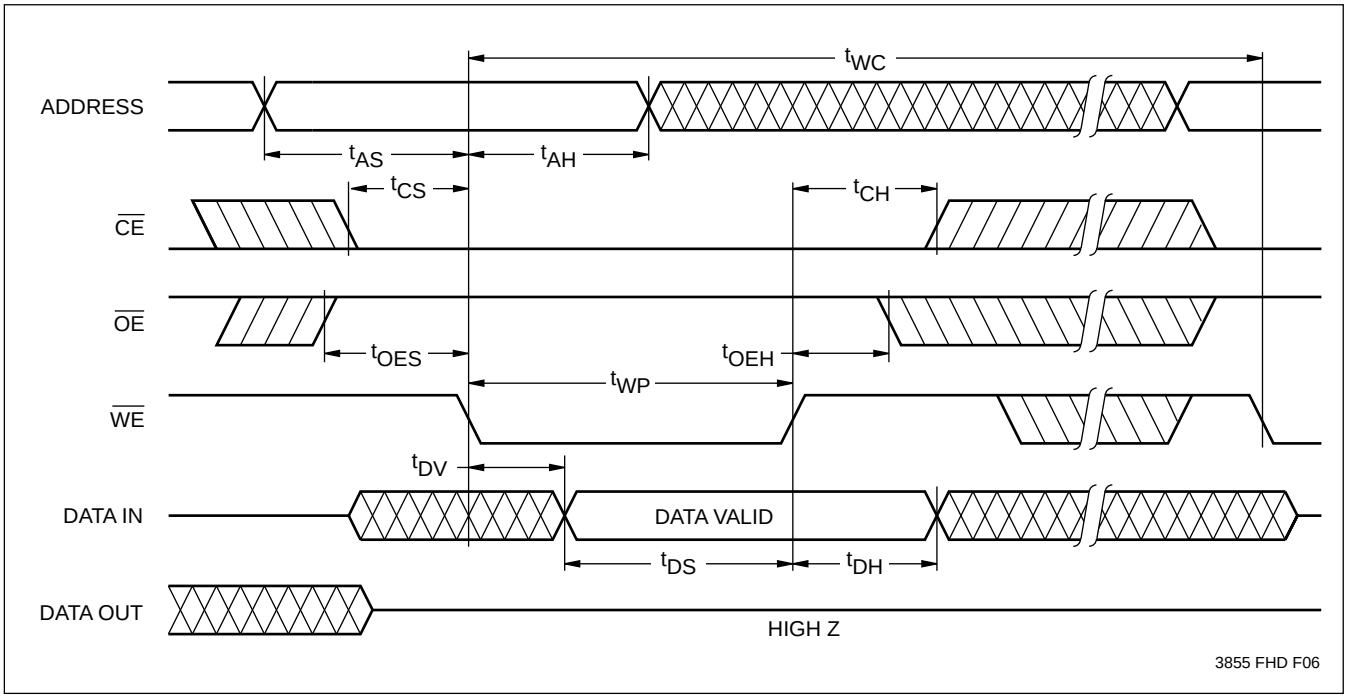
Note: (5) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are peridocally sampled and not 100% tested. t_{HZ} and t_{OHZ} are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

WRITE CYCLE LIMITS

Symbol	Parameter	Min.(9)	Typ.(6)	Max.	Units
t_{WC}(7)	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10			ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	50			ns
t_{WPH2}(8)	SDP $\overline{WE}$ Recovery	1			µs
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}(9)	Byte Load Cycle	1		100	µs

3855 PGM T11.1

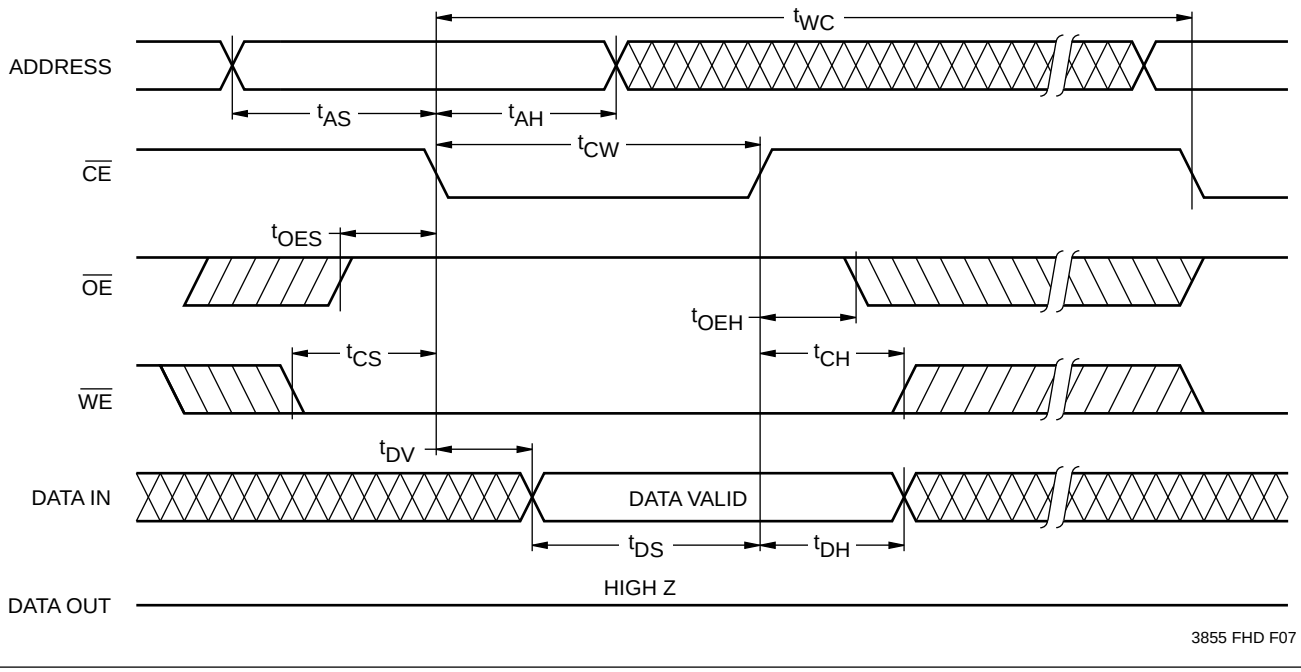
$\overline{WE}$ Controlled Write Cycle



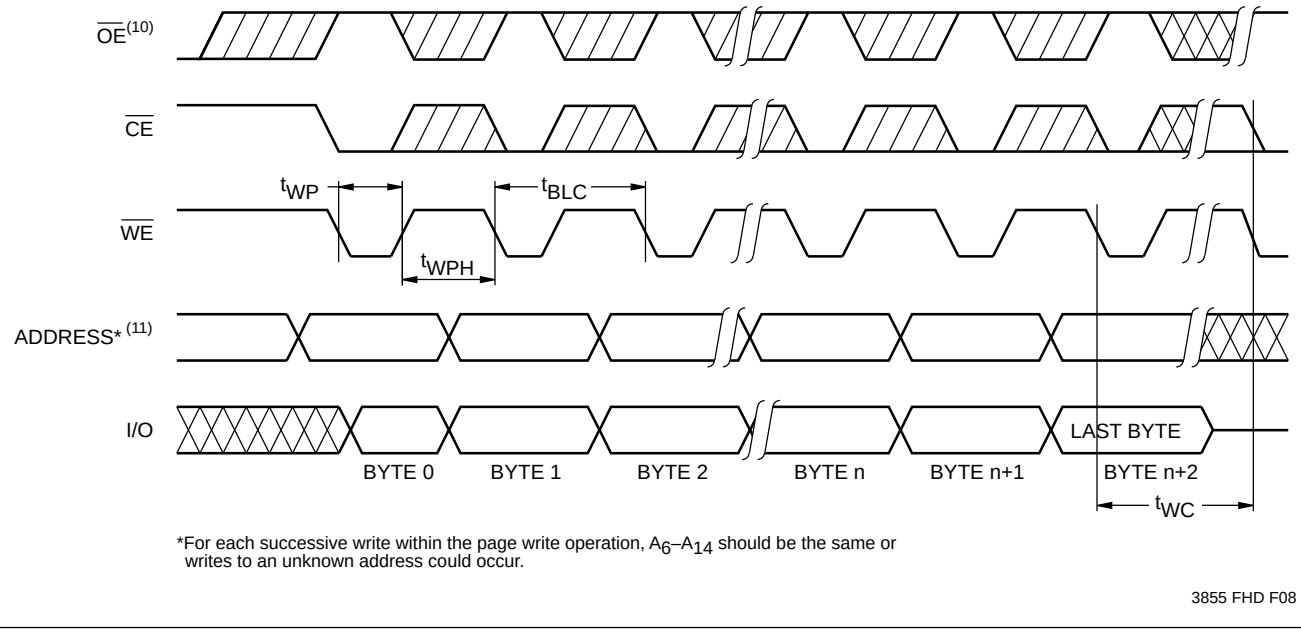
3855 FHD F06

Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
(8) t_{WPH} is the normal page write operation $\overline{WE}$ recovery time. t_{WPH2} is the $\overline{WE}$ recovery time needed only after the end of issuing the three-byte SDP command sequence and before writing the first byte of data to the array. Refer to Figure 6 which illustrates the t_{WPH2} requirement.
(9) For faster t_{WC} and t_{BLC}, refer to X28HC256 or X28VC256.

$\overline{CE}$ Controlled Write Cycle



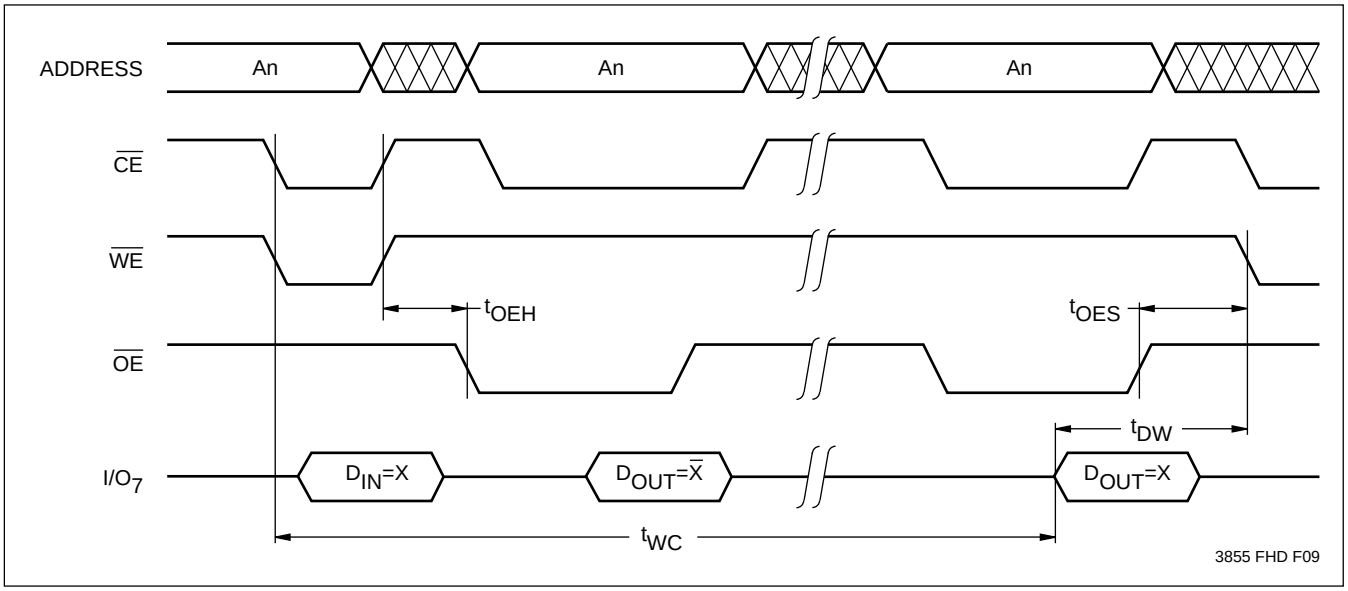
Page Write Cycle



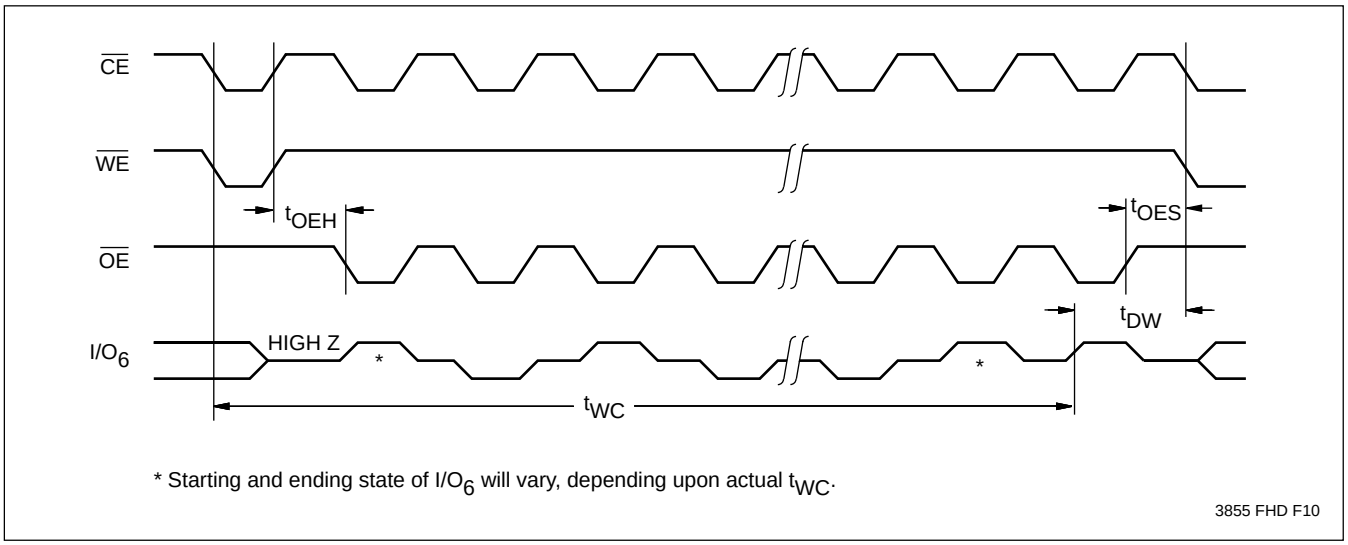
Notes: (10) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(11) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{DATA}$ Polling Timing Diagram(12)



Toggle Bit Timing Diagram(12)



Note: (12) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

ORDERING INFORMATION