# ThinkPad<sub>®</sub> ThinkCentre<sub>®</sub>

## Personal Systems Reference Intel<sup>®</sup> PC Processors

January 2009 - Version 350



Visit www.lenovo.com/psref for the latest version

### [Notebook] Intel Celeron M Processor 5xx

Intel® Celeron® M processor for mobile systems	Clock Perf Mode	Clock Battery Mode	L2 cache	System bus MHz	Core	Hyper- Threading Technology	Virtual- ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Avail- able date
Ultra Low Voltage											
Intel Celeron M Processor 523	933MHz	N/A	1MB	533MHz	Single	No	No	Yes	No	Yes	Sep 2007
Standard Voltage											
Intel Celeron M Processor 520	1.6GHz	N/A	1MB	533MHz	Single	No	No	Yes	No	Yes	Jan 2007
Intel Celeron M Processor 530	1.73GHz	N/A	1MB	533MHz	Single	No	No	Yes	No	Yes	Apr 2007
Processor generation Marketing name Core	Merom Intel Ce Single-o		Proce	ssor							
Branding	•		ntel Ce	ntrino® Pro	ocessor	Technoloav c	r Intel Ce	ntrino with	h vPro Processo	or Techno	loav
Micro-architecture	Intel Co										- 37
MMX <sup>™</sup> / Streaming SIMD	MMX™ (	(57 new	instruc	tions), Stre	eaming	SIMD Extens	ions (70 r	new instru	ctions)		
SSE2						instructions)					
SSE3		ng SIMD	Exten	sions 3 (1	3 new ir	nstructions)					
Hyper-Threading	None										
Total threads						reading suppo ous software e			gical processor)		
Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup>	None	memor	y uala		Imanut		Execution				
Virtualization Technology	None										
L1 cache	256-bit o	data patl	h, full s	peed							
L1 data cache	32KB da										
L1 instruction cache	32KB in	struction	n cache	, integrate	d						
L2 cache - size	<b>1MB</b> , fu										
L2 cache - data path		data patł	h (32 b	/tes), 64 b	yte cacl	he line size, 8	-way set	associativ	e, integrated, u	nified (on	die)
L3 cache	None										
System bus System bus - width	<b>533MHz</b> 64-bit da	•	ers data	a 4 times p	er clock	k), address bu	is transfer	rs at 2 tim	es per clock		
Execution units	0			0.	its, 1 loa	ad unit, 1 stor	e unit				
Math coprocessor	Pipeline		0.								
Compatibility	Compat	ible with	IA-32 :	software							
Process technology	65nm or				, ,.,	"					
Thermal Design Power		-		atts; Star	ndard Vo	oltage: 30 wa	tts				
Package and connector	All: 520/530		ket M	hin Pin G	rid Arra			ras 170-n	in surface mour	nt Zero Ind	ertion
	520/550		•	•		9M socket)	Gry requi	nca 479-b	an sunace mou		
	523:		· · ·	· ·		,	GA) for s	urface mo	ount (479-ball)		
Chipset support			•	•		ly; other com	,		()		
			-	-							

All trademarks are the property of their respective owners © Lenovo (M5C) Compiled by Roger Dodson, Lenovo. September 2007

### [Notebook] Intel Celeron Processor 5xx, 7xx

Intel <sup>®</sup> Celeron <sup>®</sup> mobile processor	Clock Perf Mode	Clock Battery Mode	L2 cache	System bus MHz	Core	Thermal Design Power	Hyper- Threading Technology	Virtual- ization Tech	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Avail- able date
Intel Celeron Processor 530	1.73GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Sep 2007
Intel Celeron Processor 540	1.86GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Jun 2007
Intel Celeron Processor 550	2.00GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Jun 2007
Intel Celeron Processor 560	2.13GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Jan 2008
Intel Celeron Processor 570	2.26GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Apr 2008
Intel Celeron Processor 575	2.00GHz	N/A	1MB	667MHz	Single	31W	No	No	No	Yes	Aug 2008
Intel Celeron Processor 585	2.16GHz	N/A	1MB	667MHz	Single	31W	No	No	No	Yes	Aug 2008
Intel Celeron Processor 723	1.20GHz	N/A	1MB	800MHz	Single	10W	No	No	No	Yes	Aug 2008

Processor generation	5xx: Merom; 7xx: Penryn
Marketing name	Intel Celeron mobile processor
Core	Single-core
Branding	Not part of the Intel Centrino <sup>®</sup> Processor Technology or Intel Centrino with vPro Processor Technology
Micro-architecture	Intel Core™ Micro-architecture
MMX <sup>™</sup> / Streaming SIMD	MMX <sup>™</sup> (57 new instructions), Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	None
Total threads	One thread (one cores with no Hyper-Threading support provides one logical processor)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology <sup>1</sup>	None
Virtualization Technology	None
L1 cache	256-bit data path, full speed
L1 data cache	32KB data cache, integrated
L1 instruction cache	32KB instruction cache, integrated
L2 cache - size	1MB, full speed
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None
System bus	533MHz, 667MHz, or 800MHz (transfers data 4 times per clock), address bus transfers at 2 times per clock
System bus - width	64-bit data path
Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	65nm or 0.065u
Thermal Design Power	5xx: 27-31 watts @ 0.95-1.3 volts
-	7xx: 10 watts (Ultra Low Voltage)
Package and connector	5xx: Socket P / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount
	Zero Insertion Force (ZIF) socket (mPGA479M socket)
	7xx: Socket P / Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	5xx: Mobile Intel 965 Express Chipset family; other compatible chipsets
	7xx: Mobile Intel 4 Series Express Chipset family; other compatible chipsets

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

(CEL5) Compiled by Roger Dodson, Lenovo. September 2008

### [Notebook] Intel Celeron Processor

Intel® Celeron® mobile processor	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	HD Boost	Virtual- ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Trusted Execution Tech	Avail- able date
	.66GHz .86GHz		667MHz 667MHz		No No	No No	Yes Yes	Yes Yes	Yes Yes	No No	Oct 2008 Oct 2008
Processor generation Marketing name Core Branding	Dual-o	celeron i core	<b>nobile pr</b>								
Micro-architecture Intel Wide Dynamic Execution Intel Smart Memory Access Intel Advanced Digital Media Boos Power mgmt technology Hyper-Threading Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> (EM64T) Intel Virtualization Technology	Intel C Each o Hides Enhan No Protec Intel 6 64 bit No	ore Micro core can memory erates ex- ced Intel ts memo 4 Techno	o-architect complete latency ecution of I SpeedSte	ture up to fo Stream ep™ tec eas fror xtensio	ur full ins ing SIMD hnology ( n malicio n to the I	Extensio EIST) us softwa	n (SSE2/3	,	0		lications
Intel Trusted Execution Technolog L1 cache L1 data cache L1 instruction cache	64KB 2x32K	B data c	split betwe ache / inte	grated		32KB) an	d instuctio	n cache (32KB)			
L2 cache - size L2 cache - data path								d Smart Cache) set associative /		d / unified (d	on die)
System bus Memory addressability System bus - width	64GB	•	addressal					sfers at 2 times   addressing	per clock		
Execution units Math coprocessor Compatibility	Pipelir	ed floati	1 floating ng point u h IA-32 so	nit	nits, 1 Ioa	เd unit, 1 ร	store unit				
Process technology Thermal Design Power Package and connector Chipset support	35 wat Socke	tP/Mic	u ro Flip-Ch <b>Series Cł</b>					sets			

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

(DCELM) Compiled by Roger Dodson, Lenovo. January 2009

### [Notebook] Intel Pentium Processor

Intel® Pentium® Processor	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Hyper- Threading Technology	Virtual- ization Tech		Enhanced Inte SpeedStep™ Technology	64 Tech	Trusted Execution Tech	Intel Dynam Accelera	nic	Avail- able date
Intel Pentium Processor T2060					No	No	Yes	Yes	No	No	No		2007
Intel Pentium Processor T2080					No	No	Yes	Yes	No	No	No		2007
Intel Pentium Processor T2130					No	No	Yes	Yes	No	No	No		2007
			533MHz	Dual	No	No	Yes	Yes	Yes	No	No		/ 2007
				Dual	No	No	Yes	Yes	Yes	No	No		/ 2007
			533MHz	Dual	No	No	Yes	Yes	Yes	No	No		2008
Intel Pentium Processor T2390	1.86GHz	: 1MB	533MHz	Dual	No	No	Yes	Yes	Yes	No	No	Jan	2008
Intel Pentium Processor T3200					No	No	Yes	Yes	Yes	No	No	Nov	/ 2008
Intel Pentium Processor T3400	2.16GHz	1MB	667MHz	Dual	No	No	Yes	Yes	Yes	No	No	Nov	/ 2008
Processor generation					T2310/T23	30/T237	0/T2390/	/T3200/T3400	: Merom				
Marketing name			m Proces	sor									
Core	Dual-												
Branding	Value	or ess	ential mob	oile pro	ocessor								
Micro-architecture			icro-archit										
Intel Wide Dynamic Execution					o four full in	structior	is simulta	neously using	g 14-stag	e pipeline	;		
Intel Smart Memory Access			ry latency										
Intel Advanced Digital Media Boo					•		sion (SSE	E2/3) instruction	ons used	in multim	edia app	licatio	ons
Power mgmt technology				Step™	technology								
Thermal management	-	I therm	al sensor										
Hyper-Threading	No												
Total threads			•			0		provide two lo	ogical pro	cessors)			
Execute Disable (XD) Bit			•		from malici								
Intel 64 Technology <sup>1</sup> (EM64T)					an extension architecture		A-32 inst	ruction set wh	nich adds				
Intel Virtualization Technology	No												
Intel Trusted Execution Technolog													
Intel Dynamic Accerlation	No												
L1 cache	64KB	per co	re split be	tween	data cache	(32KB)	and instu	ction cache (3	32KB)				
L1 data cache			cache / ii			(- )			,				
L1 instruction cache			uction cad	-									
L2 cache - size	1MB	/ full sp	eed, share	ed betv	ween both c	ores (Int	el Advan	ced Smart Ca	ache)				
L2 cache - data path	256-b	it data	path (32 b	ytes),	64 byte cac	he line s	ize, 8-wa	y set associa	tive, integ	rated, un	ified (on	die)	
L3 cache	None				-			-	_			,	
System bus	533M	Hz or 6	67MHz (t	ransfe	rs data 4 tim	nes per c	lock), ad	dress bus trar	nsfers at 2	2 times pe	er clock		
Memory addressability								bit addressing					
System bus - width		data p		,	(				2				
Execution units	2 inte	aer uni	ts. 1 floati	na poi	nt units, 1 lo	ad unit.	1 store u	nit					
Math coprocessor			ating point			,		-					
Compatibility	•		with IA-32		are								
Process technology	65nm	or 0.00	35u										
Package and connector	T206	0/T208	0/T2130:					ro-FCPGA) re	•	•			ero
	-				(mPGA479N	A socket	) or Micro	o Flip-Chip Ba	II Grid Ar	ray (Micro	-FCBGA	) for	
	surfac	ce mou	nt (479-ba	ull)									
			<u>`</u>			-	_				_		
	T231	0/T233						cro Flip-Chip		• •		SA)	
	T231 requii	0/T233 res 479	-pin surfac	ce mou	unt Zero Ins	ertion Fo	orce (ZIF)	cro Flip-Chip socket (mPG mount (479-l	6A479M s	• •		GA)	

All trademarks are the property of their respective owners © Lenovo (P2) Compiled by Roger Dodson, Lenovo. January 2009

### [Notebook] Intel Core 2 Solo Processor

Intel® Core™ 2 Solo processor for mobile systems	Clock Perf Mode	L2 cache	System bus MHz	Core	Hyper- Threading Technology	Virtual- ization Tech	Intel 64 Tech (EM64T)	Intel HD Boost	Intel Dynamic Acceleration	Truste Executi Tech (T	on	Avail- able date
Ultra Low Voltage												
Intel Core 2 Solo processor U2100	1.06GHz	1MB	533MHz	Single	e No	Yes	Yes	No	No	No	Se	p 2007
Intel Core 2 Solo processor U2200	1.20GHz	1MB	533MHz	Single	e No	Yes	Yes	No	No	No	Se	p 2007
Intel Core 2 Solo processor SU3300	) 1.20GHz	3MB	800MHz	Single	e No	Yes	Yes	Yes	No	Yes	Au	g 2008
Intel Core 2 Solo processor SU3500	) 1.30GHz	3MB	800MHz	Single	e No	Yes	Yes	Yes	No	Yes	Au	g 2008
Processor generation Marketing name	Uxxxx: Merc Intel Core 2			-	-	n (Monte	evina)					
Core	Single-core			/000000								
Micro-architecture	Intel Core M		hitecture									
Intel Wide Dynamic Execution				o four f	ull instructio	ns simult	aneously u	sina 14-s	tage pipeline			
Intel Smart Memory Access	Hides memo							og o	age pipeline			
Intel Advanced Digital Media Boost				amina	SIMD Exter	sion (SS	E2/3) instru	uctions us	sed in multime	dia app	licati	ions
Intel HD Boost	Some: Stre											
Power management technology	Enhanced Ir							5				
Intel Dynamic Power Coordination	indepen	dently p	er core to	help s	ave power				nent state trar			
Intel Dynamic Bus Parking			ower savin v-frequenc			attery life	e by allowin	g the chip	oset to power	down w	ith th	ne
Enhanced Intel Deeper Sleep with Dynamic Cache Sizing	Saves powe to lower			e data	to system r	nemory o	during perio	ds of inad	ctivity			
Thermal management	Digital thern	nal sens	or									
Hyper-Threading	No											
Execute Disable (XD) Bit	Protects me											
Intel 64 Technology <sup>1</sup> (EM64T)		tension	is to the x8	86 arcl		struction	set which	adds				
Virtualization Technology	Intel Virtuali	zation T	echnology	/								
Intel Dynamic Acceleration	None											
Intel Trusted Execution Tech (TXT)	Some: Prov	ides a r	nore secu	re plat	form from so	oftware-b	ased attack	s with 17	(T-enabled OS	s or app		
L1 cache	64KB per co			data ca	ache (32KB)	and inst	uction cach	e (32KB)				
L1 data cache	32KB data o		-	ا مدمد								
L1 instruction cache	32KB instru	ction ca	cne / Integ	grated								
L2 cache - size	1MB or 3ME			C 4 h. 4				:- <i>!</i> /	(intermeteral ( )		الم من	-)
L2 cache - data path	None	pain (3	Z bytes) /	64 DYI	e cache line	Size / 6-	way set ass	ociative /	/ integrated / u	ninea (c	n ai	e)
L3 cache	None											
System bus									s at 2 times pe	r clock		
Memory addressability	64GB memo		essability	(but lir	nited by chip	oset) / 36	-bit addres	sing				
System bus - width	64-bit data p	bath										
Execution units per core	2 integer un			t units	, 1 load unit,	1 store u	unit					
Math coprocessor	Pipelined flo	01										
Compatibility	Compatible	with IA-	32 softwa	re								
Process technology	Uxxxx: 65nr	n; S <i>Uxx</i>	<i>xx:</i> 45nm									
Thermal Design Power	5.5 watts											
Package and connector	Uxxxx: So											
	SUxxxx: So											
		hile lest	AL DAECM	and 0	45040 5	~	the sector of th					
Chipset support	SUxxxx: Mc								ible chipsets			

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

(C2S) Compiled by Roger Dodson, Lenovo. September 2008

#### [Notebook] Intel Core 2 Duo Processor (Socket M)

Intel <sup>®</sup> Core <sup>™</sup> 2 Duo processor for mobile systems	Clock Perf Mode	Battery	Shared L2 cache	System bus MHz	Core	Hyper- Threading Technology		Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	64 Tech	Intel Dynan Accelera	
Intel Core 2 Duo processor U7500	1.06GHz	800MHz	2MB 5	533MHz	Dual	No	Yes	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor U7600	1.20GHz	800MHz	2MB 5	533MHz	Dual	No	Yes	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor U7700	1.33GHz	800MHz	2MB 5	533MHz	Dual	No	Yes	Yes	Yes	Yes	No	Jun 2007
Intel Core 2 Duo processor L7200	1.33GHz	1.0GHz	<b>4MB</b> 6	67MHz	Dual	No	Yes	Yes	Yes	Yes	No	Jan 2007
Intel Core 2 Duo processor L7400	1.50GHz	1.0GHz	<b>4MB</b> 6	67MHz	Dual	No	Yes	Yes	Yes	Yes	No	Jan 2007
Intel Core 2 Duo processor T5200	1.60GHz	1.0GHz	2MB 5	533MHz	Dual	No	No	Yes	Yes	Yes	No	Jan 2007
Intel Core 2 Duo processor T5300	1.73GHz	1.0GHz	2MB 5	533MHz	Dual	No	No	Yes	Yes	Yes	No	Oct 2007
Intel Core 2 Duo processor T5500	1.66GHz	1.0GHz	2MB 6	67MHz	Dual	No	No	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor T5600	1.83GHz	1.0GHz	2MB 6	67MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor T7200	2.00GHz	1.0GHz	<b>4MB</b> 6	67MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor T7400	2.16GHz	1.0GHz	<b>4MB</b> 6	67MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor T7600	2.33GHz	1.0GHz	<b>4MB</b> 6	67MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006

U (Ultra Low Voltage)=<14 watts; L (Low Voltage)=15-24 watts; T (Standard Voltage)=25-49 watts; E=>50 watts

Brosser generation	Morom
Processor generation Marketing name	Merom Intel Core 2 Duo mobile processor
Core	Dual-core
Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Power management technology	Enhanced Intel SpeedStep® technology
Intel Dynamic Power Coordination	Coordinates Enhanced Intel SpeedStep Technology and idle power-management state transitions independently per core to help save power
Intel Dynamic Bus Parking	Enables platform power savings and improved battery life by allowing the chipset to power down with the processor in low-frequency mode
Enhanced Intel Deeper Sleep with Dynamic Cache Sizing	Saves power by flushing cache data to system memory during periods of inactivity to lower CPU voltage
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology <sup>1</sup> (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64-bit extensions to the x86 architecture)
Virtualization Technology	Some: Intel Virtualization Technology
Intel Dynamic Accerlation	Some: Intel Dynamic Acceleration (IDA) allows one core to deliver extra performance when other core is idle
L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache / integrated
L1 instruction cache	2x32KB instruction cache / integrated
L2 cache - size	2MB or 4MB / full speed / shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None
System bus	533MHz, 667MHz, or 800MHz (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path
Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	65nm or 0.065u
Thermal Design Power	U7xxx: 10 watts; L7xxx: 17 watts; Txxxx: 34 watts
Package and connector	Socket M / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA)
	for surface mount (479-ball)
Chipset support	Mobile Intel 945 Express Chipset family; other compatible chipsets

All trademarks are the property of their respective owners  $\circledast$  Lenovo

#### [Notebook] Intel Core 2 Duo Processor (Socket P)

Intel <sup>®</sup> Core™ 2 Duo processor for mobile systems	Clock Perf Mode	Clock Battery Mode	Shared L2 cache	System bus MHz	Core	Virtual- ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Intel Dynamic Acceleration	Avail- able date
Intel Core 2 Duo processor U7500	1.06GHz	800MHz	2MB	533MHz	Dual	Yes	Yes	Yes	Yes	Yes	Jun 2007
Intel Core 2 Duo processor U7600			2MB	533MHz		Yes	Yes	Yes	Yes	Yes	Jun 2007
Intel Core 2 Duo processor U7700			2MB	533MHz		Yes	Yes	Yes	Yes	Yes	Jan 2008
Intel Core 2 Duo processor SL7100			4MB	800MHz		Yes	Yes	Yes	Yes	Yes	Feb 2008
Intel Core 2 Duo processor L7300 Intel Core 2 Duo processor L7500			4MB 4MB	800MHz 800MHz		Yes Yes	Yes Yes	Yes Yes	Yes Yes	Yes Yes	May 2007 May 2007
Intel Core 2 Duo processor L7300			4MB	800MHz	_	Yes	Yes	Yes	Yes	Yes	Sep 2007
Intel Core 2 Duo processor T5250			2MB	667MHz		No	Yes	Yes	Yes	No	July 2007
Intel Core 2 Duo processor T5270			2MB	800MHz		No	Yes	Yes	Yes	Yes	Aug 2007
Intel Core 2 Duo processor T5450			2MB	667MHz		No	Yes	Yes	Yes	No	July 2007
Intel Core 2 Duo processor T5470			2MB	800MHz		No	Yes	Yes	Yes	Yes	Aug 2007
Intel Core 2 Duo processor T5550 Intel Core 2 Duo processor T5670			2MB 2MB	667MHz 800MHz		No No	Yes Yes	Yes Yes	Yes Yes	No Yes	July 2007 July 2008
Intel Core 2 Duo processor T5750			2MB	667MHz		No	Yes	Yes	Yes	No	Feb 2008
Intel Core 2 Duo processor T5850	2.16GHz	667MHz	2MB	667MHz	Dual	No	Yes	Yes	Yes	No	Feb 2008
Intel Core 2 Duo processor T5870	2.00GHz	800MHz	2MB	800MHz	Dual	No	Yes	Yes	Yes	Yes	Oct 2008
Intel Core 2 Duo processor T7100	1.8GHz	800MHz	2MB	800MHz		Yes	Yes	Yes	Yes	Yes	May 2007
Intel Core 2 Duo processor T7250			2MB	800MHz		Yes	Yes	Yes	Yes	Yes	Sep 2007
Intel Core 2 Duo processor T7300 Intel Core 2 Duo processor T7500			4MB 4MB	800MHz		Yes Yes	Yes Yes	Yes Yes	Yes Yes	Yes Yes	May 2007 May 2007
Intel Core 2 Duo processor 17500			4MB	800MHz 800MHz		Yes	Yes	Yes	Yes	Yes	May 2007 May 2007
Intel Core 2 Duo processor T7800			4MB	800MHz		Yes	Yes	Yes	Yes	Yes	Sep 2007
U (Ultra Low Voltage)=<14 watts; L Processor generation	(Low Volt	age)=15-2	24 watts;	T (Standar	d Volt	age)=25	-49 watts	; E=>50 watts			
Marketing name		re 2 Duo	mobile p	rocessor							
Core	Dual-co										
Micro-architecture		re Micro-a									
Intel Wide Dynamic Execution			• •	to four full	linstru	uctions s	simultaneo	ously using 14-	stage pip	eline	
Intel Smart Memory Access Intel Advanced Digital Media Boost		emory late		rooming S		vtoncio	0 (SSE2/2	) instructions u	cod in m	ultimodia ann	lications
Power management technology				technolog			I (3322/3			unimedia app	lications
Intel Dynamic Power Coordination	Coordina	ates Enha	nced Inte		ер Тес		and idle	power-manage	ment stat	e transitions	
Intel Dynamic Bus Parking	proc	essor in lo	ow-freque	ency mode				allowing the chi		ower down w	ith the
Enhanced Intel Deeper Sleep with		ower by fl wer CPU		iche data to	o syst	em men	nory durin	g periods of ina	activity		
Dynamic Cache Sizing Dynamic Front Side Bus			0	es the bus (	clock t	frequenc	y allowing	g a reduction in	core volt	age enabling	
Frequency Switching		,	-	te called su			by anowing	gureddollorini		age chabiling	
Thermal management		nermal ser			1.						
Hyper-Threading	No										
Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> (EM64T)	Intel 64	Technolog	y (an ext	is from mal ension to tl x86 archit	he IA-	32 instru		on which adds			
Virtualization Technology				echnology		-)					
Intel Dynamic Accertation						ows one	core to d	leliver extra per	formance	when other o	core is idle
L1 cache	64KB pe	er core sol	it betwee	n data cac	he (32	2KB) and	d instuctio	n cache (32KB	)		
L1 data cache	•	data cach				.,			,		
L1 instruction cache				integrated							
L2 cache - size L2 cache - data path			•				•	lvanced Smart et associative, i	,	l, unified (on (	die)
System bus (front side bus) Memory addressability System bus - width		emory ad		<b>IHz</b> (transf ity (but limi			•	ck) / address bi ddressing	us transfe	ers at 2 times	per clock
Execution units per core Math coprocessor	-	r units, 1 f d floating	• •	pint units, 1	load	unit, 1 s	tore unit				
Process technology	65nm or	0.065u									
Thermal Design Power	<i>U7xxx:</i> 1	0 watts;		7 watts; T							
Package and connector	Force (Z	IF) socket						quires 479-pin s all Grid Array (N			
Chipset support	(479-bal Mobile I	,	Express	Chipset fa	mily;	other co	mpatible	chipsets			
All trademarks are the property of the	ir respectiv	ve owners					(C2DP)C	ompiled by Rog	er Dodsor		ombor 2008

All trademarks are the property of their respective owners  $\circledast$  Lenovo

### [Notebook] Intel Core 2 Duo Processor (Penryn)

Intel <sup>®</sup> Core™ 2 Duo processor for notebook systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Thermal Design Power	Virtual- ization Tech	Intel 64 Tech	Intel Dynamic Acceleration	Trusted Execution Tech (TXT)	Ava ab da	le
Intel Core 2 Duo processor T6400		2MB	800MHz	Dual	35W	Yes	Yes	Yes	No		2009
Intel Core 2 Duo processor T6600	2.2GHz	2MB	800MHz	Dual	35W	Yes	Yes	Yes	No	Jan	2009
Intel Core 2 Duo processor T8100	2.1GHz	3MB	800MHz	Dual	35W	Yes	Yes	Yes	No	Jan	2008
Intel Core 2 Duo processor T8300		3MB	800MHz	Dual	35W	Yes	Yes	Yes	No		2008
Intel Core 2 Duo processor T9300	2.5GHz	6MB	800MHz	Dual	35W	Yes	Yes	Yes	No	Jan	2008
Intel Core 2 Duo processor T9500		6MB	800MHz	Dual	35W	Yes	Yes	Yes	No		2008
Intel Core 2 Duo processor P7370	2.00GHz	3MB	1066MHz	Dual	25W	Yes	Yes	Yes	Yes	Sep	2008
Intel Core 2 Duo processor P7450		3MB	1066MHz	Dual	25W	Yes	Yes	Yes	Yes		2009
Intel Core 2 Duo processor P8400		3MB	1066MHz	Dual	25W	Yes	Yes	Yes	Yes		2008
Intel Core 2 Duo processor P8600		3MB	1066MHz	Dual	25W	Yes	Yes	Yes	Yes		2008
Intel Core 2 Duo processor P8700		3MB	1066MHz	Dual	25W	Yes	Yes	Yes	Yes		2008
Intel Core 2 Duo processor P9500 Intel Core 2 Duo processor P9600		6MB	1066MHz	Dual	25W 25W	Yes	Yes	Yes	Yes		2008
	2.00GH2	6MB	1066MHz	Dual	2310	Yes	Yes	Yes	Yes	Dec	2008
Intel Core 2 Duo processor T9400		6MB	1066MHz	Dual	35W	Yes	Yes	Yes	Yes		2008
Intel Core 2 Duo processor T9550		6MB	1066MHz	Dual	35W	Yes	Yes	Yes	Yes		2008
Intel Core 2 Duo processor T9600 Intel Core 2 Duo processor T9800		6MB 6MB	1066MHz 1066MHz	Dual Dual	35W 35W	Yes Yes	Yes Yes	Yes Yes	Yes Yes		2008 2008
U (Ultra Low Voltage)=<12 watts; L (Low									165	Dec	2008
Processor generation Marketing name			00/T9500: Pe nobile proce	<i>.</i>	inta Rosa F	Refresh); (	Others: <b>Pe</b> i	nryn (Montev	vina)		
Core	Dual-core		noone proce	.3301							
Branding		ntel Cen	ntrino® 2 Pro	cessor	Fechnology	or Intel Co	entrino 2 v	with vPro Pro	cessor Tec	hnolo	av
Dianang			and software								-97
Micro-architecture	Intel Core			•							
· · · · · · · · · · · · ·											
Intel Wide Dynamic Execution	Each core	can com	plete up to f	our full in	structions s	imultaneou	sly using 1	4-stage pipel	line		
Intel Wide Dynamic Execution Intel Smart Memory Access	Each core Hides men			our full in	structions s	imultaneou	Isly using 1	4-stage pipel	line		
Intel Smart Memory Access Intel Advanced Digital Media Boost	Hides men Accelerate	nory late s execut	ncy ion of Strear	ning SIM	D Extensior	n (SSE2/3)	instruction			licatio	ns
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost	Hides men Accelerate Streaming	nory late s execut SIMD E	ncy ion of Strear xtensions 4 (	ning SIM (SSE4) a	D Extensior	n (SSE2/3)	instruction			licatic	ns
Intel Smart Memory Access Intel Advanced Digital Media Boost	Hides men Accelerate Streaming Enhanced Coordinate	nory late s execut SIMD E Intel Spe es Enhar	ncy ion of Strear xtensions 4 ( eedStep® teo nced Intel Sp	ning SIM (SSE4) a chnology eedStep	D Extensior nd faster Su ™ Technolog	n (SSE2/3) uper Shuffle	instruction Engine		ltimedia app		ins
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination	Hides men Accelerate Streaming Enhanced Coordinate indepe	nory late s execut SIMD E Intel Spe es Enhar ndently	ncy ion of Strear xtensions 4 ( eedStep® teo nced Intel Sp per core to h	ning SIM (SSE4) a chnology eedStep elp save	D Extensior nd faster Su ™ Technolog power	n (SSE2/3) uper Shuffle gy and idle	instruction Engine power-ma	s used in mul nagement sta	timedia app te transition		ins
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power	nory late s execut SIMD E Intel Spe s Enhar ndently	ncy ion of Strear xtensions 4 ( eedStep® teo nced Intel Sp per core to h at allows bot	ning SIM (SSE4) a chnology eedStep elp save	D Extensior nd faster Su ™ Technolog power	n (SSE2/3) uper Shuffle gy and idle	instruction Engine power-ma	s used in mul nagement sta	timedia app te transition		ns
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management	Hides men Accelerate Streaming Enhanced Coordinate indepe	nory late s execut SIMD E Intel Spe s Enhar ndently	ncy ion of Strear xtensions 4 ( eedStep® teo nced Intel Sp per core to h at allows bot	ning SIM (SSE4) a chnology eedStep elp save	D Extensior nd faster Su ™ Technolog power	n (SSE2/3) uper Shuffle gy and idle	instruction Engine power-ma	s used in mul nagement sta	timedia app te transition		ns
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No	nory late s execut SIMD E Intel Spe s Enhar ndently state th mal sen	ncy ion of Strear xtensions 4 ( eedStep® teo nced Intel Sp per core to h at allows bot sor	ning SIM (SSE4) a chnology eedStep elp save th cores a	D Extensior nd faster Su ™ Technolog power and L2 cach	n (SSE2/3) uper Shuffle gy and idle ne to be pov	instruction Engine power-mai vered dow	s used in mul nagement sta n when proce	timedia app te transition essor idle		ins
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread	nory late s execut SIMD E Intel Spe es Enhar ndently p r state th rmal sen Is (two c	ncy ion of Strear xtensions 4 ( eedStep® teo nced Intel Sp per core to h at allows bot sor	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-T	D Extensior nd faster Su ™ Technolog power and L2 cach hreading su	n (SSE2/3) uper Shuffle gy and idle ne to be pov pport provi	instruction Engine power-mai vered dow de two logi	s used in mul nagement sta	timedia app te transition essor idle		ns
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads	Hides men Accelerate Streaming Enhanced Coordinate indepe Low-power Digital ther No Two thread Protects m Intel 64 Ter	nory late s execut SIMD E: Intel Spe s Enhar ndently state th mal sen is (two c emory d chnology	ncy ion of Strear xtensions 4 ( eedStep® teo ced Intel Sp per core to h at allows bot sor ores with no lata areas fro (an extension)	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-T om malici on to the	D Extension nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e executior	instruction Engine power-mai vered dow de two logi	s used in mul nagement sta n when proce	timedia app te transition essor idle		ins
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup>	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread Protects m Intel 64 Ter 64-bit	nory late s execut SIMD E Intel Spe s Enhar ndently s state th mal sen ds (two c emory d chnology extension	ncy ion of Strear xtensions 4 ( eedStep® teo nced Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extensions to the x86	ning SIM (SSE4) a hnology eedStep elp save th cores a Hyper-T om malici on to the architec	D Extension nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e executior	instruction Engine power-mai vered dow de two logi	s used in mul nagement sta n when proce	timedia app te transition essor idle		ins
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> Virtualization Technology	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two threac Protects m Intel 64 Ter 64-bit Intel Virtua	nory late s execut SIMD E Intel Spa s Enhar ndently s state th mal sen ds (two c emory d chnology extension lization	ncy ion of Strear xtensions 4 ( eedStep® teo ced Intel Sp per core to h at allows bot sor ores with no lata areas fro (an extensions to the x86 Technology (	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the architec VT)	D Extensior nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru ture)	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e executior uction set w	instruction Engine power-mai vered dow de two logi hich adds	s used in mul nagement sta n when proce	timedia app te transition essor idle rs)	S	ins
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup>	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-powel Digital then No Two thread Protects m Intel 64 Ter 64-bit o Intel Virtua Intel Dynai	nory late s execut SIMD E Intel Spa s Enhar ndently i state th mal sen is (two c emory d chnology extension lization mic Acce	ncy ion of Strear xtensions 4 ( eedStep® teo ceed Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extension ns to the x86 Technology ( eleration (IDA	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the carchitec VT)	D Extension nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e executior uction set w deliver extu	instruction Engine power-mai vered dow de two logi hich adds ra performa	s used in mul nagement sta n when proce	timedia app te transition essor idle rs) her core is i	s dle	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Dynamic Accerelation	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread Protects m Intel 64 Te 64-bit Intel Virtua Intel Dynai Provides a	hory late s execut SIMD E Intel Spo s Enhar ndently state th mal sen ls (two c emory d chnology extension lization mic Acce more se	ncy ion of Strear xtensions 4 ( eedStep® teo ceed Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extension ns to the x86 Technology ( eleration (IDA	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the 6 architec VT) a) allows m with pr	D Extension nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru ture) one core to otection from	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e executior uction set w deliver exter m software	instruction Engine power-man wered dow de two logi hich adds ra performa based atta	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT	timedia app te transition essor idle rs) her core is i	s dle	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT)	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread Protects m Intel 64 Ter 64-bit Intel Virtua Intel Dynai Provides a 64KB per o 2x32KB da	hory late s execut SIMD E: Intel Spo se Enhar ndently f state th mal sen ds (two c emory d chnology extension lization mic Acce more se core split tat cache	ncy ion of Strear xtensions 4 ( eedStep® tech nced Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extension ns to the x86 Technology ( eleration (IDA ecure platform t between da e, integrated	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the 5 architec VT) a with pr ta cache	D Extension nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru ture) one core to otection from	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e executior uction set w deliver exter m software	instruction Engine power-man wered dow de two logi hich adds ra performa based atta	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT	timedia app te transition essor idle rs) her core is i	s dle	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread Protects m Intel 64 Ter 64-bit Intel Virtua Intel Dynai Provides a 64KB per o 2x32KB da	hory late s execut SIMD E: Intel Spo se Enhar ndently f state th mal sen ds (two c emory d chnology extension lization mic Acce more se core split tat cache	ncy ion of Strear xtensions 4 ( eedStep® tech nced Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extension ns to the x86 Fechnology ( eleration (IDA ecure platform t between da	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the 5 architec VT) a with pr ta cache	D Extension nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru ture) one core to otection from	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e executior uction set w deliver exter m software	instruction Engine power-man wered dow de two logi hich adds ra performa based atta	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT	timedia app te transition essor idle rs) her core is i	s dle	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread Protects m Intel 64 Te 64-bit d Intel Virtua Intel Dynar Provides a 64KB per o 2x32KB da 2x32KB in:	nory late s execut SIMD E: Intel Spa- se Enhar ndently   state th mal sen ls (two c emory d chnology extension lization inic Acce more second struction , or <b>6ME</b>	ncy ion of Strear xtensions 4 ( eedStep® tech need Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extensi- ns to the x86 Technology ( eleration (IDA ecure platforr t between da e, integrated cache, integ	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the architec VT) allows m with pr ta cache grated shared b	D Extension nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e executior uction set w deliver extu m software- d instuction h cores (Int	instruction Engine power-main wered dow de two logi hich adds ra performa based atta cache (32 rel Advance	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT	timedia app te transition essor idle rs) her core is i e-enabled OS	s dle 3 or ap	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 instruction cache L2 cache - size L2 cache - data path	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-powel Digital then No Two threac Protects m Intel 64 Ter 64-bit of Intel Virtua Intel Dynai Provides a 64KB per of 2x32KB da 2x32KB da 2x32KB da	hory late s execut SIMD E Intel Spa is Enhar indently s state the mal sen is (two c emory d chnology extension lization mic Acce more set truction , or <b>6ME</b>	ncy ion of Strear xtensions 4 ( eedStep® teo ceed Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extensions to the x86 Technology ( eleration (IDA ecure platform t between da e, integrated cache, integrated s, full speed, 32 bytes), 64	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the carchitec VT) a) allows m with pr ta cache grated shared b byte cac	D Extension nd faster Su "M Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and the line size	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e execution uction set w deliver extu m software- d instuction h cores (Int e, 8-way set	instruction Engine power-main vered dow de two logi hich adds ra performa based atta cache (32 rel Advanci associativ	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac e, integrated,	timedia app te transition essor idle rs) her core is i -enabled OS che) unified (on	s dle 3 or aj die)	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology Virtualization Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 instruction cache L2 cache - size	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-powel Digital then No Two threac Protects m Intel 64 Ter 64-bit o Intel Virtua Intel Dynai Provides a 64KB per o 2x32KB da 2x32KB in: 256-bit dat	hory late s execut SIMD E Intel Spa s Enhar ndently   s state th mal sen ls (two c emory d chnolog) extension lization mic Acce more set truction , or 6ME a path (3 r 1066MI	ncy ion of Strear xtensions 4 ( eedStep® teo ceed Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extensions to the x86 Technology ( eleration (IDA ecure platform t between da e, integrated cache, integrated s, full speed, 32 bytes), 64	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the carchitec VT) allows m with pr ta cache grated shared b byte cac	D Extension nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and the line size mes per clo	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e execution uction set w deliver exti m software- d instuction h cores (Int s, 8-way set pock), addres	instruction Engine power-main wered dow de two logi hich adds ra performa based atta cache (32 rel Advanci associativ s bus tran	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac	timedia app te transition essor idle rs) her core is i -enabled OS che) unified (on	s dle 3 or aj die)	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 data cache L2 cache - size L2 cache - data path System bus (front side bus)	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-powel Digital then No Two threac Protects m Intel 64 Ter 64-bit o Intel Virtua Intel Dynai Provides a 64KB per o 2x32KB da 2x32KB in: 256-bit dat	hory late s execut SIMD E Intel Spa s Enhar ndently   s state th mal sen ls (two c emory d chnolog) extension lization mic Acce more set tore split ta cache struction , or <b>6ME</b> a path (3 r <b>1066M</b> hory add	ncy ion of Strear xtensions 4 ( eedStep® teo ceed Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extensions to the x86 Technology ( eleration (IDA ecure platform t between da e, integrated cache, integ 8, full speed, 32 bytes), 64 Hz (transfers	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the carchitec VT) allows m with pr ta cache grated shared b byte cac	D Extension nd faster Su ™ Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and the line size mes per clo	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e execution uction set w deliver exti m software- d instuction h cores (Int s, 8-way set pock), addres	instruction Engine power-main wered dow de two logi hich adds ra performa based atta cache (32 rel Advanci associativ s bus tran	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac e, integrated,	timedia app te transition essor idle rs) her core is i -enabled OS che) unified (on	s dle 3 or aj die)	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 data cache L2 cache - size L2 cache - data path System bus (front side bus) Memory addressability	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital then No Two threac Protects m Intel 64 Ter 64-bit Intel Virtua Intel Oynar Provides a 64KB per of 2x32KB da 2x32KB da 2x32KB da 2x32KB da 256-bit dat	hory late s execut SIMD E Intel Spe s Enhar ndently s state th mal sen ds (two c emory d chnology extension lization mic Acce more se core split at a cache struction , or <b>6ME</b> a path (3 r <b>1066M</b>	ncy ion of Strear xtensions 4 ( eedStep® teo ceed Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extensions to the x86 Technology ( eleration (IDA ecure platform t between da e, integrated cache, integ 8, full speed, 32 bytes), 64 Hz (transfers	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the architec VT) allows m with pr ta cache shared b byte cac data 4 ti out limited	D Extension Ind faster Su Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and between both the line size mes per clo d by chipset	h (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e execution action set w deliver extr m software- d instuction h cores (Inf -, 8-way set ck), addres ), 36-bit ad	instruction Engine power-main wered dow de two logi hich adds ra performa based atta cache (32 rel Advanci associativ s bus tran	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac e, integrated,	timedia app te transition essor idle rs) her core is i -enabled OS che) unified (on	s dle 3 or aj die)	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 data cache L2 cache - size L2 cache - data path System bus (front side bus) Memory addressability System bus - width Execution units per core Math coprocessor	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-powel Digital ther No Two thread Protects m Intel 64 Ter 64-bit Intel Virtua Intel Virtua Intel Dynar Provides a 64KB per of 2x32KB da 2x32KB da 2x32KB da 2x32KB da 256-bit dat <b>800MHz</b> of 64GB men 64-bit data 2 integer u Pipelined f	hory late s execut SIMD E Intel Spa is Enhar indently is state the mal sen is (two c emory d chnology extension lization mic Acce more se inter Acce struction , or <b>6ME</b> a path (3 r <b>1066M</b> nory add path nits, 1 fid loating p	ncy ion of Strear xtensions 4 ( eedStep® teo ceed Intel Sp per core to h at allows bot sor ores with no lata areas fro / (an extensions to the x86 Technology ( eleration (IDA ecure platform t between da e, integrated cache, integrated cache, integrated s2 bytes), 64 Hz (transfers Iressability (b conting point to point unit	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the architec VT) allows m with pr ta cache grated shared b byte cac data 4 ti out limited units, 1 lc	D Extension Ind faster Su Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and between both the line size mes per clo d by chipset	h (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e execution action set w deliver extr m software- d instuction h cores (Inf -, 8-way set ck), addres ), 36-bit ad	instruction Engine power-main wered dow de two logi hich adds ra performa based atta cache (32 rel Advanci associativ s bus tran	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac e, integrated,	timedia app te transition essor idle rs) her core is i -enabled OS che) unified (on	s dle 3 or aj die)	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology Intel Dynamic Accerelation Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 data cache L2 cache - size L2 cache - size L2 cache - data path System bus (front side bus) Memory addressability System bus - width Execution units per core Math coprocessor Compatibility	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread Protects m Intel 64 Te 64-bit d Intel Virtua Intel Dynar Provides a 64KB per o 2x32KB da 2x32KB da 2x32KB da 2x32KB in: <b>2MB, 3MB</b> 256-bit data <b>800MHz</b> o 64GB men 64-bit data 2 integer u Pipelined f	hory late s execut SIMD E Intel Spa is Enhar indently is state the mal sen is (two c emory d chnology extension lization mic Acce more se inter Acce struction , or <b>6ME</b> a path (3 r <b>1066M</b> nory add path nits, 1 fid loating p	ncy ion of Strear xtensions 4 ( eedStep® teo ced Intel Sp per core to h at allows bot sor ores with no lata areas fro (an extensions to the x86 Technology ( eleration (IDA ecure platforr t between da e, integrated cache, integ 32 bytes), 64 Hz (transfers Iressability (b coating point of	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the architec VT) allows m with pr ta cache grated shared b byte cac data 4 ti out limited units, 1 lc	D Extension Ind faster Su Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and between both the line size mes per clo d by chipset	h (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e execution action set w deliver extr m software- d instuction h cores (Inf -, 8-way set ck), addres ), 36-bit ad	instruction Engine power-main wered dow de two logi hich adds ra performa based atta cache (32 rel Advanci associativ s bus tran	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac e, integrated,	timedia app te transition essor idle rs) her core is i -enabled OS che) unified (on	s dle 3 or aj die)	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 instruction cache L2 cache - size L2 cache - size L2 cache - size L2 cache - data path System bus (front side bus) Memory addressability System bus - width Execution units per core Math coprocessor Compatibility Process technology	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread Protects m Intel 64 Te 64-bit d Intel Virtua Intel Dynau Provides a 64KB per o 2x32KB da 2x32KB da	nory late s execut SIMD E. Intel Spase s Enhar ndently f state the mal sen is (two c emory d chnology extension lization inc Acce more secore split ata cache struction , or <b>6ME</b> a path (S r <b>1066M</b> nory add path nits, 1 flo	ncy ion of Strear xtensions 4 ( eedStep® tech need Intel Sp per core to h at allows bot sor ores with no lata areas fro ( an extensi- ns to the x86 Fechnology ( eleration (IDA ecure platform t between da e, integrated cache, integ 3, full speed, 32 bytes), 64 Hz (transfers iressability (t	ning SIM (SSE4) a chnology eedStep elp save th cores a m malici on to the architec VT) allows m with pr ta cache grated shared b byte cac data 4 ti out limitec	D Extension Ind faster Su Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and between both the line size mes per clo d by chipset	h (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e execution action set w deliver extr m software- d instuction h cores (Inf -, 8-way set ck), addres ), 36-bit ad	instruction Engine power-main wered dow de two logi hich adds ra performa based atta cache (32 rel Advanci associativ s bus tran	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac e, integrated,	timedia app te transition essor idle rs) her core is i -enabled OS che) unified (on	s dle 3 or aj die)	
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 data cache L2 cache - size L2 cache - size L2 cache - size L2 cache - data path System bus (front side bus) Memory addressability System bus - width Execution units per core Math coprocessor Compatibility Process technology Thermal Design Power	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital then No Two threac Protects m Intel 64 Ter 64-bit Intel Virtua Intel Oynar Provides a 64KB per of 2x32KB da 2x32KB da	hory late s execut SIMD E: Intel Spe s Enhar ndently f s state th mal sen is (two c emory d chnology extension lization mic Acce more se core split at a cache struction , or <b>6ME</b> nory add path nits, 1 fic loating p e with IA watts; <i>T</i> .	ncy ion of Strear xtensions 4 ( eedStep® teo need Intel Sp per core to h at allows bot sor ores with no lata areas fro (an extensions to the x86 Technology ( eleration (IDA ecure platforr t between da e, integrated cache, integ B, full speed, 32 bytes), 64 Hz (transfers Iressability (b coating point to cont unit -32 software	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the architec VT) allows m with pr ta cache shared b byte cac data 4 ti out limited units, 1 lc	D Extension Ind faster Su Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and between bot the line size mes per clo d by chipset wad unit, 1 s	h (SSE2/3) uper Shuffle gy and idle he to be pow pport provi e executior uction set w deliver extr m software- d instuction h cores (Inf -, 8-way set rock), addres ), 36-bit ad	instruction Engine power-main vered dow de two login hich adds ra perform: based atta cache (32 rel Advancia associativ ass bus tran dressing	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac e, integrated, sfers at 2 time	timedia app te transition essor idle rs) her core is i cenabled OS che) unified (on es per clock	s dle 3 or a <sub>l</sub> die)	ppl
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 data cache L2 cache - size L2 cache - size L2 cache - size L2 cache - data path System bus (front side bus) Memory addressability System bus - width Execution units per core Math coprocessor Compatibility Process technology Thermal Design Power	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread Protects m Intel 64 Ter 64-bit of Intel Virtua Intel Virtua Intel Dynar Provides a 64KB per of 2x32KB da 2x32KB da 2x32	hory late s execut SIMD E: Intel Spe s Enhar Indently f s state th mal sen ds (two c emory d chnology extension lization mic Acce more se core split at a cache struction , or <b>6ME</b> a path (S r <b>1066M</b> nory add path nits, 1 ft loating p e with IA	ncy ion of Strear xtensions 4 ( eedStep® teo ced Intel Sp per core to h at allows bot sor ores with no lata areas fro (an extensions to the x86 Technology ( eleration (IDA ecure platforr t between da e, integrated cache, integ B, full speed, 32 bytes), 64 Hz (transfers Iressability (b coating point to coating p	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the architec VT) allows m with pr ta cache grated shared b byte cac data 4 ti out limited units, 1 lc	D Extension Ind faster Su I <sup>™</sup> Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and between bot the line size mes per clo d by chipset bad unit, 1 s	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e execution action set w deliver exti m software- d instuction h cores (Int s, 8-way set ck), addres ), 36-bit ad tore unit	instruction Engine power-main vered dow de two logi hich adds ra performation based attra- cache (32 rel Advance associativ s bus tran dressing	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac e, integrated, sfers at 2 time	timedia app te transition essor idle rs) her core is i enabled OS the) unified (on es per clock	s dle s or a die)	ppl
Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power management technology Intel Dynamic Power Coordination Intel Deep Power Down Technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT) L1 cache L1 data cache L1 instruction cache L2 cache - size L2 cache - size L2 cache - size L2 cache - data path System bus (front side bus) Memory addressability System bus - width Execution units per core Math coprocessor Compatibility Process technology	Hides men Accelerate Streaming Enhanced Coordinate indepe / Low-power Digital ther No Two thread Protects m Intel 64 Ter 64-bit of Intel Virtua Intel Virtua Intel Dynar Provides a 64KB per of 2x32KB da 2x32KB da 2x32	hory late s execut SIMD E: Intel Spe s Enhar ndently f s state th mal sen ds (two c emory d chnology extension lization mic Acce more se core split at a cache struction , or <b>6ME</b> a path (S r <b>1066M</b> nory add path nits, 1 ft loating p e with IA	ncy ion of Strear xtensions 4 ( eedStep® teo ced Intel Sp per core to h at allows bot sor ores with no lata areas fro (an extensions to the x86 Technology ( eleration (IDA ecure platforr t between da e, integrated cache, integ B, full speed, 32 bytes), 64 Hz (transfers Iressability (b coating point to coating p	ning SIM (SSE4) a chnology eedStep elp save th cores a Hyper-Ti om malici on to the architec VT) allows m with pr ta cache grated shared b byte cac data 4 ti out limited units, 1 lc	D Extension Ind faster Su I <sup>™</sup> Technolog power and L2 cach hreading su ous softwar IA-32 instru- ture) one core to otection from (32KB) and between bot the line size mes per clo d by chipset bad unit, 1 s	n (SSE2/3) uper Shuffle gy and idle ne to be pow pport provi e execution action set w deliver exti m software- d instuction h cores (Int s, 8-way set ck), addres ), 36-bit ad tore unit	instruction Engine power-main vered dow de two logi hich adds ra performation based attra- cache (32 rel Advance associativ s bus tran dressing	s used in mul nagement sta n when proce ical processor ance when ot acks with TXT KB) ed Smart Cac e, integrated, sfers at 2 time	timedia app te transition essor idle rs) her core is i enabled OS the) unified (on es per clock	s dle s or a die)	ppl

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

#### [Notebook] Intel Core 2 Duo Processor (SFF)

Intel <sup>®</sup> Core <sup>™</sup> 2 Duo processor Small Form Factor (SFF) for notebook systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Thermal Design Power	Intel HD Boost	Intel 64 Tech	Intel Dynamic Acceleration	Trusted Execution Tech (TXT)	Avail- able date
Intel Core 2 Duo processor SU9300	1.20GHz	3MB	800MHz	Dual	10W	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SU9400	1.40GHz	3MB	800MHz	Dual	10W	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SL9300	1.60GHz	6MB	1066MHz	Dual	17W	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SL9400	1.86GHz	6MB	1066MHz	Dual	17W	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SP9300	2.26GHz	6MB	1066MHz	Dual	25W	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SP9400	2.40GHz	6MB	1066MHz	Dual	25W	Yes	Yes	Yes	Yes	Aug 2008

#### Small Form Factor (SFF) notebook processors

- SUxxxx = Ultra Low Voltage
  SLxxxx = Low Voltage
  SPxxxx = Power Optimized Performance

Processor generation	Penryn (Montevina)
Marketing name	Intel Core 2 Duo mobile processor
Core	Dual-core
Branding	Supports Intel Centrino <sup>®</sup> 2 Processor Technology or Intel Centrino 2 with vPro Processor Technology when hardware and software requirements met
Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power management technology	Enhanced Intel SpeedStep® technology
Intel Dynamic Power Coordination	Coordinates Enhanced Intel SpeedStep™ Technology and idle power-management state transitions independently per core to help save power
Intel Dynamic Bus Parking	Enables platform power savings and improved battery life by allowing the chipset to power down with the processor in low-frequency mode
Enhanced Intel Deeper Sleep with Dynamic Cache Sizing	Saves power by flushing cache data to system memory during periods of inactivity to lower CPU voltage
	/ Low-power state that allows both cores and L2 cache to be powered down when processor idle
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology <sup>1</sup>	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64-bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology (VT)
Intel Dynamic Accerelation Intel Trusted Execution Tech (TXT)	Intel Dynamic Acceleration (IDA) allows one core to deliver extra performance when other core is idle Provides a more secure platform with protection from software-based attacks with TXT-enabled OS or appl
L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache, integrated
L1 instruction cache	2x32KB instruction cache, integrated
L2 cache - size L2 cache - data path L3 cache	<b>3MB</b> or <b>6MB</b> , full speed, shared between both cores (Intel Advanced Smart Cache) 256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die) None
System bus (front side bus) Memory addressability System bus - width	<b>800MHz</b> or <b>1066MHz</b> (transfers data 4 times per clock), address bus transfers at 2 times per clock 64GB memory addressability (but limited by chipset), 36-bit addressing 64-bit data path
Execution units per core Math coprocessor Compatibility	2 integer units, 1 floating point units, 1 load unit, 1 store unit Pipelined floating point unit Compatible with IA-32 software
Process technology Thermal Design Power Package and connector Chipset support	45nm <i>SUxxxx</i> : 10 watts; <i>SLxxxx</i> : 17 watts; <i>SUxxxx</i> : 25 watts <b>Socket P</b> / Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball) <b>Mobile Intel 4 Series Chipset family</b> ; other compatible chipsets

### [Notebook] Intel Core 2 Quad Processor

Intel® Core™ 2 Quad processor for notebook systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Thermal Design Power	Virtual- ization Tech	Intel 64 Tech	Intel Dynamic Acceleration	Trusted Execution Tech (TXT)	Avail- able date
Intel Core 2 Quad processor Q9000 Intel Core 2 Quad processor Q9100			1066MHz 1066MHz	Quad Quad	45W 45W	Yes Yes	Yes Yes	Yes Yes	No No	Dec 2008 Aug 2008
	D (14		<u>,</u>							
0	Penryn (M		,							
0	Quad-core		mobile proc	essor						
			trine® 2 Dre	T	'aabaalaan	or Intel Co				hnology
Branding			and software					with vPro Pro	Jeesson red	innology
Micro-architecture	Intel Core i			requiren	ients met					
				our full in	etructione e	imultanoou		14 stago pipo	lino	
	Hides men				Structions s	sinullaneou	siy using	14-stage pipe	line	
Intel Advanced Digital Media Boost						0 (SSE2/3)	instruction	e used in mu	ltimodia anr	lications
			xtensions 4 (							lications
	0		edStep <sup>®</sup> tec	,		aper Snume	Engine			
0 0,					M Technolo	av and idle	nower-ma	nagement sta	to transition	ne -
			per core to he	•		gy and lule	power-ma	nagement sta		15
Intel Dynamic Bus Parking	Enables pla	atform p		and imp		ery life by al	lowing the	chipset to po	wer down w	vith the
Enhanced Intel Deeper Sleep with Dynamic Cache Sizing	Saves pow		shing cache		ystem men	nory during	periods of	inactivity		
Intel Deep Power Down Technology	Low-power	state th	at allows bot	h cores a	and L2 cach	ne to be pov	vered dow	n when proce	essor idle	
Thermal management	Digital ther	mal sen	sor							
51 0	No									
								ical processo	rs)	
			ata areas fro							
	64-bit e	extensio	(an extensions to the x86	architect		uction set w	hich adds			
			Fechnology (							
								ance when ot acks with TXT		
L1 cache	64KB per c	ore split	between dat	a cache	(32KB) and	d instuction	cache (32	KB)		
			e, integrated							
L1 instruction cache	2x32KB ins	struction	cache, integ	rated						
L2 cache - size	6MB or 12	MB. full	speed, share	d betwee	en cores (Ir	tel Advance	ed Smart (	Cache)		
								e, integrated,	unified (on	die)
•	None	• •		,						,
System bus (front side bus)	1066MHz (	transfer	s data 4 time	s per clo	ck), addres	s bus transf	ers at 2 tir	nes per clock		
			ressability (b					-		
System bus - width	64-bit data	path				,	•			
Execution units per coro	2 integar ···	nite 1 fl	ating point u	nite 1 la	ad unit 1 a	toro unit				
	Pipelined fl		pating point u	110	au unit, TS					
			-32 software							
	•									
0,	45nm									
	45 watts	N		<b>∼</b>			170	in ourferer	unt 7 1	
								in surface mo		
	· · · ·	socket	(IIIPGA479M	SOCKET)		ip-Unip Ball	Grid Arra	y (Micro-FCB	GA) for surf	ace mount
	(479-ball)		os Chinast	amily	thar comes	tiblo obines	to			
Chipset support	mobile inte	ei 4 Seri	es Chipset f	anniy, 0	mer compa	uble chipse	15			

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

(C2QUAD) Compiled by Roger Dodson, Lenovo. December 2008

### [Notebook] Intel Core 2 Extreme Processor

Intel <sup>®</sup> Core™ 2 Extreme processor for notebook systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core		ization	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Intel Dynamic Acceleration	Trusted Execution Tech (TX1	
Intel Core 2 Extreme processor X7800 Intel Core 2 Extreme processor X7900			800MHz 800MHz	Dual Dual	No No	Yes Yes	Yes Yes	Yes Yes	No No		July 2007 Aug 2007
Intel Core 2 Extreme processor X9000 Intel Core 2 Extreme processor X9100			800MHz 1066MHz	Dual Dual	Yes Yes	Yes Yes	Yes Yes	Yes Yes	No No		Jan 2008 July 2008
Intel Core 2 Extreme processor QX9300	) 2.53GHz	2 12MB	1066MHz	Quad	Yes	Yes	Yes	Yes	Yes	No	Aug 2008

Processor generation Marketing name Core(s) Branding	X7800/X7900: Merom (Santa Rosa); X9000/X9100: Penryn (Santa Rosa Refresh); QX9300: Penryn Intel Core 2 Extreme processor Dual-core or quad-core Intel's highest performance brand for processors
Micro-architecture Intel Wide Dynamic Execution	Intel Core micro-architecture Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel HD Boost Power mgmt technology Thermal management	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications <i>X9000/X9100/QX9300:</i> Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine Enhanced Intel SpeedStep™ technology Digital thermal sensor
Hyper-Threading	No
Total threads Execute Disable (XD) Bit	Two threads (two cores with no Hyper-Threading support provide two logical processors) Protects memory data areas from malicious software execution
Intel 64 Technology <sup>1</sup> (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds
	64 bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology
Intel Dynamic Accerlation	Some: Intel Dynamic Acceleration (IDA) allows one core to deliver extra performance when other core is idle
Intel Trusted Execution Tech (TXT)	Some: Provides a more secure platform from software-based attacks with TXT-enabled OS or appl
L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache, integrated
L1 instruction cache	2x32KB instruction cache, integrated
L2 cache - size	4MB, 6MB, or 12MB, full speed, shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None
System bus	800MHz or 1066MHz (transfers data 4 times per clock), address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset), 36-bit addressing
System bus - width	64-bit data path
Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	X7800/X7900: 65nm; X9000/X9100/QS9300: 45nm
Thermal Design Power	44 or 45 watts
Package and connector	<b>Socket P</b> / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount
Chipset support	(479-ball) Mobile Intel 965 Express Chipset family; other compatible chipsets
All trademarks are the property of the	

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

(XM) Compiled by Roger Dodson, Lenovo. August 2008

### [Desktop] Intel Celeron Processor 4xx

Intel <sup>®</sup> Celeron <sup>®</sup> Processor	Clock Perf Mode	L2	System bus MHz	Т		Total threads (logical)	ization	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Truste Executi Tech		Avail- able date
Intel Celeron Processor 420	1.60GHz	512KB	800MHz	Single	No	1	No	Yes	No	Yes	No	Jun	2007
Intel Celeron Processor 430	1.80GHz	512KB	800MHz	Single	No	1	No	Yes	No	Yes	No	Jun	2007
Intel Celeron Processor 440	2.00GHz	512KB	800MHz	Single	No	1	No	Yes	No	Yes	No	Jun	2007
Intel Celeron Processor 450	2.20GHz	512KB	800MHz	Single	No	1	No	Yes	No	Yes	No	Aug	2008
Processor generation		roe-L											
Marketing name			n Process	sor									
Core	•	gle-core											
Branding	Valu	ie or ess	ential desl	ktop prod	cessor								
Micro-architecture			icro-archit		· · · · · · ·								
Intel Wide Dynamic Execution					four fuil ir	nstructior	is simult	aneousiy	using 14-stage	pipeline;			
Intel Smart Memory Access			ry latency		mina SIN		nion (SS	E2/2) inct	ructions used i	n multime	dia ann	licoti	200
Intel Advanced Digital Media E			d Intel Spe		-		5011 (55	EZ/3) IIISI		mulume	sula app	licali	5115
Power mgmt technology Thermal management			al sensor	eeusiep	lecino	logy							
Hyper-Threading	No												
Total threads		thread											
Execute Disable (XD) Bit			mory data	orooo fr	om molio	ious ooft	voro ovo	oution					
									h adda				
Intel 64 Technology <sup>1</sup> (EM64T)			nology (ar				Silucion	Set Which	lauus				
Intel Virtualization Technology	No				mieciule	•)							
Intel Trusted Execution Techno													
L1 cache	64K	B per co	re split be	tween da	ata cache	e (32KB) ;	and instu	uction cac	che (32KB)				
L1 data cache	2x32	2KB data	a cache / ii	ntegrated	t	. ,			. ,				
L1 instruction cache	2x32	2KB insti	ruction cad	che / inte	grated								
L2 cache - size	512	KB / full	speed										
L2 cache - data path L3 cache	256 <sup>.</sup> Non		path (32 b	oytes) / 6	4 byte ca	iche line	size / 8-\	way set as	ssociative / inte	grated / u	unified (c	on die	e)
				4.1									
System bus					•	,			at 2 times per c	CIOCK			
Memory addressability			ry addres	sability (I	but limite	d by chip	set) / 36	-bit addre	essing				
System bus - width	64-b	oit data p	ath										
Execution units			ts, 1 floati		units, 1 lo	oad unit,	1 store ι	unit					
Math coprocessor	•		ating point										
Compatibility	Con	npatible	with IA-32	software	9								
Process technology		m or 0.00	65u										
Thermal Design Power		vatts	<b>.</b>		•		、 .			• • • •			
Package and connector				and Grid	Array (F	-C-LGA6	) packa	ge require	es LGA775 soc	cket (soch	ket also		
Chipset support		ed Socke I 3 Serie	,	s Chipse	et family	; Intel 94	5 and 96	5 Expres	s Chipset family	y; other c	ompatib	le chi	psets
All trademarks are the property of	6 41 1							1) Compile	ed by Roger Doc				000

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

(CEL4) Compiled by Roger Dodson, Lenovo. September 2008

### [Desktop] Intel Celeron Processor

Intel® Celeron® Processor	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	HD Boost	Virtual- ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Trusted Execution Tech	Avail- able date
Intel Celeron Processor E1200	1.60GHz	512KB	800MHz	Dual	No	No	Yes	Yes	Yes	No	Jan 2008
Intel Celeron Processor E1400	2.00GHz	512KB	800MHz	Dual	No	No	Yes	Yes	Yes	No	Apr 2008
Intel Celeron Processor E1500	2.20GHz	512KB	800MHz	Dual	No	No	Yes	Yes	Yes	No	Dec 2008
Processor generation	Conro										
Marketing name			Processor								
Core	Dual-o										
Branding	Value	or essen	tial deskto	p proce	essor						
Micro-architecture	Intel C	ore Micr	o-architect	ture							
Intel Wide Dynamic Execution			•	up to fo	ur full ins	tructions	simultaneo	ously using 14-s	tage pipel	ine;	
Intel Smart Memory Access		memory		~		<b>-</b> · ·	1005010	· · ·			
Intel Advanced Digital Media Boo							n (SSE2/3	<ol><li>Instructions us</li></ol>	sed in mul	timedia app	lications
Power mgmt technology		icea Intel	SpeedSte	ep™ tec	nnology (	EIST)					
Hyper-Threading	No										
Execute Disable (XD) Bit			ory data ar								
Intel 64 Technology <sup>1</sup> (EM64T)			ns to the x			A-32 instr	uction set	which adds			
Intel Virtualization Technology	No	exterioro			neoturo)						
Intel Trusted Execution Technology											
L1 cache	64KB	per core	split betwe	een dat	a cache (	32KB) an	d instuctio	n cache (32KB)			
L1 data cache			ache / inte			,		()			
L1 instruction cache			tion cache	0	rated						
L2 cache - size	512KE	<b>3</b> / full sp	eed / shar	ed betw	een both	cores (In	tel Advano	ced Smart Cach	e)		
L2 cache - data path								set associative /		d / unified (c	on die)
System bus	800MI	Hz (trans	fers data 4	times	per clock)	/ addres	s bus tran	sfers at 2 times	per clock		
Memory addressability					· · ·			addressing '			
System bus - width	64-bit	data patl	า			, ,	,	0			
Execution units	2 intec	aer units.	1 floating	point u	nits. 1 loa	d unit. 1 s	store unit				
Math coprocessor			ng point u		,	,					
Compatibility			h IA-32 so								
Process technology	65nm	or 0.065	u								
Thermal Design Power	65 wat		-								
Package and connector	775-la		•	d Grid A	Array (FC	-LGA6) p	ackage re	equires LGA775	socket (s	socket also	
Chipset support			) ess Chip:								

All trademarks are the property of their respective owners © Lenovo (DCEL) Compiled by Roger Dodson, Lenovo. January 2009

### [Desktop] Intel Pentium Processor

Intel® Pentium® Processor	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Hyper- Threading Technology	Total threads (logical)	Virtual- ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Truste Executio Tech	
Intel Pentium Processor E2140	1.60GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Jun 2007
Intel Pentium Processor E2160	1.80GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Jun 2007
Intel Pentium Processor E2180	2.00GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Aug 2007
Intel Pentium Processor E2200	2.20GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Dec 2007
Intel Pentium Processor E2220	2.40GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Mar 2008
Intel Pentium Processor E5200	2.50GHz	2MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Aug 2008
Intel Pentium Processor E5300	2.60GHz	2MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Dec 2008
Processor generation Marketing name			oe; <i>E5xxx</i> n Proces		fdale							
Core	Dual-											
Branding			ential desl	ktop p	rocessor							
Micro-architecture Intel Wide Dynamic Execution Intel Smart Memory Access Intel Advanced Digital Media Boo Power mgmt technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> (EM64T) Intel Virtualization Technology Intel Trusted Execution Technology Intel Trusted Execution Technology L1 cache L1 cache L1 data cache L1 instruction cache L2 cache - size L2 cache - data path	Each Hides Accel Enhai Digita No Two ti Prote Intel 6 64 bit No gy No 64KB 2x32P 2x32P 2x32P	core ca memo erates nced In I therm nreads cts mer 64 Tech extens per co (B data (B instr	ry latency execution tel Speed al sensor (two cores mory data nology (ar ions to the re split be a cache / in ruction cac	te up f of Strop™ s with areas n exte e x86 tween ntegra che / in ed / sh	to four full ir eaming SIM 4 technology no Hyper-T 6 from malici nsion to the architecture data cache ted ntegrated mared betwe	ID Extens / hreading ious soft IA-32 ins ) (32KB) ; en both o	sion (SSI support ware exe struction and instu	E2/3) inst	wo logical proc n adds	n multime essors)	edia appl	
L3 cache	None	il data		<i>y</i> (00)			0120701			grateare		
System bus Memory addressability System bus - width	64GB	•	ry addres		nes per cloc y (but limited	,			at 2 times per o ssing	clock		
Execution units Math coprocessor Compatibility	Pipeli	ned floa	ts, 1 floatin ating point with IA-32	t unit	nt units, 1 lo are	oad unit,	1 store u	nit				
Process technology Thermal Design Power Package and connector	65 wa <b>775-l</b> a	atts and Fli			rid Array (F	C-LGA6	) packaç	<b>je</b> require	es LGA775 soc	<b>:ket</b> (socł	ket also	
Chipset support		Socke	,	oset; I	ntel 4 Serie	s Expres	s Chipse	t family; o	ther compatible	e chipsets	S	

All trademarks are the property of their respective owners  $\circledast$  Lenovo

(E2) Compiled by Roger Dodson, Lenovo. January 2009

### [Desktop] Intel Core 2 Duo Processor

Intel <sup>®</sup> Core™ 2 Duo processor for desktop systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Hyper- Threading Technology	Virtual- ization Tech	Execute Disable Bit	Enhanced Inte SpeedStep™ Technology	64 Tech	Trusted Executio Tech	
Intel Core 2 Duo processor E4300	1.80GHz	2MB	800MHz	Dual	No	No	Yes	Yes	Yes	No	Jan 2007
Intel Core 2 Duo processor E4400	2.00GHz	2MB	800MHz	Dual	No	No	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor E4500	2.20GHz	2MB	800MHz	Dual	No	No	Yes	Yes	Yes	No	July 2007
Intel Core 2 Duo processor E4600	2.40GHz	2MB	800MHz	Dual	No	No	Yes	Yes	Yes	No	Oct 2007
Intel Core 2 Duo processor E4700	2.60GHz		800MHz	Dual	No	No	Yes	Yes	Yes	No	Mar 2008
Intel Core 2 Duo processor E6300	1.86GHz	2MB	1066MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor E6320	1.86GHz	4MB	1066MHz	Dual	No	Yes	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor E6400	2.13GHz		1066MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor E6420	2.13GHz		1066MHz		No	Yes	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor E6540	2.33GHz		1333MHz		No	Yes	Yes	Yes	Yes		July 2007
Intel Core 2 Duo processor E6550	2.33GHz		1333MHz	Dual	No	Yes	Yes	Yes	Yes		July 2007
Intel Core 2 Duo processor E6600	2.40GHz		1066MHz		No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor E6700	2.66GHz		1066MHz		No	Yes	Yes	Yes	Yes		July 2006
Intel Core 2 Duo processor E6750	2.66GHz		1333MHz		No	Yes	Yes	Yes	Yes		July 2007
Intel Core 2 Duo processor E6850	3.00GHz		1333MHz		No	Yes	Yes	Yes	Yes		July 2007
Processor generation Marketing name Core Branding	Conroe Intel Core 2 Dual-core Part of the I					and <b>Inte</b>	l vPro™ t	<b>echnology</b> fo	r busines	6	
Micro-architecture Intel Wide Dynamic Execution Intel Smart Memory Access Intel Advanced Digital Media Boost Power mgmt technology Thermal management Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology <sup>1</sup> (EM64T) Virtualization Technology Intel Trusted Execution Technology Intel Dynamic Acceleration	Hides memory Accelerates Enhanced II Digital therr No Two threads Protects me Intel 64 Tech 64 bit exten Some: Inte	an compory later execution ntel Spe nal sens (two co emory da hnology sions to I Virtuali	plete up to f ncy on of Strear edStep™ te or ores with no ata areas fro (an extensi the x86 arc zation Techi	ning S chnolo Hyper om ma on to t hitectu nology	IMD Extension ogy -Threading licious softwhe IA-32 inst ure)	sion (SSI support vare exe struction	E2/3) inst provide to cution set which	wo logical prod	in multim cessors)	edia appli	ications
L1 cache L1 data cache L1 instruction cache	64KB per co 2x32KB dat 2x32KB inst	a cache	, integrated		he (32KB) :	and instu	iction cac	he (32KB)			
L2 cache - size L2 cache - data path L3 cache								ed Smart Cacl ociative, integ	,	ified (on c	lie)
System bus	800MHz, 10 clock	066MHz	, or <b>1333MH</b>	l <b>z</b> (trar	nsfers data	4 times p	per clock)	/ address bus	transfers	at 2 time	es per
Memory addressability System bus - width	64GB mem 64-bit data j	•	essability (b	out limi	ited by chip	set), 36-	bit addres	sing			
Execution units Math coprocessor Compatibility	2 integer un Pipelined flo Compatible	pating po	pint unit		I load unit,	1 store u	ınit				
Process technology	65nm										
Thermal Design Power	65 watts										
Package and connector		• •	Land Grid	Array	(FC-LGA6	) packag	<b>ge</b> require	s LGA775 so	<b>cket</b> (soc	ket also	

All trademarks are the property of their respective owners  $\circledast$  Lenovo

(C2DE) Compiled by Roger Dodson, Lenovo. March 2008

### [Desktop] Intel Core 2 Duo Processor (Wolfdale)

Intel <sup>®</sup> Core <sup>™</sup> 2 Duo processor for desktop systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Virtual- ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Trusted Execution Tech	Intel Dynam Accelera	nic a	vail- able date
Intel Core 2 Duo processor E7200	2.53GHz	3MB	1066MHz	Dual	No	Yes	Yes	Yes	No	No	Apr	2008
Intel Core 2 Duo processor E7300	2.66GHz	3MB	1066MHz	Dual	No	Yes	Yes	Yes	No	No	Aug	2008
Intel Core 2 Duo processor E7400	2.80GHz	3MB	1066MHz	Dual	No	Yes	Yes	Yes	No	No	Oct	2008
Intel Core 2 Duo processor E8190	2.66GHz	6MB	1333MHz	Dual	No	Yes	Yes	Yes	No	No	Jan	2008
Intel Core 2 Duo processor E8200	2.66GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No	Jan	2008
Intel Core 2 Duo processor E8300	2.83GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No	Apr	2008
Intel Core 2 Duo processor E8400	3.00GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No	Jan	2008
Intel Core 2 Duo processor E8500	3.16GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No		2008
Intel Core 2 Duo processor E8600	3.33GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No	Мау	2008
Processor generation Marketing name	Wolfdale Intel Core 2	2 Duo di	eskton nro	005501								
Core	Dual-core	. Duo u										
Branding	Supports In	tel Core	2 Process	or wit	h Viiv™ te	echnolog	v and					
Dranding							hardware and s	software	requireme	ents met		
Micro-architecture	Intel Core M	licro-arc	hitecture									
Intel Wide Dynamic Execution	Each core c	an com	plete up to f	our full	instructio	ons simult	aneously using	g 14-stag	e pipeline	•		
Intel Smart Memory Access	Hides mem											
Intel Advanced Digital Media Boost				ming Sl	IMD Exte	nsion (SS	E2/3) instruction	ons used	l in multim	edia app	licatio	ons
Intel HD Boost							Shuffle Engine					
Power mgmt technology	Enhanced I	ntel Spe	edStep™ te	chnolo	gy	•	Ū.					
Hyper-Threading	No		•		0,							
Total threads	Two threads	(two co	ores with no	Hyper	-Threadir	ng suppor	t provide two lo	ogical pro	ocessors)			
Execute Disable (XD) Bit	Protects me	mory da	ata areas fro	om mal	icious so	ftware exe	ecution	•				
Intel 64 Technology <sup>1</sup>	Intel 64 Tecl 64 bit exten		<b>`</b>			nstructior	n set which add	ls				
Virtualization Technology	Some: Inte				16)							
Intel Trusted Execution Technology					e from ec	ftware-ba	sed attacks wi	th annro	oriato coft	ware		
Intel Dynamic Acceleration	None	DIES IIIO	ie secure p	auonn	5 110111 50	ntware-ba		ui appio	priate son	ware		
L1 cache	64KB per co	ore solit	between da	ta cacl	he (32KB	) and inst	uction cache (3	32KB)				
L1 data cache	2x32KB dat					,		,,				
L1 instruction cache	2x32KB inst											
L2 cache - size	3MB or 6MI	<b>3</b> , full sp	eed, share	d betwe	een both	cores (Int	el Advanced S	mart Cad	che)			
L2 cache - data path	256-bit data	path (3	2 bytes), 64	byte c	ache line	size, 8-w	ay set associa	tive, inte	grated, un	ified (on	die)	
L3 cache	None											
System bus (front side bus)							, address bus t		at 2 times	per cloc	k	
Memory addressability System bus - width	64GB mem 64-bit data		essability (l	out limit	ted by ch	ipset), 36	-bit addressing					
Execution units	2 integer un			units, 1	load unit	t, 1 store	unit					
Math coprocessor	Pipelined flo											
Compatibility	Compatible	with IA-	32 software									
Process technology	45nm											
Thermal Design Power	65 watts				(FO ·	<b>.</b> .			• • • •			
Package and connector	775-land Fl called Sock		Land Grid	Array	(FC-LGA	(8) packa	ge requires LG	6A775 S	ocket (soc	ket also		
Chipset support		,	ntel 4 Series	s Expre	ss Chips	et families	s; other compat	tible chip	sets			
				-								

All trademarks are the property of their respective owners © Lenovo (WOLF) Compiled by Roger Dodson, Lenovo. October 2008

### [Desktop] Intel Core 2 Extreme Processor

Intel <sup>®</sup> Core™ 2 Extreme processor for desktop systems	Clock Perf Mode	L2 cache	System bus MHz	Core	Thermal Design Power	Socket	Virtual- ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Avail- able date
Intel Core 2 Extreme processor X6800	2.93GHz	4MB	1066MHz	Dual	75W	LGA775	Yes	Yes	Yes	Yes	July 2006
Intel Core 2 Extreme processor QX670	0 2.66GHz	8MB	1066MHz	Quad	75W	LGA775	Yes	Yes	Yes	Yes	Apr 2007
Intel Core 2 Extreme processor QX680	0 2.93GHz	8MB	1066MHz	Quad	75W	LGA775	Yes	Yes	Yes	Yes	Apr 2007
Intel Core 2 Extreme processor QX685	0 3.00GHz	8MB	1333MHz	Quad	75W	LGA775	Yes	Yes	Yes	Yes	July 2007
Intel Core 2 Extreme processor QX965	0 3.00GHz	12ME	31333MHz	Quad	130W	LGA775	Yes	Yes	Yes	Yes	Nov 2007
Intel Core 2 Extreme processor QX977	'0 3.20GHz	12ME	81600MHz	Quad	136W	LGA775	Yes	Yes	Yes	Yes	Nov 2007
Intel Core 2 Extreme processor QX977	'5 3.20GHz	12ME	31600MHz	Quad	150W	LGA771	Yes	Yes	Yes	Yes	Feb 2008

Processor generation Marketing name Core Branding	Conroe (X6800) or Kentsfield (QX6xxx) or Yorkfield-XE (QX9xxx) Intel Core 2 Extreme processor Dual-core or quad-core Part of the Intel Viiv™ technology for the home and Intel vPro™ processor technology for business
Micro-architecture	Intel Core micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline;
Intel Smart Memory Access	Hides memory latency Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	QX9xxx: Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power mgmt technology	Enhanced Intel SpeedStep™ technology
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two or four threads (two or four cores with no Hyper-Threading)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology <sup>1</sup> (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds
	64 bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology
L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache / integrated
L1 instruction cache	2x32KB instruction cache / integrated
L2 cache - size	<ul> <li>X6800: 4MB / full speed / shared between both cores (Intel Advanced Smart Cache)</li> <li>QX6xxx: 8MB / full speed / 2 x 4MB shared cache on each die [dual-die] (Intel Advanced Smart Cache)</li> <li>QX9xxx: 12MB / full speed / 2 x 6MB shared cache on each die [dual-die] (Intel Advanced Smart Cache)</li> </ul>
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None
System bus	1066MHz or 1333MHz (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path
Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	Others: 65nm or 0.065u QX9xxx: 45nm or 0.045u
Package and connector	775-land Flip-Chip Land Grid Array (FC-LGA6) package requires LGA771 or LGA775 socket (also called Socket T)
Chipset support	Intel Q963, Q965, G965, P965, 975X Express Chipset families; Intel 3 Series; other compatible chipsets

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

(C2DX) Compiled by Roger Dodson, Lenovo. February 2008

### [Desktop] Intel Core 2 Quad Processor

Intel <sup>®</sup> Core™ 2 Quad processor for desktop systems	Clock Perf Mode	L2 cache	System bus MHz	Cores	Hyper- Threading Technology	threads	ization	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Trusted Executior Tech	Avail- able date
Intel Core 2 Quad processor Q6600 Intel Core 2 Quad processor Q6700			1066MHz 1066MHz		No No	4 4	Yes Yes	Yes Yes	Yes Yes	No No	Jan 2007 July 2007
Intel Core 2 Quad processor Q8200	) 2.33GHz	4MB	1333MHz	Quad	No	4	No	Yes	Yes	No	Aug 2008
Intel Core 2 Quad processor Q8300	2.50GHz	4MB	1333MHz	Quad	No	4	No	Yes	Yes	No	Dec 2008
Intel Core 2 Quad processor Q9300			1333MHz	Quad	No	4	Yes	Yes	Yes	Yes	Mar 2008
Intel Core 2 Quad processor Q9400			1333MHz		No	4	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Quad processor Q9450					No	4	Yes	Yes	Yes	Yes	Mar 2008
Intel Core 2 Quad processor Q9550					No	4	Yes	Yes	Yes	Yes	Mar 2008
Intel Core 2 Quad processor Q9650	) 3.00GHz	12MB	1333MHz	Quad	No	4	Yes	Yes	Yes	Yes	Aug 2008
Processor generation Marketing name			) or Yorkfie desktop p			x)					
Core						two Cor		processors joir	and toget	hor)	
Branding			e 2 Proces						ieu iogei		
branding								e and software	requirem	ents met	
Micro-architecture	Intel Core I	Micro-ar	chitecture								
Intel Wide Dynamic Execution	Each core	can com	plete up to	four ful	I instructior	ns simult	aneousl	y using 14-stag	e pipeline	e;	
Intel Smart Memory Access	Hides merr	nory late	ncy								
Intel Advanced Digital Media Boost	Accelerates	s execut	ion of Strea	ming S	IMD Exten	sion (SS	E2/3) in	structions used	in multin	nedia appl	ications
Intel HD Boost	Q8xxx/Q9x	xx: Stre	eaming SIM	D Exte	nsions 4 (S	SE4) an	d faster	Super Shuffle E	Ingine		
Power mgmt technology	Enhanced	Intel Spe	eedStep™ t	echnolo	ogy						
Thermal management	Digital ther	mal sen	sor								
Hyper-Threading	No										
Total threads								e two logical pro	cessors)		
Execute Disable (XD) Bit			lata areas fi								
Intel 64 Technology <sup>1</sup> (EM64T)			/ (an extens			struction	set whi	ch adds			
	64 bit exter										
Virtualization Technology			lization Tech								
Intel Trusted Execution Technology		ables mo	ore secure	olatforn	ns from soft	ware-ba	sed atta	icks with approp	oriate sof	tware	
Intel Dynamic Acceleration	No										
L1 cache	Four 32KB	per core	e, integrated	ł							
L2 cache - size			or <b>12MB</b> / fu nart Cache)		d, 2 x 3MB/	4MB/6M	IB share	ed cache on eac	h die [du	al-die]	
L2 cache - data path		a path (3	32 bytes), 6	4 byte	cache line s	size, 8-w	ay set a	ssociative, integ	grated		
L3 cache	None										
System bus								s bus transfers	at 2 times	s per clock	(
Memory addressability	64GB merr	nory add	lressability (	(but lim	ited by chip	set), 36-	bit addr	essing			
System bus - width	64-bit data	path									
Execution units per core			pating point	units,	1 load unit,	1 store ι	unit				
Math coprocessor	Pipelined fl	01		_							
Compatibility	Compatible	e with IA	-32 softwar	е							
· · ·			Q8xxx/9x	xx <sup>-</sup> 45r	m						
Process technology	Q6xxx: 65	nm;	QUAAA 3A								
	Q6xxx: 65 Q6xxx: 65		Q8xxx/9x	-	watts						
Process technology	Q6xxx: 65	watts;	Q8xxx/9x	xx: 95		C-LGA6	6) packa	ige requires LG	A775 so	cket (soci	ket also
Process technology Thermal Design Power	Q6xxx: 65 Q6xxx: <b>77</b>	watts;	Q8xxx/9x Flip-Chip L	xx: 95		C-LGA	i) packa	ige requires LG	A775 so	<b>cket</b> (socl	ket also
Process technology Thermal Design Power	Q6xxx: 65 Q6xxx: <b>77</b> ca	watts; <b>5-land l</b> lled Soc	Q8xxx/9x Flip-Chip L ket T)	xx: 95 and Gr	id Array (F		<i>,</i> .	ige requires LG package requii		`	
Process technology Thermal Design Power	Q6xxx: 65 Q6xxx: <b>77</b> ca	watts; 5-land l lled Soc x: 775-	Q8xxx/9x Flip-Chip L ket T)	xx: 95 and Gr Chip La	id Array (F		<i>,</i> .			`	
Process technology Thermal Design Power	Q6xxx: 65 Q6xxx: <b>77</b> ca Q8xxx/9xx	watts; 5-land l lled Soc x: 775 also	Q8xxx/9x Flip-Chip L ket T) -land Flip-C	xx: 95 and Gr Chip La ket T)	id Array (F Ind Grid Ai	rray (FC	-LGA8)	package requi		`	

All trademarks are the property of their respective owners © Lenovo (C2Q) Compiled by Roger Dodson, Lenovo. December 2008

### [Desktop] Intel Core i7 Processor

Intel <sup>®</sup> Core™ i7 processor for desktops	Clock speed	Shared L3 cache	Quick Path Interconnect	Core	Virtual- ization Tech	Hyper- Threading Tech	Intel 64 Tech	Intel Turbo Boost	Avail- able date
Intel Core i7-920 Processor Intel Core i7-940 Processor	2.66GHz 2.93GHz	8MB 8MB	4.8GT/s 4.8GT/s	Quad Quad	Yes Yes	Yes Yes	Yes Yes	Yes Yes	Jan 2009 Jan 2009
Processor generation Marketing name Core	Bloomfield (Neh Intel Core i7 pro Quad-core	,							
Micro-architecture Intel Wide Dynamic Execution Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power mgmt technology Hyper-Threading Total threads Execute Disable Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Trusted Execution Technology Intel Dynamic Acceleration Turbo Boost	Intel Core Micro- Each core can co Hides memory la Streaming SIMD Enhanced Intel S Intel Hyper-Threa Eight threads (for Protects memory Intel 64 Technolo Intel Virtualization None Intel Turbo Boost	mplete u tency Extensic Extensic peedSte ading Tec ur cores data are gy (exter Techno	ip to four full ir ns (SSE2, SS ns 4 (SSE4), p™ technology thnology <sup>2</sup> with Hyper-Thi teas from malic tision to IA-32 logy	E3) Super Sh /, power r reading s ious softv instructio	uffle Engine nanagemer upport prov vare execut n set addin	e, SSE4.2 nt capabilities <i>r</i> ide eight thre tion g 64-bit exter	s, multiple lo eads)		ates
L1 cache L2 cache L3 cache	64KB per core, s 256KB per core, 8MB shared amo	unified, 8	8-way set asso	ciative		,	,. ,	set associa	itive
Memory controller Memory support System bus (front side bus) QuickPath Interconnect	Integrated memo DDR3, three cha None Intel QuickPath In	nnels ma	ix, two DIMMs						
Compatibility	Compatible with	A-32 sof	tware						
Process technology Thermal Design Power Package and connector	45nm 130 watts <b>1366-land Flip-C</b>	hip Lan	d Grid Array (	(FC-LGA	8) package	e requires LG	A1366 soc	ket	
Chipset support	Intel X58 Expres	Chinco	familias: atho	r		-			

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

(I7) Compiled by Roger Dodson, Lenovo. December 2008

#### [Desktop] Intel Core i7 Processor Extreme Edition

Intel <sup>®</sup> Core™ i7 processor Extrem for desktops and workstations	e Edition	Clock speed	Shared L3 cache	Quick Path Interconnect	Core	Virtual- ization Tech	Hyper- Threading Tech	Intel 64 Tech	Intel Turbo Boost	Avail- able date
Intel Core i7-965 Processor Extrem	e Edtion	3.2GHz	8MB	6.4GT/s	Quad	Yes	Yes	Yes	Yes	Jan 2009
Processor generation Marketing name Core	Bloomfie Intel Cor Quad-co	e i7 proc	,	Extreme Editi	on					
Micro-architecture Intel Wide Dynamic Execution Intel Smart Memory Access Intel Advanced Digital Media Boost Intel HD Boost Power mgmt technology Hyper-Threading Total threads Execute Disable Bit Intel 64 Technology <sup>1</sup> Virtualization Technology Intel Trusted Execution Technology Intel Dynamic Acceleration Turbo Boost	Hides me Streamin Enhance Intel Hyp Eight thre Protects Intel 64 T Intel Virtu None None	e can co emory lat g SIMD I g SIMD I d Intel Sp er-Threa eads (fou memory echnolog ialization	mplete u ency Extensic Extensic beedSte ding Tec r cores data are gy (exter Techno	up to four full in ons (SSE2, SS ons 4 (SSE4), p™ technology <sup>2</sup> with Hyper-Th eas from malic nsion to IA-32	E3) Super Sh y, power r reading s ious soft instructio	uffle Engin nanageme upport prov vare execu n set addin	e, SSE4.2 nt capabilities vide eight thre tion ig 64-bit exter	s, multiple lo eads)		ates
L1 cache L2 cache L3 cache	256KB p	er core, i	unified, 8	een data cach 3-way set asso res (Intel Sma	ciative				v set associa	ative
Memory controller Memory support System bus (front side bus) QuickPath Interconnect	Integrated memory controller DDR3, three channels max, two DIMMs per channel max, 24GB max, 800/1066MHz None Intel QuickPath Interconnect, point-to-point link between processor and chipset, 6.4GT/sec max									
Compatibility	Compatik	ble with L	A-32 sof	tware						
Process technology Thermal Design Power Package and connector	45nm 130 watts <b>1366-lan</b>		hip Lan	d Grid Array	(FC-LGA	8) package	e requires LG	A1366 soc	ket	
Chipset support	Intel X58	Express	Chipse	t families; othe	er compat	ible chipse	ts			
All trademarks are the property of the	in na an a atiu	o ourooro				(175)	Compiled by F	Pogor Dodoo	n Lonovo D	acombor 200

All trademarks are the property of their respective owners  $\ensuremath{\textcircled{}}$  Lenovo

(I7E) Compiled by Roger Dodson, Lenovo. December 2008

This publication could include technical inaccuracies or typographical errors. References herein to Lenovo products and services do not imply that Lenovo intends to make them available in other countries. LENOVO PROVIDES THIS PUBLICATION AS IS WITHOUT WAR-RANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABIL-ITY OR FITNESS FOR A PARTICULAR PURPOSE. Some jurisdictions do not allow disclaimer of express of implied warranties; therefore this disclaimer may not apply to you.

- Intel 64 Technology (formerly EM64T): Intel 64 Technology (formerly Intel EM64T) requires a computer system with a processor, chipset, BIOS, operating system, device drivers, and applications enabled for Intel 64 Technology. Processor will not operate (including 32-bit operation) without an Intel 64 Technology-enabled BIOS. Performance will vary depending on your hardware and software configurations.
- <sup>2</sup> Intel Hyper-Threading Technology (HT Technology): Intel Hyper-Threading Technology requires a computer system with a processor supporting HT Technology and an HT Technology-enabled chipset, BIOS, and operating system. Performance will vary depending on the specific hardware and software you use. For more information, including details on which processors support HT Technology, see www.intel.com/info/hyperthreading.
- <sup>3</sup> Intel Turbo Boost Technology: Intel Turbo Boost Technology requires a PC with a processor with Intel Turbo Boost Technology capability. Intel Turbo Boost Technology performance varies depending on hardware, software, and overall system configuration. Check with your PC manufacturer on whether your system delivers Intel Turbo Boost Technology. See www.intel.com/info/technology/turboboost for more information.

**Trademarks:** Lenovo, the Lenovo logo, New World. New Thinking., Access Connections, Rescue and Recovery, Think-Centre, ThinkPad, ThinkStation, ThinkVantage, and ThinkVision are trademarks of Lenovo.

Intel logo, Intel Inside logo, Intel Core and Core Inside, Pentium, Celeron and Intel SpeedStep are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

Other company, product and service names may be trademarks or service marks of others.

## ThinkPad<sub>®</sub> ThinkCentre<sub>®</sub>

Visit **www.lenovo.com/safecomputing** periodically for the latest information on safe and effective computing.

#### Visit **www.lenovo.com/psref** for the latest version of Personal Systems Reference.

© Lenovo, 2009. All rights reserved.

Lenovo 1009 Think Place Morrisville, NC 27560 U.S.A.

January 2009 tecbook.pdf