Personal Systems Reference
Intel® PC Processors

January 2009 - Version 350

[Notebook] Intel Celeron M Processor 5xx

Intel® Celeron® M processor for mobile systems	Clock Perf Mode	Clock Battery Mode	L2 cache	System bus MHz	Core	Hyper-Threading Technology	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Avail-able date
Ultra Low Voltage											
Intel Celeron M Processor 523	933MHz	N/A	1MB	533MHz	Single	No	No	Yes	No	Yes	Sep 2007
Standard Voltage											
Intel Celeron M Processor 520	1.6GHz	N/A	1MB	533MHz	Single	No	No	Yes	No	Yes	Jan 2007
Intel Celeron M Processor 530	1.73GHz	N/A	1MB	533MHz	Single	No	No	Yes	No	Yes	Apr 2007

Processor generation	**Merom**
Marketing name	**Intel Celeron M Processor**
Core	**Single-core**
Branding	Not part of the Intel Centrino® Processor Technology or Intel Centrino with vPro Processor Technology
Micro-architecture	Intel Core™ Micro-architecture
MMX™ / Streaming SIMD	MMX™ (57 new instructions), Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	None
Total threads	One thread (one cores with no Hyper-Threading support provides one logical processor)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	None
Virtualization Technology	None
L1 cache	256-bit data path, full speed
L1 data cache	32KB data cache, integrated
L1 instruction cache	32KB instruction cache, integrated
L2 cache - size	**1MB**, full speed
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None
System bus	**533MHz** (transfers data 4 times per clock), address bus transfers at 2 times per clock
System bus - width	64-bit data path
Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	65nm or 0.065u
Thermal Design Power	*Ultra Low Voltage:* 5 watts; *Standard Voltage:* 30 watts
Package and connector	*All:* **Socket M**
	520/530: Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket)
	523: Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	**Mobile Intel 945 Express Chipset family**; other compatible chipsets

[Notebook] Intel Celeron Processor 5xx, 7xx

Intel® Celeron® mobile processor	Clock Perf Mode	Clock Battery Mode	L2 cache	System bus MHz	Core	Thermal Design Power	Hyper-Threading Technology	Virtual-ization Tech	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Avail-able date
Intel Celeron Processor 530	1.73GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Sep 2007
Intel Celeron Processor 540	1.86GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Jun 2007
Intel Celeron Processor 550	2.00GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Jun 2007
Intel Celeron Processor 560	2.13GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Jan 2008
Intel Celeron Processor 570	2.26GHz	N/A	1MB	533MHz	Single	31W	No	No	No	Yes	Apr 2008
Intel Celeron Processor 575	2.00GHz	N/A	1MB	667MHz	Single	31W	No	No	No	Yes	Aug 2008
Intel Celeron Processor 585	2.16GHz	N/A	1MB	667MHz	Single	31W	No	No	No	Yes	Aug 2008
Intel Celeron Processor 723	1.20GHz	N/A	1MB	800MHz	Single	10W	No	No	No	Yes	Aug 2008

Processor generation	*5xx:* **Merom**; *7xx:* **Penryn**
Marketing name	**Intel Celeron mobile processor**
Core	**Single-core**
Branding	Not part of the Intel Centrino® Processor Technology or Intel Centrino with vPro Processor Technology
Micro-architecture	Intel Core™ Micro-architecture
MMX™ / Streaming SIMD	MMX™ (57 new instructions), Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	None
Total threads	One thread (one cores with no Hyper-Threading support provides one logical processor)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	None
Virtualization Technology	None

L1 cache	256-bit data path, full speed
L1 data cache	32KB data cache, integrated
L1 instruction cache	32KB instruction cache, integrated

L2 cache - size	**1MB,** full speed
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None

System bus	**533MHz**, **667MHz**, or **800MHz** (transfers data 4 times per clock), address bus transfers at 2 times per clock
System bus - width	64-bit data path

Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	65nm or 0.065u
Thermal Design Power	*5xx:* 27-31 watts @ 0.95-1.3 volts
	7xx: 10 watts (Ultra Low Voltage)
Package and connector	*5xx:* **Socket P** / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket)
	7xx: **Socket P** / Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	*5xx:* **Mobile Intel 965 Express Chipset family**; other compatible chipsets
	7xx: **Mobile Intel 4 Series Express Chipset family**; other compatible chipsets

[Notebook] Intel Celeron Processor

Intel® Celeron® mobile processor	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	HD Boost	Virtual- ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Trusted Execution Tech	Avail- able date
Intel Celeron processor T1600	1.66GHz	1MB	667MHz	Dual	No	No	Yes	Yes	Yes	No	Oct 2008
Intel Celeron processor T1700	1.86GHz	1MB	667MHz	Dual	No	No	Yes	Yes	Yes	No	Oct 2008

Processor generation	**Montevina**
Marketing name	**Intel Celeron mobile processor**
Core	**Dual-core**
Branding	Value or essential mobile processor

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Power mgmt technology	Enhanced Intel SpeedStep™ technology (EIST)
Hyper-Threading	No
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Intel Virtualization Technology	No
Intel Trusted Execution Technology	No

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache / integrated
L1 instruction cache	2x32KB instruction cache / integrated

L2 cache - size	**1MB** / full speed / shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)

System bus	**667MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path

Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	65nm or 0.065u
Thermal Design Power	35 watts
Package and connector	**Socket P** / Micro Flip-Chip Ball Grid Array (Micro-FCBGA)
Chipset support	**Mobile Intel 4 Series Chipset family**; other compatible chipsets

Intel® Pentium® Processor	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Hyper-Threading Technology	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Trusted Execution Tech	Intel Dynamic Acceleration	Avail-able date
Intel Pentium Processor T2060	1.60GHz	1MB	533MHz	Dual	No	No	Yes	Yes	No	No	No	Jan 2007
Intel Pentium Processor T2080	1.70GHz	1MB	533MHz	Dual	No	No	Yes	Yes	No	No	No	Jan 2007
Intel Pentium Processor T2130	1.86GHz	1MB	533MHz	Dual	No	No	Yes	Yes	No	No	No	Oct 2007
Intel Pentium Processor T2310	1.46GHz	1MB	533MHz	Dual	No	No	Yes	Yes	Yes	No	No	July 2007
Intel Pentium Processor T2330	1.60GHz	1MB	533MHz	Dual	No	No	Yes	Yes	Yes	No	No	July 2007
Intel Pentium Processor T2370	1.73GHz	1MB	533MHz	Dual	No	No	Yes	Yes	Yes	No	No	Jan 2008
Intel Pentium Processor T2390	1.86GHz	1MB	533MHz	Dual	No	No	Yes	Yes	Yes	No	No	Jan 2008
Intel Pentium Processor T3200	2.00GHz	1MB	667MHz	Dual	No	No	Yes	Yes	Yes	No	No	Nov 2008
Intel Pentium Processor T3400	2.16GHz	1MB	667MHz	Dual	No	No	Yes	Yes	Yes	No	No	Nov 2008

Processor generation	*T2060/T2080/T2130:* **Yonah**; *T2310/T2330/T2370/T2390/T3200/T3400:* **Merom**
Marketing name	**Intel Pentium Processor**
Core	**Dual-core**
Branding	Value or essential mobile processor

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline;
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Power mgmt technology	Enhanced Intel SpeedStep™ technology
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	*Some:* Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Intel Virtualization Technology	No
Intel Trusted Execution Technology	No
Intel Dynamic Accerlation	No

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache / integrated
L1 instruction cache	2x32KB instruction cache / integrated

L2 cache - size	**1MB** / full speed, shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None

System bus	**533MHz** or **667MHz** (transfers data 4 times per clock), address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path

Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	65nm or 0.065u
Package and connector	*T2060/T2080/T2130:* Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
	T2310/T2330/T2370/T2390/T3200/T3400: **Socket P** / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)

(P2) Compiled by Roger Dodson, Lenovo. January 2009

Intel® Core™ 2 Solo processor for mobile systems	Clock Perf Mode	L2 cache	System bus MHz	Core	Hyper-Threading Technology	Virtual-ization Tech	Intel 64 Tech (EM64T)	Intel HD Boost	Intel Dynamic Acceleration	Trusted Execution Tech (TXT)	Avail-able date
Ultra Low Voltage											
Intel Core 2 Solo processor U2100	1.06GHz	1MB	533MHz	Single	No	Yes	Yes	No	No	No	Sep 2007
Intel Core 2 Solo processor U2200	1.20GHz	1MB	533MHz	Single	No	Yes	Yes	No	No	No	Sep 2007
Intel Core 2 Solo processor SU3300	1.20GHz	3MB	800MHz	Single	No	Yes	Yes	Yes	No	Yes	Aug 2008
Intel Core 2 Solo processor SU3500	1.30GHz	3MB	800MHz	Single	No	Yes	Yes	Yes	No	Yes	Aug 2008

Processor generation	*Uxxxx:* **Merom (Napa Refresh)**; *SUxxxx:* **Penryn (Montevina)**
Marketing name	**Intel Core 2 Solo mobile processor**
Core	**Single-core**
Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	*Some:* Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power management technology	Enhanced Intel SpeedStep® technology
Intel Dynamic Power Coordination	Coordinates Enhanced Intel SpeedStep Technology and idle power-management state transitions independently per core to help save power
Intel Dynamic Bus Parking	Enables platform power savings and improved battery life by allowing the chipset to power down with the processor in low-frequency mode
Enhanced Intel Deeper Sleep with Dynamic Cache Sizing	Saves power by flushing cache data to system memory during periods of inactivity to lower CPU voltage
Thermal management	Digital thermal sensor
Hyper-Threading	No
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64-bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology
Intel Dynamic Acceleration	None
Intel Trusted Execution Tech (TXT)	*Some:* Provides a more secure platform from software-based attacks with TXT-enabled OS or appl

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated

L2 cache - size	**1MB** or **3MB** / full speed
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None

System bus	**533MHz** or **800MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path

Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	*Uxxxx:* 65nm; *SUxxxx:* 45nm
Thermal Design Power	5.5 watts
Package and connector	*Uxxxx:* **Socket M** / Micro Flip-Chip Ball Grid Array (Micro-FCBGA) *SUxxxx:* **Socket P** / Micro Flip-Chip Ball Grid Array (Micro-FCBGA)
Chipset support	*Uxxxx:* **Mobile Intel 945GM and 945GMS Express Chipset**; other compatible chipsets *SUxxxx:* **Mobile Intel 4 Series Express Chipset**; other compatible chipsets

Intel® Core™ 2 Duo processor for mobile systems	Clock Perf Mode	Clock Battery Mode	Shared L2 cache	System bus MHz	Core	Hyper-Threading Technology	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Intel Dynamic Acceleration	Avail-able date
Intel Core 2 Duo processor U7500	1.06GHz	800MHz	2MB	533MHz	Dual	No	Yes	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor U7600	1.20GHz	800MHz	2MB	533MHz	Dual	No	Yes	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor U7700	1.33GHz	800MHz	2MB	533MHz	Dual	No	Yes	Yes	Yes	Yes	No	Jun 2007
Intel Core 2 Duo processor L7200	1.33GHz	1.0GHz	**4MB**	667MHz	Dual	No	Yes	Yes	Yes	Yes	No	Jan 2007
Intel Core 2 Duo processor L7400	1.50GHz	1.0GHz	**4MB**	667MHz	Dual	No	Yes	Yes	Yes	Yes	No	Jan 2007
Intel Core 2 Duo processor T5200	1.60GHz	1.0GHz	2MB	533MHz	Dual	No	No	Yes	Yes	Yes	No	Jan 2007
Intel Core 2 Duo processor T5300	1.73GHz	1.0GHz	2MB	533MHz	Dual	No	No	Yes	Yes	Yes	No	Oct 2007
Intel Core 2 Duo processor T5500	1.66GHz	1.0GHz	2MB	667MHz	Dual	No	No	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor T5600	1.83GHz	1.0GHz	2MB	667MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor T7200	2.00GHz	1.0GHz	**4MB**	667MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor T7400	2.16GHz	1.0GHz	**4MB**	667MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor T7600	2.33GHz	1.0GHz	**4MB**	667MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006

U (Ultra Low Voltage)=<14 watts; L (Low Voltage)=15-24 watts; T (Standard Voltage)=25-49 watts; E=>50 watts

Processor generation	**Merom**
Marketing name	**Intel Core 2 Duo mobile processor**
Core	**Dual-core**
Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Power management technology	Enhanced Intel SpeedStep® technology
Intel Dynamic Power Coordination	Coordinates Enhanced Intel SpeedStep Technology and idle power-management state transitions independently per core to help save power
Intel Dynamic Bus Parking	Enables platform power savings and improved battery life by allowing the chipset to power down with the processor in low-frequency mode
Enhanced Intel Deeper Sleep with Dynamic Cache Sizing	Saves power by flushing cache data to system memory during periods of inactivity to lower CPU voltage
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64-bit extensions to the x86 architecture)
Virtualization Technology	*Some:* Intel Virtualization Technology
Intel Dynamic Accerlation	*Some:* Intel Dynamic Acceleration (IDA) allows one core to deliver extra performance when other core is idle
L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache / integrated
L1 instruction cache	2x32KB instruction cache / integrated
L2 cache - size	**2MB** or **4MB** / full speed / shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None
System bus	**533MHz**, **667MHz**, or **800MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path
Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	65nm or 0.065u
Thermal Design Power	*U7xxx:* 10 watts; *L7xxx:* 17 watts; *Txxxx:* 34 watts
Package and connector	**Socket M** / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	**Mobile Intel 945 Express Chipset family**; other compatible chipsets

(C2DT) Compiled by Roger Dodson, Lenovo. September 2008

[Notebook] Intel Core 2 Duo Processor (Socket P)

Intel® Core™ 2 Duo processor for mobile systems	Clock Perf Mode	Clock Battery Mode	Shared L2 cache	System bus MHz	Core	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Intel Dynamic Acceleration	Avail-able date
Intel Core 2 Duo processor U7500	1.06GHz	800MHz	2MB	533MHz	Dual	Yes	Yes	Yes	Yes	Yes	Jun 2007
Intel Core 2 Duo processor U7600	1.20GHz	800MHz	2MB	533MHz	Dual	Yes	Yes	Yes	Yes	Yes	Jun 2007
Intel Core 2 Duo processor U7700	1.33GHz	800MHz	2MB	533MHz	Dual	Yes	Yes	Yes	Yes	Yes	Jan 2008
Intel Core 2 Duo processor SL7100	1.2GHz	800MHz	**4MB**	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	Feb 2008
Intel Core 2 Duo processor L7300	1.4GHz	800MHz	**4MB**	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	May 2007
Intel Core 2 Duo processor L7500	1.6GHz	800MHz	**4MB**	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	May 2007
Intel Core 2 Duo processor L7700	1.8GHz	800MHz	**4MB**	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	Sep 2007
Intel Core 2 Duo processor T5250	1.50GHz	667MHz	2MB	667MHz	Dual	No	Yes	Yes	Yes	No	July 2007
Intel Core 2 Duo processor T5270	1.40GHz	1.0GHz	2MB	800MHz	Dual	No	Yes	Yes	Yes	Yes	Aug 2007
Intel Core 2 Duo processor T5450	1.66GHz	667MHz	2MB	667MHz	Dual	No	Yes	Yes	Yes	No	July 2007
Intel Core 2 Duo processor T5470	1.60GHz	1.0GHz	2MB	800MHz	Dual	No	Yes	Yes	Yes	Yes	Aug 2007
Intel Core 2 Duo processor T5550	1.83GHz	667MHz	2MB	667MHz	Dual	No	Yes	Yes	Yes	No	July 2007
Intel Core 2 Duo processor T5670	1.80GHz	800MHz	2MB	800MHz	Dual	No	Yes	Yes	Yes	Yes	July 2008
Intel Core 2 Duo processor T5750	2.00GHz	667MHz	2MB	667MHz	Dual	No	Yes	Yes	Yes	No	Feb 2008
Intel Core 2 Duo processor T5850	2.16GHz	667MHz	2MB	667MHz	Dual	No	Yes	Yes	Yes	No	Feb 2008
Intel Core 2 Duo processor T5870	2.00GHz	800MHz	2MB	800MHz	Dual	No	Yes	Yes	Yes	Yes	Oct 2008
Intel Core 2 Duo processor T7100	1.8GHz	800MHz	2MB	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	May 2007
Intel Core 2 Duo processor T7250	2.0GHz	800MHz	2MB	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	Sep 2007
Intel Core 2 Duo processor T7300	2.0GHz	800MHz	**4MB**	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	May 2007
Intel Core 2 Duo processor T7500	2.2GHz	800MHz	**4MB**	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	May 2007
Intel Core 2 Duo processor T7700	2.4GHz	800MHz	**4MB**	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	May 2007
Intel Core 2 Duo processor T7800	2.6GHz	800MHz	**4MB**	800MHz	Dual	Yes	Yes	Yes	Yes	Yes	Sep 2007

U (Ultra Low Voltage)=<14 watts; L (Low Voltage)=15-24 watts; T (Standard Voltage)=25-49 watts; E=>50 watts

Processor generation	**Merom**
Marketing name	**Intel Core 2 Duo mobile processor**
Core	**Dual-core**
Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Power management technology	Enhanced Intel SpeedStep® technology
Intel Dynamic Power Coordination	Coordinates Enhanced Intel SpeedStep Technology and idle power-management state transitions independently per core to help save power
Intel Dynamic Bus Parking	Enables platform power savings and improved battery life by allowing the chipset to power down with the processor in low-frequency mode
Enhanced Intel Deeper Sleep with Dynamic Cache Sizing	Saves power by flushing cache data to system memory during periods of inactivity to lower CPU voltage
Dynamic Front Side Bus Frequency Switching	*Some (not T5xxx):* Changes the bus clock frequency allowing a reduction in core voltage enabling a lower power active state called super LFM
Thermal management	Digital thermal sensor
Hyper-Threading	No
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64-bit extensions to the x86 architecture)
Virtualization Technology	*Some:* Intel Virtualization Technology (VT)
Intel Dynamic Accerlation	*Some:* Intel Dynamic Acceleration (IDA) allows one core to deliver extra performance when other core is idle
L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache, integrated
L1 instruction cache	2x32KB instruction cache, integrated
L2 cache - size	**2MB** or **4MB,** full speed, shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
System bus (front side bus)	**533MHz**, **667MHz**, or **800MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset), 36-bit addressing
System bus - width	64-bit data path
Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Process technology	65nm or 0.065u
Thermal Design Power	*U7xxx:* 10 watts; *L7xxx:* 17 watts; *Txxxx:* 35 watts
Package and connector	**Socket P** / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	**Mobile Intel 965 Express Chipset family**; other compatible chipsets

Intel® Core™ 2 Duo processor for notebook systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Thermal Design Power	Virtual- ization Tech	Intel 64 Tech	Intel Dynamic Acceleration	Trusted Execution Tech (TXT)	Avail- able date
Intel Core 2 Duo processor T6400	2.0GHz	2MB	800MHz	Dual	35W	Yes	Yes	Yes	No	Jan 2009
Intel Core 2 Duo processor T6600	2.2GHz	2MB	800MHz	Dual	35W	Yes	Yes	Yes	No	Jan 2009
Intel Core 2 Duo processor T8100	2.1GHz	3MB	800MHz	Dual	35W	Yes	Yes	Yes	No	Jan 2008
Intel Core 2 Duo processor T8300	2.4GHz	3MB	800MHz	Dual	35W	Yes	Yes	Yes	No	Jan 2008
Intel Core 2 Duo processor T9300	2.5GHz	**6MB**	800MHz	Dual	35W	Yes	Yes	Yes	No	Jan 2008
Intel Core 2 Duo processor T9500	2.6GHz	**6MB**	800MHz	Dual	35W	Yes	Yes	Yes	No	Jan 2008
Intel Core 2 Duo processor P7370	2.00GHz	3MB	1066MHz	Dual	**25W**	Yes	Yes	Yes	Yes	Sep 2008
Intel Core 2 Duo processor P7450	2.13GHz	3MB	1066MHz	Dual	**25W**	Yes	Yes	Yes	Yes	Jan 2009
Intel Core 2 Duo processor P8400	2.26GHz	3MB	1066MHz	Dual	**25W**	Yes	Yes	Yes	Yes	July 2008
Intel Core 2 Duo processor P8600	2.4GHz	3MB	1066MHz	Dual	**25W**	Yes	Yes	Yes	Yes	July 2008
Intel Core 2 Duo processor P8700	2.53GHz	3MB	1066MHz	Dual	**25W**	Yes	Yes	Yes	Yes	Dec 2008
Intel Core 2 Duo processor P9500	2.53GHz	**6MB**	1066MHz	Dual	**25W**	Yes	Yes	Yes	Yes	July 2008
Intel Core 2 Duo processor P9600	2.66GHz	**6MB**	1066MHz	Dual	**25W**	Yes	Yes	Yes	Yes	Dec 2008
Intel Core 2 Duo processor T9400	2.53GHz	**6MB**	1066MHz	Dual	35W	Yes	Yes	Yes	Yes	July 2008
Intel Core 2 Duo processor T9550	2.66GHz	**6MB**	1066MHz	Dual	35W	Yes	Yes	Yes	Yes	Dec 2008
Intel Core 2 Duo processor T9600	2.8GHz	**6MB**	1066MHz	Dual	35W	Yes	Yes	Yes	Yes	July 2008
Intel Core 2 Duo processor T9800	2.93GHz	**6MB**	1066MHz	Dual	35W	Yes	Yes	Yes	Yes	Dec 2008

U (Ultra Low Voltage)=<12 watts; L (Low Voltage)=12-19 watts; P =20-29 watts; T (Standard Voltage)=30-39 watts; X or QX=>40 watts

Processor generation	*T8100/T8300/T9300/T9500:* **Penryn (Santa Rosa Refresh);** *Others:* **Penryn (Montevina)**
Marketing name	**Intel Core 2 Duo mobile processor**
Core	**Dual-core**
Branding	Supports **Intel Centrino® 2 Processor Technology** or **Intel Centrino 2 with vPro Processor Technology** when hardware and software requirements met
Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power management technology	Enhanced Intel SpeedStep® technology
Intel Dynamic Power Coordination	Coordinates Enhanced Intel SpeedStep™ Technology and idle power-management state transitions independently per core to help save power
Intel Deep Power Down Technology	Low-power state that allows both cores and L2 cache to be powered down when processor idle
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64-bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology (VT)
Intel Dynamic Acceleration	Intel Dynamic Acceleration (IDA) allows one core to deliver extra performance when other core is idle
Intel Trusted Execution Tech (TXT)	Provides a more secure platform with protection from software-based attacks with TXT-enabled OS or appl
L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache, integrated
L1 instruction cache	2x32KB instruction cache, integrated
L2 cache - size	**2MB, 3MB,** or **6MB**, full speed, shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
System bus (front side bus)	**800MHz** or **1066MHz** (transfers data 4 times per clock), address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset), 36-bit addressing
System bus - width	64-bit data path
Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	45nm
Thermal Design Power	*Pxxxx:* 25 watts; *Txxxx:* 35 watts
Package and connector	**Socket P** / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	**Mobile Intel 965 Express Chipset family**; **Mobile Intel 4 Series Chipset family**; other compatible chipsets

[Notebook] Intel Core 2 Duo Processor (SFF)

Intel® Core™ 2 Duo processor *Small Form Factor (SFF)* *for notebook systems*	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Thermal Design Power	Intel HD Boost	Intel 64 Tech	Intel Dynamic Acceleration	Trusted Execution Tech (TXT)	Avail- able date
Intel Core 2 Duo processor SU9300	1.20GHz	3MB	800MHz	Dual	**10W**	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SU9400	1.40GHz	3MB	800MHz	Dual	**10W**	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SL9300	1.60GHz	**6MB**	1066MHz	Dual	**17W**	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SL9400	1.86GHz	**6MB**	1066MHz	Dual	**17W**	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SP9300	2.26GHz	**6MB**	1066MHz	Dual	**25W**	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Duo processor SP9400	2.40GHz	**6MB**	1066MHz	Dual	**25W**	Yes	Yes	Yes	Yes	Aug 2008

- **Small Form Factor (SFF) notebook processors**
  - **SUxxxx = Ultra Low Voltage**
  - **SLxxxx = Low Voltage**
  - **SPxxxx = Power Optimized Performance**

Processor generation	**Penryn (Montevina)**
Marketing name	**Intel Core 2 Duo mobile processor**
Core	**Dual-core**
Branding	Supports **Intel Centrino® 2 Processor Technology** or **Intel Centrino 2 with vPro Processor Technology** when hardware and software requirements met
Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power management technology	Enhanced Intel SpeedStep® technology
Intel Dynamic Power Coordination	Coordinates Enhanced Intel SpeedStep™ Technology and idle power-management state transitions independently per core to help save power
Intel Dynamic Bus Parking	Enables platform power savings and improved battery life by allowing the chipset to power down with the processor in low-frequency mode
Enhanced Intel Deeper Sleep with Dynamic Cache Sizing	Saves power by flushing cache data to system memory during periods of inactivity to lower CPU voltage
Intel Deep Power Down Technology	Low-power state that allows both cores and L2 cache to be powered down when processor idle
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64-bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology (VT)
Intel Dynamic Acceleration	Intel Dynamic Acceleration (IDA) allows one core to deliver extra performance when other core is idle
Intel Trusted Execution Tech (TXT)	Provides a more secure platform with protection from software-based attacks with TXT-enabled OS or appl

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache, integrated
L1 instruction cache	2x32KB instruction cache, integrated

L2 cache - size	**3MB** or **6MB**, full speed, shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None

System bus (front side bus)	**800MHz** or **1066MHz** (transfers data 4 times per clock), address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset), 36-bit addressing
System bus - width	64-bit data path

Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	45nm
Thermal Design Power	*SUxxxx:* 10 watts; *SLxxxx:* 17 watts; *SUxxxx:* 25 watts
Package and connector	**Socket P** / Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	**Mobile Intel 4 Series Chipset family**; other compatible chipsets

[Notebook] Intel Core 2 Quad Processor

Intel® Core™ 2 Quad processor for notebook systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Thermal Design Power	Virtual-ization Tech	Intel 64 Tech	Intel Dynamic Acceleration	Trusted Execution Tech (TXT)	Avail-able date
Intel Core 2 Quad processor Q9000	2.00GHz	6MB	1066MHz	Quad	45W	Yes	Yes	Yes	No	Dec 2008
Intel Core 2 Quad processor Q9100	2.26GHz	12MB	1066MHz	Quad	45W	Yes	Yes	Yes	No	Aug 2008

Processor generation	**Penryn** (Montevina)
Marketing name	**Intel Core 2 Quad mobile processor**
Core	**Quad-core**
Branding	Supports **Intel Centrino® 2 Processor Technology** or **Intel Centrino 2 with vPro Processor Technology** when hardware and software requirements met
Micro-architecture	Intel Core micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power management technology	Enhanced Intel SpeedStep® technology
Intel Dynamic Power Coordination	Coordinates Enhanced Intel SpeedStep™ Technology and idle power-management state transitions independently per core to help save power
Intel Dynamic Bus Parking	Enables platform power savings and improved battery life by allowing the chipset to power down with the processor in low-frequency mode
Enhanced Intel Deeper Sleep with Dynamic Cache Sizing	Saves power by flushing cache data to system memory during periods of inactivity to lower CPU voltage
Intel Deep Power Down Technology	Low-power state that allows both cores and L2 cache to be powered down when processor idle
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64-bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology (VT)
Intel Dynamic Accerelation	Intel Dynamic Acceleration (IDA) allows one core to deliver extra performance when other core is idle
Intel Trusted Execution Tech (TXT)	Provides a more secure platform with protection from software-based attacks with TXT-enabled OS or appl
L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache, integrated
L1 instruction cache	2x32KB instruction cache, integrated
L2 cache - size	**6MB** or **12MB**, full speed, shared between cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None
System bus (front side bus)	**1066MHz** (transfers data 4 times per clock), address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset), 36-bit addressing
System bus - width	64-bit data path
Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	45nm
Thermal Design Power	45 watts
Package and connector	**Socket P** / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	**Mobile Intel 4 Series Chipset family**; other compatible chipsets

Intel® Core™ 2 Extreme processor for notebook systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	HD Boost	Virtual- ization Tech	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Intel Dynamic Acceleration	Trusted Execution Tech (TXT)	Avail- able date
Intel Core 2 Extreme processor X7800	2.60GHz	4MB	800MHz	Dual	No	Yes	Yes	Yes	No	No	July 2007
Intel Core 2 Extreme processor X7900	2.80GHz	4MB	800MHz	Dual	No	Yes	Yes	Yes	No	No	Aug 2007
Intel Core 2 Extreme processor X9000	2.80GHz	6MB	800MHz	Dual	Yes	Yes	Yes	Yes	No	**Yes**	Jan 2008
Intel Core 2 Extreme processor X9100	3.06GHz	6MB	1066MHz	Dual	Yes	Yes	Yes	Yes	No	**Yes**	July 2008
Intel Core 2 Extreme processor QX9300	2.53GHz	12MB	1066MHz	**Quad**	Yes	Yes	Yes	Yes	**Yes**	No	Aug 2008

Processor generation	*X7800/X7900:* **Merom (Santa Rosa)**; *X9000/X9100:* **Penryn (Santa Rosa Refresh)**; *QX9300:* **Penryn**
Marketing name	**Intel Core 2 Extreme processor**
Core(s)	**Dual-core** or **quad-core**
Branding	Intel's highest performance brand for processors

Micro-architecture	Intel Core micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	*X9000/X9100/QX9300:* Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power mgmt technology	Enhanced Intel SpeedStep™ technology
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology
Intel Dynamic Accerlation	*Some:* Intel Dynamic Acceleration (IDA) allows one core to deliver extra performance when other core is idle
Intel Trusted Execution Tech (TXT)	*Some:* Provides a more secure platform from software-based attacks with TXT-enabled OS or appl

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache, integrated
L1 instruction cache	2x32KB instruction cache, integrated

L2 cache - size	**4MB**, **6MB,** or **12MB**, full speed, shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None

System bus	**800MHz** or **1066MHz** (transfers data 4 times per clock), address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset), 36-bit addressing
System bus - width	64-bit data path

Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	*X7800/X7900:* 65nm; *X9000/X9100/QS9300:* 45nm
Thermal Design Power	44 or 45 watts
Package and connector	**Socket P** / Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	**Mobile Intel 965 Express Chipset family**; other compatible chipsets

Intel® Celeron® Processor	Clock Perf Mode	L2 cache	System bus MHz	Core	Hyper-Threading Technology	Total threads (logical)	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Trusted Execution Tech	Avail-able date
Intel Celeron Processor 420	1.60GHz	512KB	800MHz	Single	No	1	No	Yes	No	Yes	No	Jun 2007
Intel Celeron Processor 430	1.80GHz	512KB	800MHz	Single	No	1	No	Yes	No	Yes	No	Jun 2007
Intel Celeron Processor 440	2.00GHz	512KB	800MHz	Single	No	1	No	Yes	No	Yes	No	Jun 2007
Intel Celeron Processor 450	2.20GHz	512KB	800MHz	Single	No	1	No	Yes	No	Yes	No	Aug 2008

Processor generation	**Conroe-L**
Marketing name	**Intel Celeron Processor**
Core	**Single-core**
Branding	Value or essential desktop processor

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline;
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Power mgmt technology	No Enhanced Intel SpeedStep™ technology
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	One thread
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Intel Virtualization Technology	No
Intel Trusted Execution Technology	No

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache / integrated
L1 instruction cache	2x32KB instruction cache / integrated

L2 cache - size	**512KB** / full speed
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None

System bus	**800MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path

Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	65nm or 0.065u
Thermal Design Power	65 watts
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA6) package** requires **LGA775 socket** (socket also called Socket T)
Chipset support	**Intel 3 Series Express Chipset family;** Intel 945 and 965 Express Chipset family; other compatible chipsets

Intel® Celeron® Processor	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	HD Boost	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Trusted Execution Tech	Avail-able date
Intel Celeron Processor E1200	1.60GHz	512KB	800MHz	Dual	No	No	Yes	Yes	Yes	No	Jan 2008
Intel Celeron Processor E1400	2.00GHz	512KB	800MHz	Dual	No	No	Yes	Yes	Yes	No	Apr 2008
Intel Celeron Processor E1500	2.20GHz	512KB	800MHz	Dual	No	No	Yes	Yes	Yes	No	Dec 2008

Processor generation	**Conroe**
Marketing name	**Intel Celeron Processor**
Core	**Dual-core**
Branding	Value or essential desktop processor

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline;
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Power mgmt technology	Enhanced Intel SpeedStep™ technology (EIST)
Hyper-Threading	No
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Intel Virtualization Technology	No
Intel Trusted Execution Technology	No

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache / integrated
L1 instruction cache	2x32KB instruction cache / integrated

L2 cache - size	**512KB** / full speed / shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)

System bus	**800MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path

Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	65nm or 0.065u
Thermal Design Power	65 watts
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA6) package** requires **LGA775 socket** (socket also called Socket T)
Chipset support	**Intel G31 Express Chipset families;** other compatible chipsets

(DCEL) Compiled by Roger Dodson, Lenovo. January 2009

Intel® Pentium® Processor	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Hyper-Threading Technology	Total threads (logical)	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Trusted Execution Tech	Avail-able date
Intel Pentium Processor E2140	1.60GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Jun 2007
Intel Pentium Processor E2160	1.80GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Jun 2007
Intel Pentium Processor E2180	2.00GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Aug 2007
Intel Pentium Processor E2200	2.20GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Dec 2007
Intel Pentium Processor E2220	2.40GHz	1MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Mar 2008
Intel Pentium Processor E5200	2.50GHz	2MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Aug 2008
Intel Pentium Processor E5300	2.60GHz	2MB	800MHz	Dual	No	2	No	Yes	Yes	Yes	No	Dec 2008

Processor generation	*E2xxx:* **Conroe**; *E5xxx:* **Wolfdale**
Marketing name	**Intel Pentium Processor**
Core	**Dual-core**
Branding	Value or essential desktop processor

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline;
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Power mgmt technology	Enhanced Intel SpeedStep™ technology
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Intel Virtualization Technology	No
Intel Trusted Execution Technology	No

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache / integrated
L1 instruction cache	2x32KB instruction cache / integrated

L2 cache - size	**1MB** or **2MB** / full speed / shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None

System bus	**800MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path

Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	*E2xxx:* 65nm; *E5xxx:* 45nm
Thermal Design Power	65 watts
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA6) package** requires **LGA775 socket** (socket also called Socket T)
Chipset support	Intel G31 Express Chipset; Intel 4 Series Express Chipset family; other compatible chipsets

(E2) Compiled by Roger Dodson, Lenovo. January 2009

[Desktop] Intel Core 2 Duo Processor

Intel® Core™ 2 Duo processor for desktop systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Hyper-Threading Technology	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Trusted Execution Tech	Avail-able date
Intel Core 2 Duo processor E4300	1.80GHz	2MB	800MHz	Dual	No	**No**	Yes	Yes	Yes	No	Jan 2007
Intel Core 2 Duo processor E4400	2.00GHz	2MB	800MHz	Dual	No	**No**	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor E4500	2.20GHz	2MB	800MHz	Dual	No	**No**	Yes	Yes	Yes	No	July 2007
Intel Core 2 Duo processor E4600	2.40GHz	2MB	800MHz	Dual	No	**No**	Yes	Yes	Yes	No	Oct 2007
Intel Core 2 Duo processor E4700	2.60GHz	2MB	800MHz	Dual	No	**No**	Yes	Yes	Yes	No	Mar 2008
Intel Core 2 Duo processor E6300	1.86GHz	2MB	1066MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor E6320	1.86GHz	**4MB**	1066MHz	Dual	No	Yes	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor E6400	2.13GHz	2MB	1066MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor E6420	2.13GHz	**4MB**	1066MHz	Dual	No	Yes	Yes	Yes	Yes	No	Apr 2007
Intel Core 2 Duo processor E6540	2.33GHz	**4MB**	1333MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2007
Intel Core 2 Duo processor E6550	2.33GHz	**4MB**	1333MHz	Dual	No	Yes	Yes	Yes	Yes	**Yes**	July 2007
Intel Core 2 Duo processor E6600	2.40GHz	**4MB**	1066MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor E6700	2.66GHz	**4MB**	1066MHz	Dual	No	Yes	Yes	Yes	Yes	No	July 2006
Intel Core 2 Duo processor E6750	2.66GHz	**4MB**	1333MHz	Dual	No	Yes	Yes	Yes	Yes	**Yes**	July 2007
Intel Core 2 Duo processor E6850	3.00GHz	**4MB**	1333MHz	Dual	No	Yes	Yes	Yes	Yes	**Yes**	July 2007

Processor generation	**Conroe**
Marketing name	**Intel Core 2 Duo desktop processor**
Core	**Dual-core**
Branding	Part of the **Intel Viiv™ technology** for the home and **Intel vPro™ technology** for business

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Power mgmt technology	Enhanced Intel SpeedStep™ technology
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Virtualization Technology	*Some:* Intel Virtualization Technology
Intel Trusted Execution Technology	*Some:* enables more secure platforms from software-based attacks with appropriate software
Intel Dynamic Acceleration	No

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache, integrated
L1 instruction cache	2x32KB instruction cache, integrated

L2 cache - size	**2MB** or **4MB**, full speed, shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None

System bus	**800MHz, 1066MHz,** or **1333MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset), 36-bit addressing
System bus - width	64-bit data path

Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	65nm
Thermal Design Power	65 watts
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA6) package** requires **LGA775 socket** (socket also called Socket T)
Chipset support	**Intel Q963, Q965, G965, P965, 946, 975X Express Chipset families;** other compatible chipsets

(C2DE) Compiled by Roger Dodson, Lenovo. March 2008

[Desktop] Intel Core 2 Duo Processor (Wolfdale)

Intel® Core™ 2 Duo processor for desktop systems	Clock Perf Mode	Shared L2 cache	System bus MHz	Core	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Trusted Execution Tech	Intel Dynamic Acceleration	Avail-able date
Intel Core 2 Duo processor E7200	2.53GHz	3MB	1066MHz	Dual	**No**	Yes	Yes	Yes	**No**	No	Apr 2008
Intel Core 2 Duo processor E7300	2.66GHz	3MB	1066MHz	Dual	**No**	Yes	Yes	Yes	**No**	No	Aug 2008
Intel Core 2 Duo processor E7400	2.80GHz	3MB	1066MHz	Dual	**No**	Yes	Yes	Yes	**No**	No	Oct 2008
Intel Core 2 Duo processor E8190	2.66GHz	6MB	1333MHz	Dual	**No**	Yes	Yes	Yes	**No**	No	Jan 2008
Intel Core 2 Duo processor E8200	2.66GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No	Jan 2008
Intel Core 2 Duo processor E8300	2.83GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No	Apr 2008
Intel Core 2 Duo processor E8400	3.00GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No	Jan 2008
Intel Core 2 Duo processor E8500	3.16GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No	Jan 2008
Intel Core 2 Duo processor E8600	3.33GHz	6MB	1333MHz	Dual	Yes	Yes	Yes	Yes	Yes	No	May 2008

Processor generation	**Wolfdale**
Marketing name	**Intel Core 2 Duo desktop processor**
Core	**Dual-core**
Branding	Supports **Intel Core 2 Processor with Viiv™ technology** and **Intel Core 2 Processor with vPro™ technology** when hardware and software requirements met

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power mgmt technology	Enhanced Intel SpeedStep™ technology
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Virtualization Technology	*Some:* Intel Virtualization Technology
Intel Trusted Execution Technology	*Some:* Enables more secure platforms from software-based attacks with appropriate software
Intel Dynamic Acceleration	None

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache, integrated
L1 instruction cache	2x32KB instruction cache, integrated

L2 cache - size	**3MB** or **6MB**, full speed, shared between both cores (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated, unified (on die)
L3 cache	None

System bus (front side bus)	**1066MHz** or **1333MHz** (transfers data 4 times per clock), address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset), 36-bit addressing
System bus - width	64-bit data path

Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	45nm
Thermal Design Power	65 watts
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA8) package** requires **LGA775 socket** (socket also called Socket T)
Chipset support	Intel 3 Series and Intel 4 Series Express Chipset families; other compatible chipsets

Intel® Core™ 2 Extreme processor for desktop systems	Clock Perf Mode	L2 cache	System bus MHz	Core	Thermal Design Power	Socket	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech (EM64T)	Avail-able date
Intel Core 2 Extreme processor X6800	2.93GHz	4MB	1066MHz	Dual	75W	LGA775	Yes	Yes	Yes	Yes	July 2006
Intel Core 2 Extreme processor QX6700	2.66GHz	8MB	1066MHz	Quad	75W	LGA775	Yes	Yes	Yes	Yes	Apr 2007
Intel Core 2 Extreme processor QX6800	2.93GHz	8MB	1066MHz	Quad	75W	LGA775	Yes	Yes	Yes	Yes	Apr 2007
Intel Core 2 Extreme processor QX6850	3.00GHz	8MB	1333MHz	Quad	75W	LGA775	Yes	Yes	Yes	Yes	July 2007
Intel Core 2 Extreme processor QX9650	3.00GHz	12MB	1333MHz	Quad	130W	LGA775	Yes	Yes	Yes	Yes	Nov 2007
Intel Core 2 Extreme processor QX9770	3.20GHz	12MB	1600MHz	Quad	136W	LGA775	Yes	Yes	Yes	Yes	Nov 2007
Intel Core 2 Extreme processor QX9775	3.20GHz	12MB	1600MHz	Quad	150W	LGA771	Yes	Yes	Yes	Yes	Feb 2008

Processor generation	**Conroe (X6800)** or **Kentsfield (QX6xxx)** or **Yorkfield-XE (QX9xxx)**
Marketing name	**Intel Core 2 Extreme processor**
Core	**Dual-core** or **quad-core**
Branding	Part of the **Intel Viiv™ technology** for the home and **Intel vPro™ processor technology** for business

Micro-architecture	Intel Core micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline;
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	*QX9xxx:* Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power mgmt technology	Enhanced Intel SpeedStep™ technology
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two or four threads (two or four cores with no Hyper-Threading)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology

L1 cache	64KB per core split between data cache (32KB) and instuction cache (32KB)
L1 data cache	2x32KB data cache / integrated
L1 instruction cache	2x32KB instruction cache / integrated

L2 cache - size	*X6800:* **4MB** / full speed / shared between both cores (Intel Advanced Smart Cache)
	QX6xxx: **8MB** / full speed / 2 x 4MB shared cache on each die [dual-die] (Intel Advanced Smart Cache)
	QX9xxx: **12MB** / full speed / 2 x 6MB shared cache on each die [dual-die] (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None

System bus	**1066MHz** or **1333MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset) / 36-bit addressing
System bus - width	64-bit data path

Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	*Others:* 65nm or 0.065u
	QX9xxx: 45nm or 0.045u
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA6) package** requires **LGA771** or **LGA775 socket** (also called Socket T)
Chipset support	Intel Q963, Q965, G965, P965, 975X Express Chipset families; Intel 3 Series; other compatible chipsets

[Desktop] Intel Core 2 Quad Processor

Intel® Core™ 2 Quad processor for desktop systems	Clock Perf Mode	L2 cache	System bus MHz	Cores	Hyper-Threading Technology	Total threads (logical)	Virtual-ization Tech	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Trusted Execution Tech	Avail-able date
Intel Core 2 Quad processor Q6600	2.40GHz	8MB	1066MHz	Quad	No	4	Yes	Yes	Yes	No	Jan 2007
Intel Core 2 Quad processor Q6700	2.66GHz	8MB	1066MHz	Quad	No	4	Yes	Yes	Yes	No	July 2007
Intel Core 2 Quad processor Q8200	2.33GHz	4MB	1333MHz	Quad	No	4	No	Yes	Yes	No	Aug 2008
Intel Core 2 Quad processor Q8300	2.50GHz	4MB	1333MHz	Quad	No	4	No	Yes	Yes	No	Dec 2008
Intel Core 2 Quad processor Q9300	2.50GHz	6MB	1333MHz	Quad	No	4	Yes	Yes	Yes	Yes	Mar 2008
Intel Core 2 Quad processor Q9400	2.66GHz	6MB	1333MHz	Quad	No	4	Yes	Yes	Yes	Yes	Aug 2008
Intel Core 2 Quad processor Q9450	2.66GHz	12MB	1333MHz	Quad	No	4	Yes	Yes	Yes	Yes	Mar 2008
Intel Core 2 Quad processor Q9550	2.83GHz	12MB	1333MHz	Quad	No	4	Yes	Yes	Yes	Yes	Mar 2008
Intel Core 2 Quad processor Q9650	3.00GHz	12MB	1333MHz	Quad	No	4	Yes	Yes	Yes	Yes	Aug 2008

Processor generation	**Kentsfield (Q6xxx)** or **Yorkfield (Q8xxx, Q9xxx)**
Marketing name	**Intel Core 2 Quad desktop processor**
Core	**Quad-core** (dual-core on dual-die so essentially two Core 2 Duo processors joined together)
Branding	Supports **Intel Core 2 Processor with Viiv™ technology** and **Intel Core 2 Processor with vPro™ technology** when hardware and software requirements met

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline;
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Accelerates execution of Streaming SIMD Extension (SSE2/3) instructions used in multimedia applications
Intel HD Boost	*Q8xxx/Q9xxx:* Streaming SIMD Extensions 4 (SSE4) and faster Super Shuffle Engine
Power mgmt technology	Enhanced Intel SpeedStep™ technology
Thermal management	Digital thermal sensor
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1] (EM64T)	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Virtualization Technology	*Some:* Intel Virtualization Technology
Intel Trusted Execution Technology	*Some:* Enables more secure platforms from software-based attacks with appropriate software
Intel Dynamic Acceleration	No

L1 cache	Four 32KB per core, integrated

L2 cache - size	**4MB**, **6MB**, **8MB**, or **12MB** / full speed, 2 x 3MB/4MB/6MB shared cache on each die [dual-die] (Intel Advanced Smart Cache)
L2 cache - data path	256-bit data path (32 bytes), 64 byte cache line size, 8-way set associative, integrated
L3 cache	None

System bus	**1066MHz** or **1333MHz** (transfers data 4 times per clock), address bus transfers at 2 times per clock
Memory addressability	64GB memory addressability (but limited by chipset), 36-bit addressing
System bus - width	64-bit data path

Execution units per core	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software

Process technology	*Q6xxx:* 65nm; *Q8xxx/9xxx:* 45nm
Thermal Design Power	*Q6xxx:* 65 watts; *Q8xxx/9xxx:* 95 watts
Package and connector	*Q6xxx:* **775-land Flip-Chip Land Grid Array (FC-LGA6) package** requires **LGA775 socket** (socket also called Socket T)
	Q8xxx/9xxx: **775-land Flip-Chip Land Grid Array (FC-LGA8) package** requires **LGA775 socket** (socket also called Socket T)
Chipset support	Intel 3 Series and Intel 4 Series desktop chipset; other compatible chipsets

[Desktop] Intel Core i7 Processor

Intel® Core™ i7 processor for desktops	Clock speed	Shared L3 cache	Quick Path Interconnect	Core	Virtual- ization Tech	Hyper- Threading Tech	Intel 64 Tech	Intel Turbo Boost	Avail- able date
Intel Core i7-920 Processor	2.66GHz	8MB	4.8GT/s	Quad	Yes	Yes	Yes	Yes	Jan 2009
Intel Core i7-940 Processor	2.93GHz	8MB	4.8GT/s	Quad	Yes	Yes	Yes	Yes	Jan 2009

Processor generation	**Bloomfield** (Nehalem)
Marketing name	**Intel Core i7 processor**
Core	**Quad-core**

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Streaming SIMD Extensions (SSE2, SSE3)
Intel HD Boost	Streaming SIMD Extensions 4 (SSE4), Super Shuffle Engine, SSE4.2
Power mgmt technology	Enhanced Intel SpeedStep™ technology, power management capabilities, multiple low-power states
Hyper-Threading	Intel Hyper-Threading Technology[2]
Total threads	Eight threads (four cores with Hyper-Threading support provide eight threads)
Execute Disable Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (extension to IA-32 instruction set adding 64-bit extensions)
Virtualization Technology	Intel Virtualization Technology
Intel Trusted Execution Technology	None
Intel Dynamic Acceleration	None
Turbo Boost	Intel Turbo Boost Technology[3] (scales processor frequency higher)

L1 cache	64KB per core, split between data cache (32KB) and instuction cache (32KB), 8-way set associative
L2 cache	256KB per core, unified, 8-way set associative
L3 cache	8MB shared among all cores (Intel Smart Cache), 16-way set associative

Memory controller	Integrated memory controller
Memory support	DDR3, three channels max, two DIMMs per channel max, 24GB max, 800/1066MHz
System bus (front side bus)	None
QuickPath Interconnect	Intel QuickPath Interconnect, point-to-point link between processor and chipset, 4.8GT/sec max

Compatibility	Compatible with IA-32 software

Process technology	45nm
Thermal Design Power	130 watts
Package and connector	**1366-land Flip-Chip Land Grid Array (FC-LGA8) package** requires **LGA1366 socket**

Chipset support	Intel X58 Express Chipset families; other compatible chipsets

[Desktop] Intel Core i7 Processor Extreme Edition

Intel® Core™ i7 processor Extreme Edition for desktops and workstations	Clock speed	Shared L3 cache	Quick Path Interconnect	Core	Virtual- ization Tech	Hyper- Threading Tech	Intel 64 Tech	Intel Turbo Boost	Avail- able date
Intel Core i7-965 Processor Extreme Edtion	3.2GHz	8MB	6.4GT/s	Quad	Yes	Yes	Yes	Yes	Jan 2009

Processor generation	**Bloomfield** (Nehalem)
Marketing name	**Intel Core i7 processor Extreme Edition**
Core	**Quad-core**

Micro-architecture	Intel Core Micro-architecture
Intel Wide Dynamic Execution	Each core can complete up to four full instructions simultaneously using 14-stage pipeline
Intel Smart Memory Access	Hides memory latency
Intel Advanced Digital Media Boost	Streaming SIMD Extensions (SSE2, SSE3)
Intel HD Boost	Streaming SIMD Extensions 4 (SSE4), Super Shuffle Engine, SSE4.2
Power mgmt technology	Enhanced Intel SpeedStep™ technology, power management capabilities, multiple low-power states
Hyper-Threading	Intel Hyper-Threading Technology[2]
Total threads	Eight threads (four cores with Hyper-Threading support provide eight threads)
Execute Disable Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (extension to IA-32 instruction set adding 64-bit extensions)
Virtualization Technology	Intel Virtualization Technology
Intel Trusted Execution Technology	None
Intel Dynamic Acceleration	None
Turbo Boost	Intel Turbo Boost Technology[3] (scales processor frequency higher)

L1 cache	64KB per core, split between data cache (32KB) and instuction cache (32KB), 8-way set associative
L2 cache	256KB per core, unified, 8-way set associative
L3 cache	8MB shared among all cores (Intel Smart Cache), 16-way set associative

Memory controller	Integrated memory controller
Memory support	DDR3, three channels max, two DIMMs per channel max, 24GB max, 800/1066MHz
System bus (front side bus)	None
QuickPath Interconnect	Intel QuickPath Interconnect, point-to-point link between processor and chipset, 6.4GT/sec max

Compatibility	Compatible with IA-32 software

Process technology	45nm
Thermal Design Power	130 watts
Package and connector	**1366-land Flip-Chip Land Grid Array (FC-LGA8) package** requires **LGA1366 socket**

Chipset support	Intel X58 Express Chipset families; other compatible chipsets

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[1] **Intel 64 Technology (formerly EM64T):** Intel 64 Technology (formerly Intel EM64T) requires a computer system with a processor, chipset, BIOS, operating system, device drivers, and applications enabled for Intel 64 Technology. Processor will not operate (including 32-bit operation) without an Intel 64 Technology-enabled BIOS. Performance will vary depending on your hardware and software configurations.

[2] **Intel Hyper-Threading Technology (HT Technology):** Intel Hyper-Threading Technology requires a computer system with a processor supporting HT Technology and an HT Technology-enabled chipset, BIOS, and operating system. Performance will vary depending on the specific hardware and software you use. For more information, including details on which processors support HT Technology, see www.intel.com/info/hyperthreading.

[3] **Intel Turbo Boost Technology:** Intel Turbo Boost Technology requires a PC with a processor with Intel Turbo Boost Technology capability. Intel Turbo Boost Technology performance varies depending on hardware, software, and overall system configuration. Check with your PC manufacturer on whether your system delivers Intel Turbo Boost Technology. See www.intel.com/info/technology/turboboost for more information.

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