Technical Information Manual

PC 300GL Types 6267, 6277, and 6287

Preliminary Edition (November 1998)

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Preface

This *Technical Information Manual* provides information for the IBM PC 300GL Types 6267, 6277, and 6287. It is intended for developers who want to provide hardware and software products to operate with these IBM computers and provides an in-depth view of how these IBM computers work. Users of this publication should have an understanding of computer architecture and programming concepts.

Related Publications

In addition to this manual, the following IBM publications provide information related to the operation of the IBM PC 300GL. To order publications in the U.S. and Puerto Rico, call 1-800-879-2755. In other countries, contact an IBM reseller or an IBM marketing representative.

- *PC 300GL User Guide*
  This publication contains information about configuring, operating, and maintaining the PC 300GL, as well as installing new options in the PC 300GL. Also included are warranty information, instructions for diagnosing and solving problems, and information on how to obtain help and service.

- *Understanding Your Personal Computer*
  This online document includes general information about using computers and detailed information about the features of the PC 300GL.

- *About Your Software*
  This publication (provided only with computers that have IBM-preinstalled software) contains information about the preinstalled software package.

- *Hardware Maintenance Manual*
  This publication contains information for trained service technicians. It is available at http://www.pc.ibm.com/us/cdt/hmm.html on the World Wide Web, and it can also be ordered from IBM. To purchase a copy, refer to the "Getting Help, Service, and Information" section in *PC 300GL User Guide*.

- *Compatibility Report*
  This publication contains information about compatible hardware and software for the PC 300GL. It is available at http://www.pc.ibm.com/us/cdt on the World Wide Web.

- *Network Administrator's Guide*
  This publication contains information for network administrators who configure and service local area networks (LANs). Look for this publication at http://www.pc.ibm.com/us/cdt on the World Wide Web.

Terminology Usage

Attention! The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

In this manual, some signals are represented in a small, all-capital-letter format (-ACK). A minus sign in front of the signal indicates that the signal is active low. No sign in front of the signal indicates that the signal is active high.

The use of the term *hex* indicates a hexadecimal number. Also, when numerical modifiers such as "K", "M" and "G" are used, they typically indicate powers of 2, not powers of 10. For example, 1 KB equals 1 024 bytes (2^{10}), 1 MB equals 1 048 576 bytes (2^{20}), and 1 GB equals 1 073 741 824 bytes (2^{30}).

When expressing storage capacity, MB equals 1 000 KB (1 024 000). The value is determined by counting the number of sectors and assuming that every two sectors equals 1 KB.

Note: Depending on the operating system and other system requirements, the storage capacity available to the user might vary.

Chapter 1. System Overview

PC 300GL Types 6267, 6277, and 6287 are minitower systems designed to provide state-of-the-art computing power with room for future growth.

Major Features

The major features are:

- An Intel® Pentium® II microprocessor with MMX™ technology and 100 MHz Front Side Bus (FSB), with 512 KB of L2 cache with ECC
  Or

- An Intel Celeron™ microprocessor with MMX technology, with 128 KB L2 cache

- Up to 384 MB of system memory

- Integrated IDE bus master controller, Ultra DMA/33 capable

- EIDE hard disk drive

- System management

  - Wake on LAN support
  - DMI (Desktop Management Interface) BIOS and DMI software
  - Integrated network protocols
  - Enablement for remote administration
  - Universal Management Agent (UMA) and UMA Plus

- 32X Max IDE CD-ROM[1] drive, standard on some models

- Asset security

  - Security settings provided by the Configuration/Setup Utility Program
    - Power-on and administrator password protection
    - Startup sequence control
    - Hard disk drive and diskette drive access control
    - I/O port control
  - Cover lock loop
  - U-bolt and security cabling (optional)
  - Operating system security
  - Diskette write-protection

- Integrated AGP S3 Trio3D SVGA video controller with 2 MB of SDRAM video memory (can be upgraded to 4 MB) in some models and 4 MB of SDRAM video memory in other models

- Audio adapter (supports SoundBlaster, Adlib, and Microsoft Windows Sound System applications) is optional in some models

- Integrated 16-bit, stereo ESS 1938 audio controller and built-in high quality speaker in some models (supports SoundBlaster, Adlib, and Microsoft Windows Sound System applications)

- Networking

  - IBM 10/100 Mbit, PCI Ethernet adapter with Wake on LAN in some models.

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[1] Variable read rate. Actual playback speed will vary and is often less than the maximum possible.

> – IBM PCI token ring adapter with Wake on LAN is optional.

- Expansion

  – Four drive bays, four expansion slots (one ISA, three PCI)

- ISA/PCI I/O-bus compatibility

- Industry-standard compatibility

- EnergyStar compliance

- 3.5-inch, 1.44 MB diskette drive

- Input/Output Features

  – One 25-pin, ECP/EPP parallel port
  – Two 9-pin, UART serial ports
  – Two 4-pin, USB ports
  – One 6-pin, keyboard port (Windows 95-compatible)
  – One 6-pin, mouse port
  – One 15-pin, DDC2B-compliant monitor port
  – Three 3.5 mm audio jacks (line out, headphone, microphone) on models with integrated sound system.

Other Features

The following features may be supported by the PC 300GL.

Wake on LAN

The power supply of the computer supports the Wake on LAN feature. With the Wake on LAN feature, the computer can be turned on when a specific LAN frame is passed to the PC over the LAN.

To use the Wake on LAN feature, the computer must be equipped with a network subsystem that supports Wake on LAN.

The menu used for setting the Wake on LAN feature is found in the Configuration/Setup Utility Program.

Wake Up on Ring

All models are configurable to turn on the computer after a ring is detected from an external or internal modem. The menu used for setting the Wake Up on Ring feature is found in the Configuration/Setup Utility Program. Two options control this feature:

- **Serial Ring Detect:** Use this option if the computer has an external modem connected to the serial port.

- **Modem Ring Detect:** Use this option if the computer has an internal modem.

Network Enablement

PC 300GL computers are enabled to support management over a network. The following is a list of supported functions:

- Selectable startup sequence
- Selectable Automatic Power On Startup Sequence
- Update POST/BIOS from network
- Wake on LAN

- CMOS Save/Restore utility program
- CMOS setup over LAN
- Wake Up on Ring

Chapter 2. System Board Features

This section includes information about system-board features. For an illustration of the system board, see "System Board, Types 6267, 6277, and 6287" on page 13.

Microprocessor

PC 300GL Types 6267, 6277, and 6287 comes with an Intel Pentium II microprocessor with MMX technology or an Intel Celeron microprocessor. The microprocessor, which has a heat sink attached, plugs directly into a connector on the system board.

Pentium II Microprocessor with MMX Technology

The features of this microprocessor are as follows:

- Optimization for 32-bit software
- Operation at a lower voltage level than previous microprocessors
- 64-bit microprocessor data bus
- 100 MHz FSB
- 512 KB L2 cache with ECC
- 32-bit microprocessor address bus
- Math coprocessor
- MMX technology, which boosts the processing of graphic, video, and audio data
- L2 cache integrated into the microprocessor
- Cache operates at 1/2 processor core speed
  - 4-way set associative
  - Nonblocking

More information on these microprocessors is available at http://www.intel.com on the World Wide Web.

Celeron Microprocessor with MMX Technology

The features of this microprocessor are as follows:

- Optimization for 32-bit software
- Operation at a lower voltage level than previous microprocessors
- 64-bit microprocessor data bus
- 66 MHz FSB
- 128 KB L2 cache
- 32-bit microprocessor address bus
- Math coprocessor
- MMX technology, which boosts the processing of graphic, video, and audio data
- L2 cache integrated into the microprocessor
- Cache operates at processor core speed
  - 4-way set associative
  - Nonblocking

Chip Set Control

Two components, the Intel 440BX and PIIX4E, make up the chip set that is the interface between the microprocessor and the following:

- Memory subsystem
- PCI bus
- IDE Bus Master connection
- High-performance, PCI-to-ISA bridge
- USB ports
- SMBus
- Enhanced DMA controller

L2 Cache

The Pentium II microprocessor with MMX technology provides 512 KB of L2 cache with ECC. The Celeron microprocessor provides 128 KB L2 cache. The L2 cache ECC function is automatically enabled when ECC memory is installed. If nonparity memory is installed, the L2 cache ECC is disabled. (For information on overriding these settings, refer to Chapter 5, Configuration/Setup Utility Program, in *PC 300GL User Guide.*)

System Memory

The system memory interface is controlled by the 440BX chip set. Synchronous dynamic random access memory (SDRAM) is standard.

The maximum amount of system memory is 384 MB on some models and 256 MB on some models. For memory expansion, some system board models provide three dual inline memory module (DIMM) connectors. Other models provide two DIMM connectors. 100 MHz DIMMs in sizes of 16 MB, 32 MB, 64 MB, and 128 MB are supported. The amount of memory preinstalled varies by model.

The following information applies to system memory:

- SDRAM (synchronous dynamic random access memory), nonparity memory is standard.
- Error correcting code (ECC) is supported in Pentium II models
- The maximum height of memory modules is 3.18 cm (1.25 in.).
- Only PC 100 industry-standard, gold-lead DIMMs are supported.
- A mix of ECC and nonparity types configures as nonparity.

For information on the pin assignments for the memory module connectors, see "Memory Connectors" on page 28.

Chapter 2. System-Board Features

The following figure shows some possible configurations for the supported DIMMs.

Note: Values in the following table are represented in megabytes (MB).

Figure 1. Memory Configurations			
Total Memory (MB)	**Mem 0**	**Mem 1**	**Mem2**[2]
16	16	0	0
32	16	16	0
32	32	0	0
48	16	16	16
48	32	16	0
64	32	16	16
64	32	32	0
64	64	0	0
96	32	32	32
96	64	32	0
128	64	32	32
128	64	64	0
128	128	0	0
160	32	64	64
192	64	64	64
224	32	64	128
256	128	64	64
256	128	128	0
288	32	128	128
384	128	128	128

PCI Bus

The fully synchronous 33 MHz PCI bus originates in the chip set. Features of the PCI bus are:

- Integrated arbiter with multitransaction PCI arbitration acceleration hooks
- Zero-wait-state, microprocessor-to-PCI write interface for high performance graphics
- Built-in PCI bus arbiter with support for up to five masters
- Microprocessor-to-PCI memory write posting with 5-Dword-deep buffers
- Converts back-to-back sequential microprocessor-to-PCI memory write to PCI burst write
- PCI-to-DRAM posting 18 Dwords
- PCI-to-DRAM up to 100+ MB/sec bandwidth
- Multitransaction timer to support multiple short PCI transactions within one PCI ARB cycle
- PCI 2.1 compliant
- Delayed transaction
- PCI parity checking and generation support

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[2] Only in some Pentium II models

IDE Bus Master Interface

The system board incorporates a PCI-to-IDE interface that complies with the *AT Attachment Interface with Extensions*.

The Intel PIIX4E bridge functions as a *bus master* for the IDE interface. The chip set is PCI 2.1 compliant. It connects directly to the PCI bus and is designed to allow concurrent operations on the PCI bus and IDE bus. The chip set is capable of supporting PIO mode 0–4 devices and IDE DMA mode 0–2 devices, Ultra DMA 33 transfers up to 33 Mbytes/sec.

The IDE devices receive their power through a four-position power cable containing +5, +12, and ground voltage. When adding devices to the IDE interface, one device is designated as the master device and another is designated as the slave or subordinate device. These designations are determined by switches or jumpers on each device. There are two IDE ports, one designated 'Primary' and the other 'Secondary,' allowing for up to four devices to be attached. The total number of physical IDE devices is dependent on the mechanical package.

For the IDE interface, no resource assignments are given in the system memory or the direct memory access (DMA) channels. For information on the resource assignments, see "Input/Output Address Map" on page 40 and Figure 44 on page 44 (for IRQ assignments).

Two connectors are provided on the riser for the IDE interface. For information on the connector pin assignments, see "IDE Connectors" on page 35.

PCI-to-ISA Bridge

On the system board, the Intel PIIX4E bridge provides the interface between the peripheral component interface (PCI) and industry standard architecture (ISA) buses. The chip set is used to convert PCI bus cycles to ISA bus cycles; the chip set also includes all the subsystems of the ISA bus, including two cascaded interrupt controllers, two DMA controllers with four 8-bit and three 16-bit channels, three counters equivalent to a programmable interval timer, and power management. The PCI bus operates at 33 MHz. The ISA bus operates at 8.25 MHz.

For the ISA bus, no resource assignments are given in the system memory or the DMA channels. For information on resource assignments, see "Input/Output Address Map" on page 40 and Figure 44 on page 44 (for IRQ assignments).

USB Interface

Universal serial bus (USB) technology is a standard feature of the computer. Using the chip set, the system board provides the USB interface with two connectors. A USB-enabled device can attach to each connector, and if that device is a hub, multiple peripherals can attach to the hub and be used by the system. The USB connectors use Plug and Play technology for installed devices. The speed of the USB is up to 12 MB/sec with a maximum of 127 peripherals. The USB is compliant with Universal Host Controller Interface Guide 1.0.

Features provided by USB technology include:

- Support for hot-pluggable devices
- Support for concurrent operation of multiple devices
- Suitable for different device bandwidths
- Support for up to five meters length from host to hub or from hub to hub
- Guaranteed bandwidth and low latencies appropriate for specific devices
- Wide range of packet sizes

- Limited power to hubs

For information on the connector pin assignments for the USB interface, see "USB Port Connectors" on page 37.

Video Subsystem

The video subsystem on the system board includes the Integrated AGP S3 Trio3D SVGA (super video graphics array) controller. The system board supports up to two SGRAM memory modules. Each module contains 2 MB of SGRAM memory.

Integrated AGP S3 Trio3D SVGA (Super Video Graphics Array)

The Integrated AGP S3 Trio3D SVGA (super video graphics array) supports all video graphics array (VGA) modes and is compliant with super video graphics array (SVGA) modes and Video Electronics Standards Association (VESA) 1.2. Some enhanced features are:

- Plug and Play support
- 100 MHz SGRAM support
- Advanced Power Management support
- Color space conversion
- Hardware scaling

The PC 300GL has an AGP bus and is AGP 1.0 compliant. The S3 Trio3D video subsystem supports the VESA Display Data Channel (DDC) standard 1.1 and uses DDC1 and DDC2B to determine optimal values during automatic monitor detection.

The video subsystem has the following resource assignments:

Figure 2. Video Subsystem Resources	
Resource	**Assignment**
ROM (hex)	C0000–C7FFF (32KB)
RAM (hex)	A0000–BFFFF
I/O (hex)	VGA, Sequencer, CRT controller, graphics controller, attribute, RAMDAC, extended sequencer, extended CRTC Registers
IRQ	PCI interrupt #2 (automatically assigned to ISA IRQ 9 by POST or can be disabled in Setup Utility)
DMA	None

For further information on resource assignments, see Appendix B, "System Address Maps" on page 40 and Appendix C, "IRQ and DMA Channel Assignments" on page 44.

The PC 300GL supports the following video subsystem modes:

Mode (hex)	Display Mode	Screen Resolution	Colors	Buffer Start (hex)	Dot Clock (MHz)	Sweep Rate (kHz)	Refresh Rate (Hz)
00	Text	40 x 25 characters	2	B8000	28.322	31.5	70
01	Text	40 x 25 characters	16	B8000	28.322	31.5	70
02	Text	80 x 25 characters	B/W	B8000	28.322	31.5	70
03	Text	80 x 25 characters	16	B8000	28.322	31.5	70
04	Graphics	320 x 200 pixels	4	B8000	25.175	31.5	70
05	Graphics	320 x 200 pixels	4	B8000	25.175	31.5	70
06	Text	640 x 200 pixels	2	B8000	25.175	31.5	70
07	Text	80 x 25 characters	Mono	B0000	28.322	31.5	70
0D	Graphics	320 x 200 pixels	16	A0000	25.175	31.5	70
0E	Graphics	640 x 200 pixels	16	A0000	25.175	31.5	70
0F	Graphics	640 x 350 pixels	Mono	A0000	25.175	31.5	70
10	Graphics	640 x 350 pixels	16	A0000	25.175	31.5	70
11	Graphics	640 x 480 pixels	2	A0000	25.175	31.5	60
12	Graphics	640 x 480 pixels	16	A0000	25.175	31.5	60
13	Graphics	320 x 200 pixels	256	A0000	25.175	31.5	70

Figure 3. Supported VGA Video Modes

The video subsystem provides a 15-pin monitor connector on the system board. For information on connector pin assignments, see "AGP Monitor Port Connector" on page 28.

Video Memory

The video memory interface is controlled by an S3 Trio3D graphics controller. Some models are shipped with 4 MB SGRAM with the video subsystem, other models are shipped with 2MB SGRAM.

The video memory is 2 MB 256K X32 socket with 100MHz SGRAM. The video memory can be upgraded from 2 MB SGRAM to 4 MB SGRAM with a 2 MB SGRAM 100 MHz SODIMM. The SODIMM can be plugged into the SODIMM socket on the system board. For details, see *PC 300GL User Guide*.

Audio Subsystem

Some PC 300GL models come with an ESS 1938 integrated audio controller. These models, which are capable of playing and recording sounds, support SoundBlaster, Adlib, and Microsoft Windows Sound System applications.

The device drivers for the preinstalled audio adapter are on the hard disk drive. The device drivers are also available on the *Software Selections* CD provided with all models.

If you connect an optional device to the audio adapter, follow the instructions provided by the manufacturer. (Note that device drivers might be required. If necessary, contact the manufacturer for information on these device drivers.)

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3 An electronic device connected to the joystick/MIDI connector might require an optional adapter cable. For more information, refer to the documentation that comes with the electronic device.

The following connectors are available on the audio adapter or integrated audio controller:

- *Joystick/MIDI (Musical Instrument Digital Interface)* for connecting a game control or a musical device, such as an electronic keyboard. This feature is available on some models only.

- *Line Out* port for connecting powered speakers. Your audio system requires a set of speakers connected to the Line Out port in order to hear audio from the adapter. These speakers must be powered with a built-in amplifier. In general, any powered speakers designed for use with personal computers can be used with your audio adapter. These speakers are available with a wide range of features and power outputs.

- *Headphone* port for connecting Headphones. In general, any headphones designed for use with personal computers can be used with your audio adapter.

- *Microphone* for connecting a microphone.

Input/Output Controller

Control of the integrated input/output (I/O) and diskette drive controllers is provided by a single module, the SMC 37C673. This module, which supports Plug and Play, controls the following features:

- Diskette drive interface
- Serial port
- Parallel port
- Keyboard and mouse ports
- General purpose I/O ports

Diskette Drive Interface

The PC 300GL has four drive bays for installing internal devices. The following is a list of devices that the diskette drive subsystem supports:

- 1.44 MB, 3.5 inch diskette drive
- 1.44 MB, 3.5 inch, 3-mode drive for Japan (no BIOS support for 3-mode drive)
- 1.2 MB, 5.25 inch diskette drive
- 1 Mbps, 500 Kbps, or 250 Kbps internal tape drive

One connector is provided on the system board for diskette drive support. For information on the connector pin assignments, see "Diskette Drive Connector" on page 36.

Serial Ports

One universal asynchronous receiver/transmitter (UART) serial port is integrated into the system board. The serial port includes a 16-byte data, first-in first-out (FIFO) buffer, and has programmable baud rate generators. The serial port is NS16450 and PC16550A compatible.

For information on the connector pin assignments, see "Serial Port Connector" on page 38.

Note: Current loop interface is not supported.

The following figure shows the serial port assignments in the configuration.

Figure 4 (Page 1 of 2). Serial Port Assignments		
Port Assignment	**Address Range (hex)**	**IRQ Level**
Serial 1	03F8–03FF	IRQ4
Serial 2	02F8–02FF	IRQ3

Figure 4 (Page 2 of 2). Serial Port Assignments		
Port Assignment	Address Range (hex)	IRQ Level
Serial 3	03E8–03FF	IRQ4
Serial 4	02E8–02FF	IRQ3

The default setting for the serial port is COM1.

Parallel Port

Integrated in the system board is support for extended capabilities port (ECP), enhanced parallel port (EPP), and standard parallel port (SPP) modes. The modes of operation are selected through the Configuration/Setup Utility Program with the default mode set to SPP. The ECP and EPP modes are compliant with IEEE 1284.

The following figure shows the parallel port assignments used in the configuration.

Figure 5. Parallel Port Assignments		
Port Assignment	Address Range (hex)	IRQ Level
Parallel 1	03BC–03BE	IRQ7
Parallel 2	0378–037F	IRQ5
Parallel 3	0278–027F	IRQ5

The default setting for the parallel port is Parallel 1.

The system board has one connector for the parallel port. For information on the connector pin assignments, see "Parallel Port Connector" on page 39.

Keyboard and Mouse Ports

The keyboard and mouse subsystem is controlled by a general purpose 8-bit microcontroller; it is compatible with 8042AH. The controller consists of 256 bytes of data memory and 2 KB of read-only memory (ROM).

The controller has two logical devices: one controls the keyboard and the other controls the mouse. The keyboard has two fixed I/O addresses and a fixed IRQ line and can operate without the mouse. The mouse cannot operate without the keyboard because, although it has a fixed IRQ line, the mouse relies on the addresses of the keyboard for operation. For the keyboard and mouse interfaces, no resource assignments are given in the system memory addresses or DMA channels. For information on the resource assignments, see "Input/Output Address Map" on page 40 and Figure 44 on page 44 (for IRQ assignments).

The system board has one connector for the keyboard port and one connector for the mouse port. For information on the connector pin assignments, see "Mouse and Keyboard Port Connectors" on page 38.

Network Connection

Some PC 300GL models are equipped with an Ethernet adapter that supports the Wake on LAN feature.

Features of the optional Ethernet adapter are:

- Operates in shared 10BASE-T or 100BASE-TX environment
- Transmits and receives data at 10 Mbps or 100 Mbps

- RJ-45 connector for LAN attachment
- Operates in symmetrical multiprocessing (SMP) environments
- Wake on LAN support
- Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP) support

Features of the optional token ring adapter are:

- Transmits and receives data at 4 Mbps or 16 Mbps
- RJ-45 and D-shell connectors for LAN attachment
- Wake on LAN support
- Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP) support

Real-Time Clock and CMOS

The real-time clock is a low-power clock that provides a time-of-day clock and a calendar. The clock settings are maintained by an external battery source of 3 V DC.

The system uses 242 bytes of memory to store complementary metal-oxide semiconductor (CMOS) memory. Moving a jumper on the system board erases CMOS memory.

To locate the battery, see "System Board, Types 6267, 6277, and 6287" on page 13.

Flash EEPROM

The system board uses a 2 MB flash electrically erasable, programmable, read-only memory (EEPROM) to store the basic input/output system (BIOS), video BIOS, IBM logo, Configuration/Setup Utility, and Plug and Play data.

If necessary, the EEPROM can be easily updated using a stand-alone utility program that is available on a 3.5-inch diskette.

Expansion Adapters

Each ISA expansion connector is a 16–bit slot, and each PCI-expansion connector is a 32–bit slot. PCI-expansion connectors support the 32–bit 5 V DC, local-bus signalling environment that is defined in *PCI Local Bus Specification 2.1*. The ISA bus is buffered to provide sufficient drive for the ISA expansion connectors, assuming two low-power Schottky (LS) loads per slot.

The PC 300GL has three PCI slots and one ISA slot to support the addition of adapters. For information on installing adapters, see *PC 300GL User Guide*.

Figure 6. System Board Characteristics	
Expansion Slots	**4x4 System Board**
Dedicated PCI	3
Dedicated ISA	1

For information on the connector pin assignments, see "ISA Connectors" on page 32 and "PCI Connectors" on page 34.

Physical Layout

The system board might look slightly different from the one shown.

Note: A diagram of the system board, including switch and jumper settings, is attached to the underside of the computer cover.

System Board, Types 6267, 6277, and 6287

1 Microprocessor
2 DIMM 0
3 DIMM 1
4 DIMM 2 (Not in some Celeron models)
5 Video memory socket/ Module
6 Wake on LAN connector
7 Primary IDE connector
8 Secondary IDE connector
9 Diskette connector
10 Wake on Ring connector
11 CMOS clear jumper
12 Rocker switch
13 Battery
14 ISA connector
15 CD-ROM audio connector
16 PCI connector 3
17 PCI connector 2
18 PCI connector 1
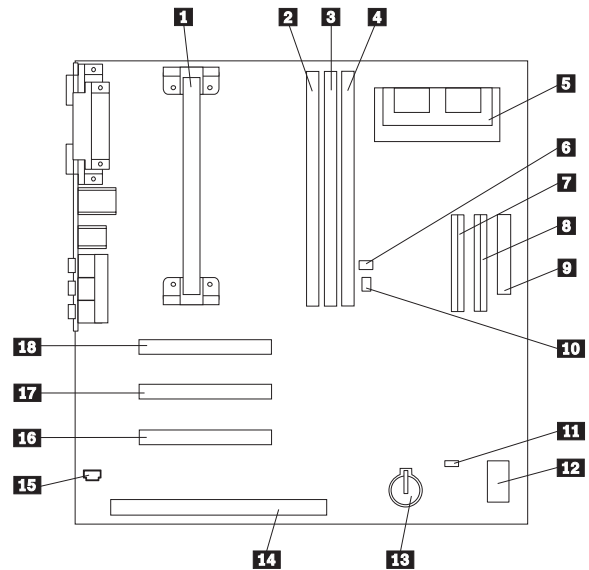
System Board Switches

Switches are provided on the system board to allow for custom configuration. The switches, which are contained in a six-position switch block on the system board, are rocker switches. The side of the rocker that is pushed down is the active side.

Switches 1 through 4 determine the speed of the microprocessor (CPU) and local processor bus. Switch settings for the Intel microprocessors supported by PC 300GL are shown in the following table. Note that the two speeds shown for each microprocessor are the microprocessor core speed followed by the local processor bus speed (for example, 350/100 MHz).

Note: Only the switch values shown in the following table are supported. Using unsupported switch settings will cause unpredictable results.

PC 300GL Types 6267, 6277, and 6287 computers are designed to support both 66 and 100MHz FSB microprocessors.

Figure 7 (Page 1 of 2). Microprocessor Speed 66 MHz FSB (Switches 1-4)					
Microprocessor	**Switch 1**	**Switch 2**	**Switch 3**	**Switch 4**	**Multiplier**
133 MHz	On	On	On	On	2.0
200 MHz	On	Off	On	On	3.0
233 MHz	Off	Off	On	On	3.5

Chapter 2. System-Board Features

Figure 7 (Page 2 of 2). Microprocessor Speed 66 MHz FSB (Switches 1-4)					
Microprocessor	**Switch 1**	**Switch 2**	**Switch 3**	**Switch 4**	**Multiplier**
266 MHz	On	On	Off	On	4.0
300 MHz	Off	On	Off	On	4.5
333 MHz	On	Off	Off	On	5.0
366 MHz	Off	Off	Off	On	5.0

Figure 8. Microprocessor Speed 100 MHz FSB (Switches 1-4)					
Microprocessor	**Switch 1**	**Switch 2**	**Switch 3**	**Switch 4**	**Multiplier**
300 MHz	On	Off	On	On	3.0
350 MHz	Off	Off	On	On	3.5
400 MHz	On	On	Off	On	4.0
450 MHz	Off	On	Off	On	4.5

Switch 5 is ROM Recovery.

Figure 9. ROM Recovery (Switch 5)	
Normal operation	Off (factory default)
ROM Recovery	On

Switch 6 must be on when a Wake on LAN adapter is installed. (Note that only one Wake on LAN device can be used.) Switch 6 controls writes to the diskette drive.

Figure 10. Floppy Device Access (Switch 6)	
Write enabled (factory default)	Off
Write protected	On

Jumper

Jumpers on the system board are used for custom configurations. For the location of the Clear CMOS Request jumper, refer to the "System Board, Types 6267, 6277, and 6287" on page 13, above.

Figure 11. Clear CMOS Clear Jumper (J9)	
Pins	**Description**
1 and 2	Normal (Factory default)
2 and 3	Clear CMOS/Password

Connecting Cables

Connections for attaching devices are provided on the back of the computer. The connectors are:

- USB (2)
- Mouse
- Keyboard
- Serial
- Parallel

- Monitor

- Some models only: Ethernet adapter with an RJ-45 connector

- Some models only: Integrated ESS 1938 audio controller with headphone, line out, and microphone connectors and joystick/MIDI connector

Connector Panel

Connectors for features that are integrated into the system board can be identified by a symbol directly below the connector. Connectors provided by an adapter might not have an identifying symbol.

For pinout details on connectors, see Appendix A, "Connector Pin Assignments" on page 28.
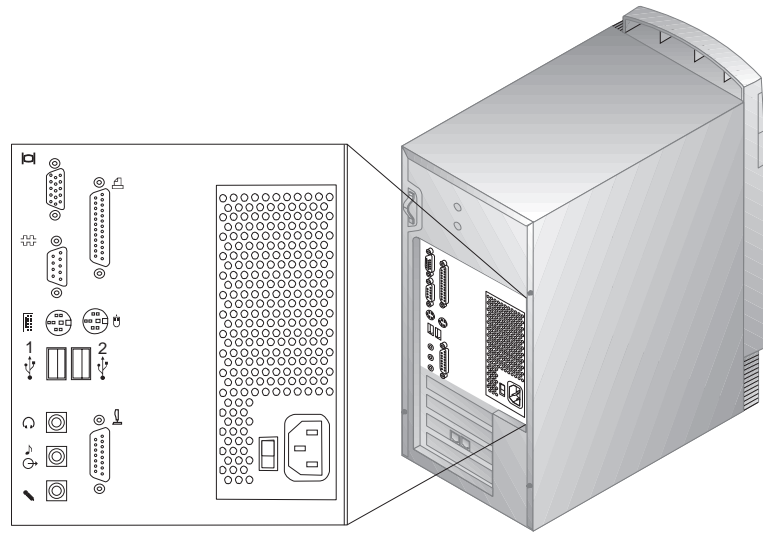
Chapter 3. Physical Specifications

This section lists the physical specifications for the PC 300GL Types 6267, 6277, and 6287. The PC 300GL has four expansion slots and four drive bays.

Notes:

- The maximum altitude for the PC 300GL is 2133.6 m (7000 ft.). This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.

- The PC 300GL computers comply with FCC Class B; however, computers with ethernet LAN connections comply with FCC Class A.

PC 300GL

Dimensions

- Height: 356 mm (14.00 in.)
- Width: 194 mm (7.625 in.)
- Depth: 381 mm (15.00 in.)

Weight

- Minimum configuration as shipped: 8.28 kg (18.25 lb)
- Maximum configuration as shipped: 10.2 kg (22.5 lb)

Environment

- Air temperature:
  - System on: 10° to 37°C (50° to 90°F) at altitude 0-914 m (3000 ft); 10° to 32 °C (50° to 90°F) at altitude 915 m (3001 ft) to 2133 m (7000ft)
  - System off: 10° to 43°C (50° to 110°F)
- Humidity:
  - System on: 8% to 80%
  - System off: 8% to 80%
- Maximum altitude: 2134 m (7000 ft)

Electrical Input

- Sine-wave input (50 to 60 Hz) is required
- Input voltage/current:
  - Low range:
    - Minimum: 100 V AC
    - Maximum: 127 V AC
    - Current rating: 4.0 amps
    - Voltage switch setting: 115 or 115 V
  - High range:
    - Minimum: 200 V AC
    - Maximum: 240 V AC
    - Voltage switch setting: 230 or 230 V
    - Current rating: 2.0 amps
  - Input kilovolt-amperes (kVA) (approximately):
  - Maximum configuration: 0.10 kVA

  Note: Power consumption and heat output vary depending on the number and type of optional features installed and the power-management optional features in use.

Heat Output

- Approximate heat output in British thermal units (Btu) per hour:
  - Minimum configuration: 245 Btu/hr (70 watts)
  - Maximum configuration: 725 Btu/hr (207 watts)

Airflow

- Approximately 0.56 cubic meters per minute (20 cubic feet per minute)

Acoustical Noise-Emission Values

- Average sound-pressure levels:
  - At operator position:
    - 38 dBA idle
    - 43 dBA operating
  - At bystander position–1 meter (3.3 ft):
    - 33 dBA idle
    - 37 dBA operating
- Declared (upper limit) sound power levels:
  - 4.3 bels idle
  - 5.0 bels operating

  Note: These levels were measured in controlled acoustical environments according to procedures specified by the American National Standards Institute (ANSI) S12.10 and ISO 7779, and are reported in accordance with ISO 9296. Actual sound-pressure levels in your location might exceed the average values stated because of room reflections and other nearby noise sources. The declared sound power levels indicate an upper limit, below which a large number of computers will operate.

Note: PC 300GL computers do not support IDE expansion adapters or the IBM PCMCIA adapter for PCI.

Cabling Requirements for Wake on LAN Adapters

The PC 300GL has a 3-pin header on the system board that provides the AUX5 and wakeup signal connections. Newer Wake on LAN adapters have a single 3-pin header that connects to a 3-pin header on the system board. Some Wake on LAN adapters have two headers: a 3-pin, right-angle header for providing AUX5 (Auxiliary 5 volts), and a 2-pin straight header for connecting the wakeup signal to the system board. These Wake on LAN adapter options will provide a Y-cable that has the 3-pin system board connector on one end and splits into the 3-pin and 2-pin connectors required to interface the card.

Chapter 4. Power Supply

The power supply requirements are supplied by 145-watt PC 300GL power supply. The power supply provides 3.3-volt power for the Pentium microprocessor and core chip set and 5-volt power for ISA and PCI adapters. Also included is an auxiliary 5-volt (AUX 5) supply to provide power to power management circuitry and a Wake on LAN adapter. The power supply converts the AC input voltage into four DC output voltages and provides power for the following:

- System board
- Adapters
- Internal drives
- Keyboard and auxiliary devices
- USB devices

A logic signal on the power connector controls the power supply; the front panel switch is not directly connected to the power supply.

The power supply connects to the system board with a 2 x 10 connector.

Power Input

The following figure shows the input power specifications. The power supply has a manual switch to select the correct input voltage.

Figure 12. Power Input Requirements	
Specification	**Measurements**
Input voltage, low range	100 (min) to 127 (max) V AC
Input voltage, high range	200 (min) to 240 (max) V AC
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz

Power Output

The power supply outputs shown in the following figures include the current supply capability of all the connectors, including system board, DASD, PCI, and auxiliary outputs.

Figure 13. Power Output (145 Watt)			
Output Voltage	**Regulation**	**Minimum Current**	**Maximum Current**
+5 volts	+5% to −5%	1.5 A	18.0 A
+12 volts	+5% to −5%	0.02 A	4.2 A
−12 volts	+10% to −10%	0.0 A	0.4 A
+3.3 volts	+5% to −5%	0.0 A	10.0 A
+5 volt (auxiliary)	+5% to −5%	0.0 A	0.720 A

The total combined 3.3 V and 5 V power should not exceed 100 watts.

Component Outputs

The power supply provides separate voltage sources for the system board and internal storage devices. The following figures show the approximate power that is provided for specific system components. Many components draw less current than the maximum shown.

Figure 14. System Board		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+3.3 V DC	3000 mA	+5.0% to −5.0%
+5.0 V DC	4000 mA	+5.0% to −4.0%
+12.0 V DC	25.0 mA	+5.0% to −5.0%
−12.0 V DC	25.0 mA	+10.0% to −9.0%

Figure 15. Keyboard Port		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V DC	275 mA	+5.0% to −4.0%

Figure 16. Auxiliary Device Port		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V DC	300 mA	+5.0% to −4.0%

Figure 17. ISA-Bus Adapters (Per Slot)		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V DC	2000 mA	+5.0% to −4.0%
−5.0 V DC	200 mA	+5.0% to −5.0%
+12.0 V DC	1500 mA	+5.0% to −5.0%
−12.0 V DC	300 mA	+10.0% to −9.0%

Figure 18. PCI-Bus Adapters (Per Slot) either/or		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V DC	2000 mA	+5.0% to −4.0%
+3.3 V DC	3030 mA	+5.0% to −4.0%

Note: For each PCI or ISA connector, the maximum power consumption is rated at 10 watts for +5 V DC and +3.3 V DC combined. Typical power budget assumptions use 7.5 watts per adapter. If maximum power is used, then the overall system configuration will be limited in performance.

Figure 19. USB Port		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V DC	500 mA	+5.0% to −4.0%

Figure 20. Internal DASD		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V DC	1400 mA	+5.0% to –5.0%
+12.0 V DC	1500 mA at startup, 400 mA when active	+5.0% to –5.0%

Figure 21. Video Port Pin 9		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V DC	1100mA	+5.0% to – 5.0%

Note: Some adapters and hard disk drives draw more current than the recommended limits. These adapters and drives can be installed in the system; however, the power supply will shut down if the total power used exceeds the maximum power that is available.

Output Protection

The power supply protects against output overcurrent, overvoltage, and short circuits. See the power supply specifications on the previous pages for details.

A short circuit that is placed on any DC output (between outputs or between an output and DC return) latches all DC outputs into a shutdown state, with no damage to the power supply. If this shutdown state occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

If an overvoltage fault occurs (in the power supply), the power supply latches all DC outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Connector Description

The power supply for the PC 300GL has four, 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in "Component Outputs" on page 19. For connector pin assignments, see Appendix A, "Connector Pin Assignments" on page 28.

Chapter 5. System Software

This section briefly describes some of the system software included with the computer.

BIOS

The computer uses the IBM basic input/output system (BIOS), which is stored in flash electrically erasable programmable read-only memory (EEPROM). Some features of the BIOS are:

- PCI support according to PCI BIOS Specification 2.2
- Microsoft's PCI IRQ Routing Table
- Plug and Play support according to Plug and Play BIOS Specification 1.1a
- Advanced Power Management (APM) support according to APM BIOS Interface Specification 1.2
- Wake on LAN support
- Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP)
- Startable CD-ROM support
- Flash-over-LAN support
- Alternate Startup Sequence
- IBM Look and Feel – Screen arrangements, etc.
- ACPI (Advanced Configuration and Power Interfaces)
- IDE Logical Block Addressing (LBA support)
- LSA 2.0 support
- Bootable CD ROM support
- LS120 support
- DM BIOS 2.1 (DMI 2.0 compliant)
- PC98 compliant

Plug and Play

Support for Plug and Play conforms to the following:

- Plug and Play BIOS Specification 1.1a and 1.0
- Plug and Play BIOS Extension Design Guide 1.0
- Plug and Play BIOS Specification, Errata, and Clarifications 1.0
- Guide to Integrating the Plug and Play BIOS Extensions with system BIOS 1.2
- Plug and Play Kit for DOS and Windows

POST

IBM power-on self-test (POST) code is used. Also, initialization code is included for the on-board system devices and controllers.

POST error codes include text messages for determining the cause of an error. For more information, see Appendix D, "Error Codes" on page 45.

Configuration/Setup Utility Program

The Configuration/Setup Utility program provides menus for selecting options for devices, I/O ports, date and time, system security, start options, advanced setup, ISA legacy resources, and power management.

More information on using the Configuration/Setup Utility program is provided in *PC 300GL User Guide*.

Advanced Power Management (APM)

The PC 300GL computers come with built-in energy-saving capabilities. Advanced Power Management (APM) is a feature that reduces the power consumption of systems when they are not being used. When enabled, APM initiates reduced-power modes for the monitor, microprocessor, and hard disk drive after a specified period of inactivity.

The BIOS supports APM 1.2. This enables the system to enter a power-managed state, which reduces the power drawn from the AC wall outlet. Advanced Power Management is enabled through the Configuration/Setup Utility Program and is controlled by the individual operating system.

For more information on APM, see *PC 300GL User Guide* and *Understanding Your Personal Computer*.

Advanced Configuration and Power Interface (ACPI)

When Automatic Configuration and Power Interface (ACPI) BIOS mode is enabled, the operating system is allowed to control the power management features of your computer and the settings for APM BIOS mode are ignored. Not all operating systems support ACPI BIOS mode. Refer to your operating system documentation to determine if ACPI is supported.

Flash Update Utility Program

The flash update utility program is a stand-alone program to support flash updates. This utility program updates the BIOS code in flash and the Machine Readable Information (MRI) to different languages.

The flash update utility program is available on a 3.5 inch diskette.

Diagnostic Program

The diagnostic program that comes with PC 300PL and PC 300GL computers is provided as a startable *IBM Enhanced Diagnostic* diskette image on the hard disk and on the *Software Selection* CD. It runs independently of the operating system. The user interface for running the diagnostics and utilities is provided by WaterGate Software's PC-Doctor. It can also be downloaded from the following World Wide Web page: http://www.pc.ibm.com/support/desktop/desktop_support.html. For more information on this diagnostic program, see *PC 300GL User Guide*.

PC 300GL computers use the PC Doctor programs and IBM Enhanced Diagnostics. See *About Your Software* and *PC 300GL User Guide* for more information.

Universal Management Agent

The Universal Management Agent (UMA) is a collection of tools designed to use the hardware features on your computer to make managing your system over a network easier. The Universal Management Agent Browser launches and manages each tool from a central interface using ActiveX controls in an Internet or Intranet environment. You can use the tools locally on the computer where UMA is installed or remotely by using the Internet or Intranet to access the computer where UMA is installed to remotely manage and monitor your computer.

UMA can also integrate into a number of server-based management programs such as IBM Netfinity Manager; enterprise-management systems such as Tivoli TME 10, Tivoli NetView, and Microsoft System Management Server (SMS); and Microsoft Management Console (MMC). Additionally, you can configure the UMA program to forward simple network management protocol (SNMP) traps to workgroup- and enterprise-level network management applications such as Microsoft SMS, Tivoli NetView, and Computer Associates Unicenter.

For more information on UMA and its components, see the UMA web page at

`http://www.pc.ibm.com/us/cdt/uma.html`

Chapter 6. System Compatibility

This chapter discusses some of the hardware, software, and BIOS compatibility issues for the computer. Refer to *Compatibility Report* for a list of compatible hardware and software options.

Hardware Compatibility

This section discusses hardware, software, and BIOS compatibility issues that must be considered when designing application programs.

Many of the interfaces are the same as those used by the IBM Personal Computer AT. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces are compatible with the following interfaces:

- Intel 8259 interrupt controllers (edge-triggered mode)
- National Semiconductor NS16450 and NS16550A serial communication controllers
- Motorola MC146818 Time of Day Clock command and status (CMOS reorganized)
- Intel 8254 timer, driven from a 1.193 MHz clock (channels 0, 1, and 2)
- Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions; the Mode register is partially supported
- Intel 8272 or 82077 diskette drive controllers
- Intel 8042 keyboard controller at addresses hex 0060 and hex 0064
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes
- Parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode

Use the above information to develop application programs. Whenever possible, use the BIOS as an interface to hardware to provide maximum compatibility and portability of applications among systems.

Hardware Interrupts

Hardware interrupts are level-sensitive for PCI interrupts and edge-sensitive for ISA interrupts. The interrupt controller clears its in-service register bit when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI command is sent regardless of whether the incoming interrupt request to the controller is active or inactive.

The interrupt-in-progress latch is readable at an I/O-address bit position. This latch is read during the interrupt service routine and might be reset by the read operation or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

With level-sensitive interrupts, the interrupt controller requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler:

1. Clears the interrupt
2. Waits one I/O delay

3. Sends the EOI

4. Waits one I/O delay

5. Enables the interrupt through the Set Interrupt Enable Flag command

Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt hex 0A. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.

2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.

3. When the interrupt occurs, the system microprocessor passes control to the IRQ9 (interrupt hex 71) interrupt handler.

4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt hex 0A) interrupt handler.

5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

Diskette Drives and Controller

The following figures show the reading, writing, and formatting capabilities of each type of diskette drive.

Figure 22. 5.25-Inch Diskette Drive Reading, Writing, and Formatting Capabilities			
Diskette Drive Type	**250/500 KB Mode**	**300/500 KB Mode**	**1 MB Mode**
Single sided (48 Tracks Per Inch (TPI))	RWF	—	—
Double sided (48 TPI)	RWF	RWF	—
High capacity (1.2 MB)	RWF	RWF	RWF

Figure 23. 3.5-Inch Diskette Drive Reading, Writing, and Formatting Capabilities		
Diskette Drive Type	**720 KB Mode**	**1.44 MB Mode**
1.44 MB drive	RWF	RWF
2.88 MB drive	RWF	RWF

Notes:

1. Do not use either a 250/500 KB or 300/500 KB diskette drive for 5.25-inch diskettes that are designed for the 1.2MB mode.
2. Low-density 5.25-inch diskettes that are written to or formatted by a high-capacity 1.2 MB diskette drive can be reliably read only by another 1.2 MB diskette drive.

Copy Protection

The following methods of copy protection might not work in systems using the 3.5-inch 1.44 MB diskette drive.

- Bypassing BIOS routines

  - Data transfer rate: BIOS selects the proper data transfer rate for the media being used.

  - Diskette parameter table: Copy protection, which creates its own diskette parameter table, might not work in these drives.

Chapter 6. System Compatibility

- Diskette drive controls

  - Rotational speed: The time between two events in a diskette drive is a function of the controller.

  - Access time: Diskette BIOS routines must set the track-to-track access time for the different types of media that are used in the drives.

  - 'Diskette change' signal: Copy protection might not be able to reset this signal.

- Write-current control: Copy protection that uses write-current control does not work, because the controller selects the proper write current for the media that is being used.

Hard Disk Drives and Controller

Reading from and writing to the hard disk is initiated in the same way as in IBM Personal Computer products; however, new functions are supported.

Software Compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02Fx or 06Fx, where x is the interrupt level) does not create interference.

Software Interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-Sensitive Programs

Programs can select machine specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return System Configuration Parameters function (AH)=C0H).

Appendix A. Connector Pin Assignments

The following figures show the pin assignments for various system board connectors.

AGP Monitor Port Connector
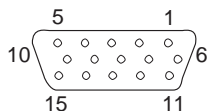
Figure 24. AGP Monitor Port Connector Pin Assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Red	O	2	Green	O
3	Blue	O	4	Monitor ID 2 - Not used	I
5	Ground	NA	6	Red ground	NA
7	Green ground	NA	8	Blue ground	NA
9	+5 V, used by DDC2B	NA	10	Ground	NA
11	Monitor ID 0 - Not used	I	12	DDC2B serial data	I/O
13	Horizontal sync	O	14	Vertical sync	O
15	DDC2B clock	I/O			

Memory Connectors
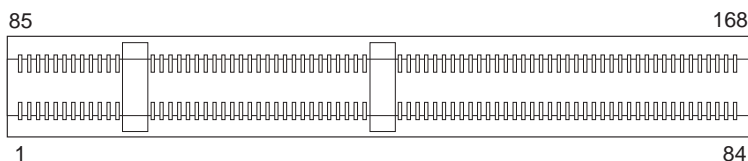
Figure 25 (Page 1 of 3). System Memory Connector Pin Assignments					
Pin	**x64 Non-Parity**	**x72 ECC**	**Pin**	**x64 Non-Parity**	**x72 ECC**
1	VSS	VSS	85	VSS	VSS
2	DQ0	DQ0	86	DQ32	DQ32
3	DQ1	DQ1	87	DQ33	DQ33
4	DQ2	DQ2	88	DQ34	DQ34
5	DQ3	DQ3	89	DQ35	DQ35
6	VCC	VCC	90	VCC	VCC
7	DQ4	DQ4	91	DQ36	DQ36
8	DQ5	DQ5	92	DQ37	DQ37
9	DQ6	DQ6	93	DQ38	DQ38
10	DQ7	DQ7	94	DQ39	DQ39
11	DQ8	DQ8	95	DQ40	DQ40
12	VSS	VSS	96	VSS	VSS

| Pin	x64 Non-Parity	x72 ECC	Pin	x64 Non-Parity	x72 ECC
13	DQ9	DQ9	97	DQ41	DQ41
14	DQ10	DQ10	98	DQ42	DQ42
15	DQ11	DQ11	99	DQ43	DQ43
16	DQ12	DQ12	100	DQ44	DQ44
17	DQ13	DQ13	101	DQ45	DQ45
18	VCC	VCC	102	VCC	VCC
19	DQ14	DQ14	103	DQ46	DQ46
20	DQ15	DQ15	104	DQ47	DQ47
21	NC	CB0	105	NC	CB4
22	NC	CB1	106	NC	CB5
23	VSS	VSS	107	VSS	VSS
24	NC	NC	108	NC	NC
25	NC	NC	109	NC	NC
26	VCC	VCC	110	VCC	VCC
27	/WE	/WE0	111	/CAS	/CAS
28	DQMB0	DQMB0	112	DQMB4	DQMB4
29	DQMB1	DQMB1	113	DQMB5	DQMB5
30	/S0	/S0	114	NC	/S1
31	DU	NC	115	/RAS	/RAS
32	VSS	VSS	116	VSS	VSS
33	A0	A0	117	A1	A1
34	A2	A2	118	A3	A3
35	A4	A4	119	A5	A5
36	A6	A6	120	A7	A7
37	A8	A8	121	A9	A9
38	A10/AP	A10/AP	122	BA0	BA0
39	NC	BA1	123	NC	A11
40	VCC	VCC	124	VCC	VCC
41	VCC	VCC	125	CK1	CK1
42	CK0	CK0	126	A12	A12
43	VSS	VSS	127	VSS	VSS
44	DU	NC	128	CKE0	CKE0
45	/S2	/S2	129	NC	/S3
46	DQMB2	DQMB2	130	DQMB6	DQMB6
47	DQMB3	DQMB3	131	DQMB7	DQMB7
48	DU	NC	132	A13	A13
49	VCC	VCC	133	VCC	VCC
50	NC	NC	134	NC	NC
51	NC	NC	135	NC	NC
52	NC	CB2	136	NC	CB6
53	NC	CB3	137	NC	CB7
54	VSS	VSS	138	VSS	VSS
55	DQ16	DQ16	139	DQ48	DQ48

Figure 25 (Page 2 of 3). System Memory Connector Pin Assignments

Appendix A. Connector Pin Assignments

Pin	x64 Non-Parity	x72 ECC	Pin	x64 Non-Parity	x72 ECC
		Figure 25 (Page 3 of 3). System Memory Connector Pin Assignments			
56	DQ17	DQ17	140	DQ49	DQ49
57	DQ18	DQ18	141	DQ50	DQ50
58	DQ19	DQ19	142	DQ51	DQ51
59	VCC	VCC	143	VCC	VCC
60	DQ20	DQ20	144	DQ52	DQ52
61	NC	NC	145	NC	NC
62	NC	NC	146	NC	NC
63	NC	CKE1	147	NC	NC
64	VSS	VSS	148	VSS	VSS
65	DQ21	DQ21	149	DQ53	DQ53
66	DQ22	DQ22	150	DQ54	DQ54
67	DQ23	DQ23	151	DQ55	DQ55
68	VSS	VSS	152	VSS	VSS
69	DQ24	DQ24	153	DQ56	DQ56
70	DQ25	DQ25	154	DQ57	DQ57
71	DQ26	DQ26	155	DQ58	DQ58
72	DQ27	DQ27	156	DQ59	DQ59
73	VCC	VCC	157	VCC	VCC
74	DQ28	DQ28	158	DQ60	DQ60
75	DQ29	DQ29	159	DQ61	DQ61
76	DQ30	DQ30	160	DQ62	DQ62
77	DQ31	DQ31	161	DQ63	DQ63
78	VSS	VSS	162	VSS	VSS
79	CK2	CK2	163	CK3	CK3
80	NC	NC	164	NC	NC
81	NC	NC	165	SA0	SA0
82	SDA	SDA	166	SA1	SA1
83	SCL	SCL	167	SA2	SA2
84	VCC	VCC	168	VCC	VCC

Pin	Signal Name	I/O	Pin	Signal Name	I/O
		Figure 26 (Page 1 of 3). System Memory Connector Pin Input/Output			
1	GND	N/A	85	GND	N/A
2	MD0	I/O	86	MD32	I/O
3	MD1	I/O	87	MD33	I/O
4	MD2	I/O	88	MD34	I/O
5	MD3	I/O	89	MD35	I/O
6	VDD	I/O	90	VDD	N/A
7	MD4	I/O	91	MD36	N/A
8	MD5	I/O	92	MD37	I/O
9	MD6	I/O	93	MD38	I/O
10	MD7	I/O	94	MD39	I/O
11	MD8 (PAR0)	I/O	95	MD40	I/O

Pin	Signal Name	I/O	Pin	Signal Name	I/O
\ _Figure 26 (Page 2 of 3). System Memory Connector Pin Input/Output_					
12	GND	N/A	96	GND	N/A
13	MD9	I/O	97	MD41	I/O
14	MD10	I/O	98	MD42	I/O
15	MD11	I/O	99	MD43	I/O
16	MD12	I/O	100	MD44	I/O
17	MD13	I/O	101	MD45	I/O
18	VDD	N/A	102	VDD	N/A
19	MD14	I/O	103	MD46	I/O
20	MD15	I/O	104	MD47	I/O
21	NC	I/O	105	NC	I/O
22	NC	I/O	106	NC	I/O
23	GND	I/O	107	GND	N/A
24	NC	N/A	108	NC	N/A
25	NC	N/A	109	NC	N/A
26	VDD	N/A	110	VDD	N/A
27	WE#	I	111	CAS#	N/A
28	DQMB0#	I	112	DQMB4#	I
29	DQMB1#	I	113	DQMB4#	I
30	S0#	I	114	S1#	I
31	OE0#	i	115	RAS#	N/A
32	GND	N/A	116	GND	N/A
33	A0	I	117	A1	I
34	A2	I	118	A3	I
35	A4	I	119	A5	I
36	A6	I	120	A7	I
37	A8	I	121	A9	I
38	A10/AP	I	122	A11	I
39	NC	BA1	123	NC	A11
40	VDD	N/A	124	VDD	N/A
41	NC	N/A	125	CK1	N/A
42	CK0	N/A	126	A14	O
43	GND	N/A	127	GND	N/A
44	OE2#	I	128	CKE0	N/A
45	S2#	I	129	S3#	I
46	DQMB2#	I	130	DQMB6#	I
47	DQMB3#	I	131	DQMB7#	I
48	WE2#	I	132	A15	I
49	VDD	N/A	133	VDD	N/A
50	NC	N/A	134	NC	N/A
51	NC	N/A	135	NC	N/A
52	NC	I/O	136	NC	I/O
53	NC	I/O	137	NC	I/O
54	GND	NA	138	GND	N/A

Pin	Signal Name	I/O	Pin	Signal Name	I/O
Figure 26 (Page 3 of 3). System Memory Connector Pin Input/Output					
55	MD16	I/O	139	MD48	I/O
56	MD17	I/O	140	MD49	I/O
57	MD18	I/O	141	MD50	I/O
58	MD19	I/O	142	MD51	I/O
59	VDD	N/A	143	VDD	N/A
60	MD20	I/O	144	MD52	I/O
61	CKE1	N/A	145	NC	N/A
62	VREF	N/A	146	VREF	N/A
63	(CKE1)*	N/A	147	NC	N/A
64	GND	N/A	148	GND	N/A
65	MD21	I/O	149	MD53	I/O
66	MD22	I/O	150	MD54	I/O
67	MD23	I/O	151	MD55	I/O
68	GND	N/A	152	GND	N/A
69	MD24	I/O	153	MD56	I/O
70	MD25	I/O	154	MD57	I/O
71	MD26	I/O	155	MD58	I/O
72	MD27	I/O	156	MD59	I/O
73	VDD	N/A	157	VDD	N/A
74	MD28	I/O	158	MD60	I/O
75	MD29	I/O	159	MD61	I/O
76	MD30	I/O	160	MD62	I/O
77	MD31	I/O	161	MD63	I/O
78	GND	N/A	162	GND	N/A
79	CK2	O	163	CK3	O
80	NC	N/A	164	NC	N/A
81	NC	O	165	SA0	O
82	SDA	O	166	SA1	O
83	SCL	O	167	SA0	O
84	VDD	N/A	168	VDD	N/A

ISA Connectors

A1   A31   C1   C18

B1   B31   D1   D18
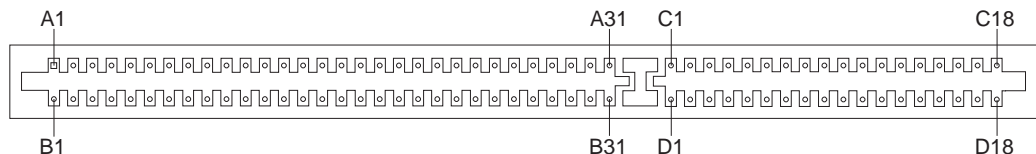
Pin	Signal	I/O	Pin	Signal	I/O
Figure 27 (Page 1 of 3). ISA Connector Pin Assignments					
B1	Ground	NA	A1	IOCHCK#	I
B2	RESET DRV	O	A2	SD7	I/O

Pin	Signal	I/O	Pin	Signal	I/O
B3	+5 V DC	NA	A3	SD6	I/O
B4	IRQ2	I	A4	SD5	I/O
B5	-5 V DC	NA	A5	SD4	I/O
B6	DRQ2	I	A6	SD3	I/O
B7	-12 V DC	NA	A7	SD2	I/O
B8	OWS#	I	A8	SD1	I/O
B9	+12 V DC	NA	A9	SD0	I/O
B10	Ground	NA	A10	IOCHRDY	I
B11	SMEMW#	O	A11	AEN	O
B12	SMEMR#	O	A12	SA19	I/O
B13	IOW#	I/O	A13	SA18	I/O
B14	IOR#	I/O	A14	SA17	I/O
B15	DACK3#	O	A15	SA16	I/O
B16	DRQ3	I	A16	SA15	I/O
B17	DACK1#	O	A17	SA14	I/O
B18	DRQ1	I	A18	SA13	I/O
B19	REFRESH#	I/O	A19	SA12	I/O
B20	CLK	O	A20	SA11	I/O
B21	IRQ7	I	A21	SA10	I/O
B22	IRQ6	I	A22	SA9	I/O
B23	IRQ5	I	A23	SA8	I/O
B24	IRQ4	I	A24	SA7	I/O
B25	IRQ3	I	A25	SA6	I/O
B26	DACK2#	O	A26	SA5	I/O
B27	TC	O	A27	SA4	I/O
B28	BALE	O	A28	SA3	I/O
B29	+5 V DC	NA	A29	SA2	I/O
B30	OSC	O	A30	SA1	I/O
B31	Ground	NA	A31	SA0	I/O
D1	MEMCS16#	I	C1	SBHE#	I/O
D2	IOCS16#	I	C2	LA23	I/O
D3	IRQ10	I	C3	LA22	I/O
D4	IRQ11	I	C4	LA21	I/O
D5	IRQ12	I	C5	LA20	I/O
D6	IRQ15	I	C6	LA19	I/O
D7	IRQ14	I	C7	LA18	I/O
D8	DACK0#	O	C8	LA17	I/O
D9	DRQ0	I	C9	MEMR#	I/O
D10	DACK5#	O	C10	MEMW#	I/O
D11	DRQ5	I	C11	SD8	I/O
D12	DACK6#	O	C12	SD9	I/O
D13	DRQ6	I	C13	SD10	I/O
D14	DACK7#	O	C14	SD11	I/O

Figure 27 (Page 2 of 3). ISA Connector Pin Assignments

Appendix A. Connector Pin Assignments

| Figure 27 (Page 3 of 3). ISA Connector Pin Assignments					
Pin	Signal	I/O	Pin	Signal	I/O
D15	DRQ7	I	C15	SD12	I/O
D16	+5 V DC	NA	C16	SD13	I/O
D17	MASTER#	I	C17	SD14	I/O
D18	Ground	NA	C18	SD15	I/O

PCI Connectors
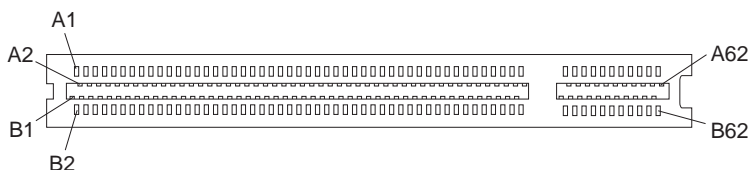
Figure 28. PCI Bus Connector

Figure 29 (Page 1 of 2). PCI Connector Pin Assignments					
Pin	Signal	I/O	Pin	Signal	I/O
A1	TRST#	O	B1	−12 V DC	NA
A2	+12 V DC	NA	B2	TCK	O
A3	TMS	O	B3	Ground	NA
A4	TDI	O	B4	TDO	I
A5	+5 V DC	NA	B5	+5 V DC	NA
A6	INTA#	I	B6	+5 V DC	NA
A7	INTC#	I	B7	INTB#	I
A8	+5 V DC	NA	B8	INTD#	I
A9	Reserved	NA	B9	PRSNT1#	I
A10	+5 V DC (I/O)	NA	B10	Reserved	NA
A11	Reserved	NA	B11	PRSNT2	I
A12	Ground	NA	B12	Ground	NA
A13	Ground	NA	B13	Ground	NA
A14	Reserved	NA	B14	Reserved	NA
A15	RST#	O	B15	Ground	NA
A16	+5 V DC (I/O)	NA	B16	CLK	O
A17	GNT#	O	B17	Ground	NA
A18	Ground	NA	B18	REQ#	I
A19	PCIPME	NA	B19	+5 V DC (I/O)	NA
A20	Address/Data 30	I/O	B20	Address/Data 31	I/O
A21	+3.3 V DC	NA	B21	Address/Data 29	I/O
A22	Address/Data 28	I/O	B22	Ground	NA
A23	Address/Data 26	I/O	B23	Address/Data 27	I/O
A24	Ground	I/O	B24	Address/Data 25	NA
A25	Address/Data 24	I/O	B25	+3.3 V DC	NA
A26	IDSEL	O	B26	C/BE 3#	I/O
A27	+3.3 V DC	NA	B27	Address/Data 23	I/O

Pin	Signal	I/O	Pin	Signal	I/O
A28	Address/Data 22	I/O	B28	Ground	NA
A29	Address/Data 20	I/O	B29	Address/Data 21	I/O
A30	Ground	I/O	B30	Address/Data 19	NA
A31	Address/Data 18	I/O	B31	+3.3 V DC	NA
A32	Address/Data 16	I/O	B32	Address/Data 17	I/O
A33	+3.3 V DC	NA	B33	C/BE 2#	I/O
A34	FRAME#	I/O	B34	Ground	NA
A35	Ground	NA	B35	IRDY#	I/O
A36	TRDY#	I/O	B36	+3.3 V DC	NA
A37	Ground	NA	B37	DEVSEL#	I/O
A38	STOP#	I/O	B38	Ground	NA
A39	+3.3 V DC	NA	B39	LOCK#	I/O
A40	SDONE	I/O	B40	PERR#	I/O
A41	SBO#	I/O	B41	+3.3 V DC	NA
A42	Ground	NA	B42	SERR#	I/O
A43	+3.3 V DC	NA	B43	+3.3 V DC	NA
A44	C/BE(1)#	I/O	B44	C/BE 1#	I/O
A45	Address/Data 14	I/O	B45	Address/Data 14	I/O
A46	Ground	NA	B46	Ground	NA
A47	Address/Data 12	I/O	B47	Address/Data 12	I/O
A48	Address/Data 10	I/O	B48	Address/Data 10	I/O
A49	Ground	NA	B49	Ground	NA
A50	Key	NA	B50	Key	NA
A51	Key	NA	B51	Key	NA
A52	Address/Data 8	I/O	B52	Address/Data 8	I/O
A53	Address/Data 7	I/O	B53	Address/Data 7	I/O
A54	+3.3 V DC	NA	B54	+3.3 V DC	NA
A55	Address/Data 5	I/O	B55	Address/Data 5	I/O
A56	Address/Data 3	I/O	B56	Address/Data 3	I/O
A57	Ground	NA	B57	Ground	NA
A58	Address/Data 1	I/O	B58	Address/Data 1	I/O
A59	+5 V DC (I/O)	NA	B59	+5 V DC (I/O)	NA
A60	ACK64#	I/O	B60	ACK64#	I/O
A61	+5 V DC	NA	B61	+5 V DC	NA
A62	+5 V DC	NA	B62	+5 V DC	NA

Figure 29 (Page 2 of 2). PCI Connector Pin Assignments
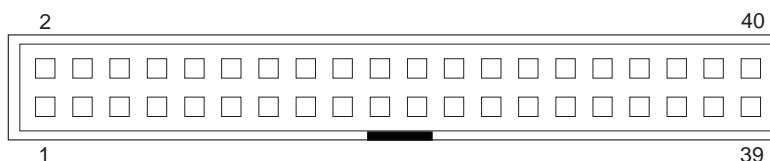
IDE Connectors

Appendix A. Connector Pin Assignments

Figure 30. IDE Connector Pin Assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	RESET	O	21	NC	NA
2	Ground	NA	22	Ground	NA
3	Data bus bit 7	I/O	23	I/O write	O
4	Data bus bit 8	I/O	24	NC	NA
5	Data bus bit 6	I/O	25	I/O read	O
6	Data bus bit 9	I/O	26	Ground	NA
7	Data bus bit 5	I/O	27	I/O channel ready	I
8	Data bus bit 10	I/O	28	ALE	O
9	Data bus bit 4	I/O	29	NC	NA
10	Data bus bit 11	I/O	30	Ground	NA
11	Data bus bit 3	I/O	31	IRQ	I
12	Data bus bit 12	I/O	32	CS16#	I
13	Data bus bit 2	I/O	33	SA1	O
14	Data bus bit 13	I/O	34	PDIAG#	I
15	Data bus bit 1	I/O	35	SA0	O
16	Data bus bit 14	I/O	36	SA2	O
17	Data bus bit 0	I/O	37	CS0#	O
18	Data bus bit 15	I/O	38	CS1	O
19	Ground	NA	39	Active#	I
20	Key (Reserved)	NA	40	Ground	NA

Diskette Drive Connector

Figure 31 (Page 1 of 2). Diskette Drive Connector Pin Assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Drive 2 installed #	I	2	High density select	O
3	Not connected	NA	4	Not connected	NA
5	Ground	NA	6	Data rate 0	NA
7	Ground	NA	8	Index#	I
9	Reserved	NA	10	Motor enable 0#	O
11	Ground	NA	12	Drive select 1#	O
13	Ground	NA	14	Drive select 0#	O
15	Ground	NA	16	Motor enable 1#	O
17	MSEN1	I	18	Direction in#	O
19	Ground	NA	20	Step#	O
21	Ground	NA	22	Write data#	O
23	Ground	NA	24	Write enable#	O
25	Ground	NA	26	Track0#	I
27	MSEN0	I	28	Write protect#	I
29	Ground	NA	30	Read data#	I
31	Ground	NA	32	Head 1 select#	O

Figure 31 (Page 2 of 2). Diskette Drive Connector Pin Assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
33	Data rate 1	NA	34	Diskette change#	I

Power Supply Connector

Figure 32. Power Supply Connector Pin Assignments			
Pin	**Signal Name**	**Pin**	**Signal Name**
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	−12 V
3	Ground	13	Ground
4	+5 V	14	ON/OFF
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWR GOOD	18	Reserved
9	+5 V AUX	19	+5 V
10	+12 V	20	+5 V

Modem/Ring Wakeup and Wake on LAN Connectors

Figure 33. J13 Modem/Ring Wakeup Connector Pin Assignments	
Pin	**Description**
1	Internal Modem Wake Up on Ring
2	Ground

Figure 34. J22 Wake on LAN Connector Pin Assignments	
Pin	**Description**
1	+5v AUX
2	Ground
3	Internal Wake on LAN

USB Port Connectors
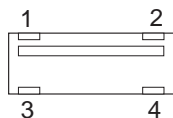
Figure 35 (Page 1 of 2). USB Port Connector Pin Assignments	
Pin	**Signal**
1	VCC

Figure 35 (Page 2 of 2). USB Port Connector Pin Assignments	
Pin	**Signal**
2	-Data
3	+Data
4	Ground

# Mouse and Keyboard Port Connectors
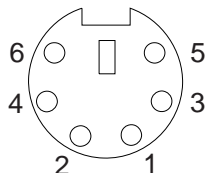
| Figure 36. Mouse Port Connector Pin Assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Data	I/O	2	Reserved	I/O
3	Ground	NA	4	+5 V DC	NA
5	Clock	I/O	6	Reserved	NA

Figure 37. Keyboard Port Connector Pin Assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Keyboard Data	I/O	2	Mouse Data	I/O
3	Ground	NA	4	+5 V DC	NA
5	Keyboard Clock	I/O	6	Mouse Clock	I/O

Serial Port Connector
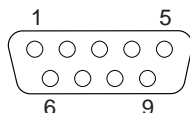
Figure 38. Serial Port Connector Pin Assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Data carrier detect	I	2	Receive data#	I
3	Transmit data#	O	4	Data terminal read	O
5	Ground	NA	6	Data set ready	I
7	Request to send	O	8	Clear to send	I
9	Ring indicator	I			

Parallel Port Connector
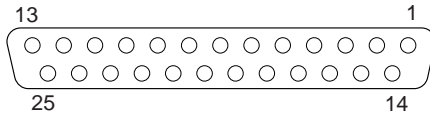
Figure 39. Parallel Port Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	STROBE#	I/O	2	Data bit 0	I/O
3	Data bit 1	I/O	4	Data bit 2	I/O
5	Data bit 3	I/O	6	Data bit 4	I/O
7	Data bit 5	I/O	8	Data bit 6	I/O
9	Data bit 7	I/O	10	ACK#	I
11	BUSY	I	12	PE	I
13	SLCT	I	14	AUTO FD XT#	O
15	ERROR#	I	16	INIT#	O
17	SLCT IN#	O	18	Ground	NA
19	Ground	NA	20	Ground	NA
21	Ground	NA	22	Ground	NA
23	Ground	NA	24	Ground	NA
25	Ground	NA			

Joystick/MIDI Connector

Figure 40. Joystick/MIDI Connector Pin Assignments

Pin	Signal	I/O
1	+5 V	N/A
2	Joystick A, Button 1	I
3	Joystick A, X Position	I
4	Ground	N/A
5	Ground	N/A
6	Joystick A, Y Position	I
7	Joystick A, Button 2	I
8	+5 V	N/A
9	+5 V	N/A
10	Joystick B, Button 1	I
11	Joystick B, X Position	I
12	MIDI Out	O
13	Joystick B, Y Position	I
14	Joystick B, Button 2	I
15	MIDI In	I

Appendix B. System Address Maps

System Memory Map

The first 640 KB of system board RAM is mapped starting at address hex 0000000. A 256 byte area and a 1 KB area of this RAM are reserved for BIOS data areas. Memory can be mapped differently if POST detects an error.

Figure 41. System Memory Map			
Address Range (decimal)	**Address Range (hex)**	**Size**	**Description**
0 K – 512 K	00000–7FFFF	512 KB	Conventional
512 K – 639 K	80000–9FBFF	127 KB	Extended conventional
639 K – 640 K	9FC00–9FFFF	1 KB	Extended BIOS data
640 K – 767 K	A0000–BFFFF	128 KB	S3 Video RAM
768 K – 800 K	C0000 to C7FFF	32 KB	S3 Video ROM BIOS (shadowed)
800 K – 896 K	C8000–DFFFF	96 KB	PCI/ISA space, available to adapter ROMs
896 K – 1 MB	E0000–FFFFF	128 KB	System ROM BIOS(ISA Bus, main memory shadowed)
1 MB – 16 MB	100000–FFFFFF	15 MB	PCI/ISA Space
16 MB – 4095.872 MB	1000000–FFDFFFFF	4079.8 MB	PCI Space (positive decode)
FFFE0000 –FFFFFFFF	128 KB	System ROM BIOS (ISA Bus)	

Input/Output Address Map

The following figure lists resource assignments for the I/O address map. Any addresses that are not shown are reserved.

Figure 42 (Page 1 of 3). I/O Address Map		
Address (Hex)	**Size**	**Description**
0000–000F	16 bytes	DMA 1
0010–001F	16 bytes	General I/O Locations — available to ISA Bus
0020–0021	2 bytes	Interrupt controller 1
0022–003F	30 bytes	General I/0 locations — available to ISA Bus
0040–0043	4 bytes	Counter/timer 1
0044–00FF	28 bytes	General I/0 locations — available to ISA Bus
0060	1 byte	Keyboard controller byte - reset IRQ
0061	1 byte	PIIX4, System port B
0064	1 byte	Keyboard controller, CMD/STAT byte
0070, bit 7	1 bit	Enable NMI
0070, bits 6:0	1 bit	Real time clock, address
0071	1 byte	Real time clock, data
0072–007F	14 bytes	General I/O locations — available to ISA bus

Figure 42 (Page 2 of 3). I/O Address Map		
Address (Hex)	**Size**	**Description**
0080	1 byte	POST checkpoint register during POST only
008F	1 byte	Refresh page register
0080–008F	16 bytes	PIIX4, DMA page registers
0090–0091	15 bytes	General I/O locations — available to ISA bus
0092	1 byte	PS/2 keyboard controller registers
0093–009F	15 bytes	General I/O locations
00A0–00A1	2 bytes	Interrupt controller 2
00A2–00BF	30 bytes	APM control
00C0–00DF	31 bytes	DMA 2
00E0–00EF	16 bytes	General I/O locations — available to ISA bus
00F0	1 byte	BX, Coprocessor Error Register
00F1–016F	127 bytes	General I/O locations — available to ISA bus
0170–0177	8 bytes	Secondary IDE channel
01F0–01F7	8 bytes	Primary IDE channel
0200–0207	8 bytes	Available
0220–0227	8 bytes	SMC 37C673, Serial port 3 or 4
0228–0277	80 bytes	General I/O locations — available to ISA bus
0278–027F	8 bytes	SMC 27C673, LPT3
0280–02E7	102 bytes	Available
02E8–02EF	8 bytes	SMC PC37C673, Serial port 3 or 4
02F8–02FF	8 bytes	COM2
0338–033F	8 bytes	SMC PC37C673, Serial port 3 or 4
0340–036F	48 bytes	Available
0370–0371.	2 bytes	SMC SIO planar Plug–n–Play index/data registers
0372–0375	4 bytes	Available
0376–0377	2 bytes	IDE channel 1 command
0378–037F	8 bytes	LPT2
0380–03B3	52 bytes	Available
03B4–03B7	4 bytes	Video
03BA	1 byte	Video
03BC–03BE	16 bytes	LPT1
03C0–03CF	16 bytes	Video
03D4–03D7	4 bytes	Video
03DA	1 byte	Video
03D0–03DF	11 bytes	Available
03E0–03E7	8 bytes	Available
03E8–03EF	8 bytes	COM3 or COM4
03F0–03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F7 (Write)	1 byte	Diskette channel 1 command
03F7, bit 7	1 bit	Diskette disk change channel
03F7, bits 6:0	7 bits	Primary IDE channel status port
03F8–03FF	8 bytes	COM1

Appendix B. System Address Maps

Figure 42 (Page 3 of 3). I/O Address Map		
Address (Hex)	**Size**	**Description**
0400–047F	128 bytes	Available
0480–048F	16 bytes	DMA channel high page registers
0490–0CF7	1912 bytes	Available
0CF8–0CFB	4 bytes	PCI Configuration address register
0CFC–0CFF	4 bytes	PCI Configuration data register
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + hex 400
0CF9	1 byte	Turbo and reset control register
0D00–FFFF	62207 bytes	Available

DMA I/O Address Map

The following figure lists resource assignments for the DMA address map. Any addresses that are not shown are reserved.

Figure 43 (Page 1 of 2). DMA I/O Address Map			
Address (Hex)	**Description**	**Bits**	**Byte Pointer**
0000	Channel 0, Memory Address register	00–15	Yes
0001	Channel 0, Transfer Count register	00–15	Yes
0002	Channel 1, Memory Address register	00–15	Yes
0003	Channel 1, Transfer Count register	00–15	Yes
0004	Channel 2, Memory Address register	00–15	Yes
0005	Channel 2, Transfer Count register	00–15	Yes
0006	Channel 3, Memory Address register	00–15	Yes
0007	Channel 3, Transfer Count register	00–15	Yes
0008	Channels 0–3, Read Status/Write Command register	00–07	
0009	Channels 0–3, Write Request register	00–02	
000A	Channels 0–3, Write Single Mask register bits	00–02	
000B	Channels 0–3, Mode register (write)	00–07	
000C	Channels 0–3, Clear byte pointer (write)	N/A	
000D	Channels 0–3, Master clear (write)/temp (read)	00–07	
000E	Channels 0–3, Clear Mask register (write)	00–03	
000F	Channels 0–3, Write All Mask register bits	00–03	
0081	Channel 2, Page Table Address register [4]	00–07	
0082	Channel 3, Page Table Address register [4]	00–07	
0083	Channel 1, Page Table Address register [4]	00–07	
0087	Channel 0, Page Table Address register [4]	00–07	
0089	Channel 6, Page Table Address register [4]	00–07	
008A	Channel 7, Page Table Address register [4]	00–07	
008B	Channel 5, Page Table Address register [4]	00–07	
008F	Channel 4, Page Table Address/Refresh register	00–07	
00C0	Channel 4, Memory Address register	00–15	Yes
00C2	Channel 4, Transfer Count register	00–15	Yes
00C4	Channel 5, Memory Address register	00–15	Yes

Address (Hex)	Description	Bits	Byte Pointer
	Figure 43 (Page 2 of 2). DMA I/O Address Map		
00C6	Channel 5, Transfer Count register	00–15	Yes
00C8	Channel 6, Memory Address register	00–15	Yes
00CA	Channel 6, Transfer Count register	00–15	Yes
00CC	Channel 7, Memory Address register	00–15	Yes
00CE	Channel 7, Transfer Count register	00–15	Yes
00D0	Channels 4–7, Read Status/Write Command register	00–07	
00D2	Channels 4–7, Write Request register	00–02	
00D4	Channels 4–7, Write Single Mask register bit	00–02	
00D6	Channels 4–7, Mode register (write)	00–07	
00D8	Channels 4–7, Clear byte pointer (write)	N/A	
00DA	Channels 4–7, Master clear (write)/temp (read)	00–07	
00DC	Channels 4–7, Clear Mask register (write)	00–03	
00DE	Channels 4–7, Write All Mask register bits	00–03	
00DF	Channels 5–7, 8- or 16-bit mode select	00–07	

PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 84440BX (Host bridge)
00	01	00	Intel 84440BX (PCI/ AGP)
00	02	00	Intel 82371AB PCI/ISA bus
00	02	01	Intel 82371AB IDE bus master
00	02	02	Intel 82371AB USB
00	02	03	Intel 82371AB power management
00	03	00	1938 Audio Controller
01	00	00	S3 Trio3D AGP video

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[4] Upper byte of memory address register.

Appendix C. IRQ and DMA Channel Assignments

The following figures list the interrupt request (IRQ) and direct memory access (DMA) channel assignments.

Figure 44. IRQ Channel Assignments	
IRQ	**System Resource**
NMI	Critical System Error
SMI	System Management Interrupt — Power Management
0	Reserved (interval timer)
1	Reserved (keyboard)
2	Reserved, Cascade interrupt from slave PIC
3	Available to user
4	COM1 [5]
5	LPT2/Audio (if present)
6	Diskette controller
7	LPT1 [5]
8	Real-time clock
9	Video
10	Available to user
11	Available to user
12	Mouse port
13	Reserved (math coprocessor)
14	Primary IDE (if present)
15	Secondary IDE (if present)

Figure 45. DMA Channel Assignments		
DMA Channel	**Data Width**	**System Resource**
0	8 bits	Open
1	8 bits	Open
2	8 bits	Diskette drive
3	8 bits	Parallel port (for ECP or EPP)
4	–	Reserved (cascade channel)
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

---

[5] Default, can be changed to another IRQ.

Appendix D. Error Codes

A complete list of POST error codes is provided in *PC 300GL User Guide* and in *Hardware Maintenance Manual*.

POST Error Codes

POST error messages appear when POST finds problems with the hardware during power-on or when a change in the hardware configuration is found. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages.

Beep Codes

A complete list of beep codes is provided in *Hardware Maintenance Manual*.

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