Technical Information Manual

S78H-5083-01

PC 330 (Type 6577) and PC 350 (Type 6587)

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Note

Before using this information and the product it supports, be sure to read the general information under Appendix E, “Notices and Trademarks” on page 55.

Second Edition (April 1997)

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Preface

This *Technical Information Manual* provides information for the IBM PC 330 (Type 6577) and the IBM PC 350 (Type 6587). It is intended for developers who want to provide hardware and software products to operate with these IBM computers and provides a more in-depth view of how these IBM computers work. Users of this publication should have an understanding of computer architecture and programming concepts.

Related Publications

In addition to this manual, the following IBM publications provide information related to the operation of the PC 330 and PC 350. To order publications in the U.S. and Puerto Rico, call 1-800-879-2755. In other countries, contact an IBM reseller or an IBM marketing representative.

- *Using Your Personal Computer*
  This publication contains information about configuring, operating, and maintaining the PC 330 and PC 350. Also, information on diagnosing and solving problems, how to get help and service, and warranty issues is included.
- *Installing Options in Your Personal Computer*
  This publication contains instructions for installing options in the PC 330 and PC 350.
- *Understanding Your Personal Computer*
  This publication includes general information about using computers and detailed information about the features of the PC 330 and PC 350.
- *PC 300 Systems (6577/6587) Compatibility Report*
  This publication contains information about compatible hardware and software for the PC 330 and PC 350. This publication is available at *http://www.pc.ibm.com/cdt*.

Manual Style

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

In this manual, some signals are represented in a small, all-capital-letter format (-ACK). A minus sign in front of the signal indicates that the signal is active low. No sign in front of the signal indicates that the signal is active high.

The use of the letter “h” indicates a hexadecimal number. Also, when numerical modifiers such as “K”, “M” and “G“ are used, they typically indicate powers of 2, not powers of 10. For example, 1 KB equals 1024 bytes (2^{10}), 1 MB equals 1048576 bytes (2^{20}), and 1 GB equals 1073741824 bytes (2^{30}).

When expressing storage capacity, MB equals 1000 KB (1024000). The value is determined by counting the number of sectors and assuming that every two sectors equals 1 KB.

Note: Depending on the operating system and other system requirements, the storage capacity available to the user might vary.

Chapter 1. System Overview

The IBM PC 330 (Type 6577) and PC 350 (Type 6587) are versatile products designed to provide state-of-the-art computing power with room for future growth. Several model variations are available.

Major Features

The major features are:

- Intel Pentium Processor or Intel Pentium Processor with MMX Technology
- 256 KB of external L2 cache (expandable to 512 KB)
- Up to 192 MB of system memory
- S3 Trio64V+ video subsystem
- 1 MB of video memory expandable to 2 MB
- Industry-standard compatibility
- ISA/PCI I/O-bus compatibility
- ISA/PCI expansion slots
- Enhanced IDE drives
- Bus master IDE controller
- One 16550-UART serial port
- Two USB ports
- One infrared port
- One parallel port
- Ports for keyboard and mouse
- EnergyStar compliant
- Choice of system unit size
  - The PC 330 has three expansion slots and three drive bays
  - The PC 350 has five expansion slots and five drive bays

Other Features

The following features are supported by the PC 330 and PC 350. Optional hardware is required for these features.

LAN Wake Up

Systems are configurable for LAN connection with an Ethernet adapter or a token ring adapter. To use this feature, LAN adapters that support LAN Wake Up are required. The LAN Wake Up feature allows the computer to turn on when a specific LAN frame is passed to the PC through the LAN. This feature works in coordination with Advanced Power Management (APM).

The menu used for setting the LAN Wake Up feature is found in the Configuration/Setup Utility program.

Wake Up On Ring

All models are configurable to turn on the computer after a ring is detected from an external or internal modem. The menu used for setting the Wake Up On Ring feature is found in the Configuration/Setup Utility program. Two options control this feature:

- **Serial Ring Detect:** Use this option if the computer has an external modem connected to the serial port.
- **Modem Ring Detect:** Use this option if the computer has an internal modem.

PCMCIA Support

The computer supports the addition of *Personal Computer Memory Card International Association (PCMCIA)* connectors attached to a PCMCIA adapter. Up to two PCMCIA connectors can be added to the computer; after installation, the connectors are accessible through a knock-out feature on the front panel of the computer. Each connector can accept type 1, 2, or 3 PC cards.

For information on purchasing the PCMCIA option or any other options:

- Within the U.S., call 1-800-IBM-2YOU (1-800-426-2968)
- Within Canada, call 1-800-565-3344 or 1-800-465-7999
- Outside the U.S. and Canada, contact the place of purchase or an IBM reseller

Chapter 2. System Board Features

This section includes information about system board features. For an illustration of the system board, see “System Board” on page 15.

Microprocessor

The microprocessor in the PC 330 (Type 6577) and PC 350 (Type 6587) is the Intel Pentium Processor or the Intel Pentium Processor with MMX Technology. The microprocessor features are:

- Intel Pentium Processor
  - 8 KB write-through code cache (internal)
  - 8 KB write-back data cache (internal)
- Intel Pentium Processor with MMX Technology
  - 16 KB write-through code cache (internal)
  - 16 KB write-back data cache (internal)
  - Split power supplies (V_{IO} = 3.3 V, V_{CORE} = 2.8 V)
  - Support for Intel architecture MMX technology
- Superscalar architecture
- Branch prediction
- Power management capabilities
- Enhanced floating point capabilities
- 64-bit data bus, 32-bit address bus

The system board operates with a 3.3 volt microprocessor. The microprocessor plugs directly into a 321-pin zero-insertion-force (ZIF) socket (Socket 7). Socket 7 allows for a performance upgrade. After installing an upgrade, the internal speed of the microprocessor is updated by setting switches on the system board. For information on switch configuration, see “Switches” on page 17.

Chipset Control

The Intel Triton-II chipset is the interface between the microprocessor and the following:

- L2 cache controller
- Memory subsystem
- PCI bus
- Bus master IDE connection
- High performance PCI to ISA bridge
- USB port

L2 Cache

The chipset supports an L2 cache that uses pipeline-burst, synchronous random access memory (SRAM). L2 cache modules are removable and the base size module of 256 KB is upgradable to 512 KB. In addition to these sizes, a "cacheless" state with 0 KB of L2 cache is supported. Characteristics of each L2 cache size are shown below.

Figure 1. L2 Cache Characteristics

Cache Characteristics	**256 KB L2 Cache**	**512 KB L2 Cache**
Cacheable Memory	64 MB	64 MB
Line Size	32 bytes	32 bytes
SRAM Type	2 chips 32K x 32	4 chips 32K x 32
SRAM Voltage	3.3 V with 3.3 V output	3.3 V with 3.3 V output
SRAM Speed	8.5 ns	8.5 ns
Tag RAM Type	1 chip 8K x 8	2 chips 8K x 8 or 1 chip 16K x 8
Tag RAM Voltage	5 V	5 V
Tag RAM Speed	15 ns	15 ns
Tag RAM Tag Address	A(25:18)	A(25:19)
Tag RAM Set Address	A(17:5)	A(18:5)

The L2 cache is a look-aside, direct-mapped (one-way associativity) cache architecture. The L2 cache operates in write-back mode, and by default, is implemented as unified cache (stores code and data). The L2 cache supports the cache timings shown below.

Figure 2. L2 Cache Timings

Cycle	**256 KB L2 (60/66 MHz)**	**512 KB L2 (60/66 MHz)**
Single Read	3	3
Burst Read Hit	3-1-1-1	3-1-1-1
Burst Read Hit Pipelined	3-1-1-1-1-1-1-1	3-1-1-1-2-1-1-1
Single Write	3	3
Burst Write Hit	3-1-1-1	3-1-1-1
Write Miss	NA	NA

System Memory

The system memory interface is controlled by the chipset. Dynamic random access memory (DRAM) is standard.

The maximum amount of system memory is 192 MB. For memory expansion, the system board provides four single inline memory module (SIMM) connectors and one dual inline memory module (DIMM) connector. The SIMM connectors on the system board are divided into two banks, with each bank containing two SIMM connectors; the DIMM connector is also designated as a bank. Minimally, two SIMMs (of equivalent type, speed, and size) or one DIMM must be installed.

The following figure shows the system memory speed and size supported.

Figure 3. System Memory Speed and Size

Type	Speed (ns)	Size (MB)
SIMM	60	4, 8, 16, 32
DIMM	60	8, 16, 32, 64

The following information applies to system memory:

- Extended data output (EDO), nonparity memory is standard.
- Memory modules have a maximum height of 2.54 cm (1 in.).
- Only industry-standard, tin-lead SIMMs and gold-lead DIMMs are supported.
- A mix of parity and nonparity type configures as nonparity.

For information on the pin assignments for the memory module connectors, see “SIMM Connectors” on page 33 and “DIMM Connector” on page 34.

The following figure shows configuration information for the supported SIMMs and DIMMs.

Figure 4. System Memory Configuration

Total Memory (MB)	Bank 2 (SIMM 3, 4)	Bank 1 (SIMM 1, 2)	Bank 0 (DIMM 0)
8	0, 0	4, 4	0
16	0, 0	0, 0	16
16	4, 4	4, 4	0
24	0, 0	4, 4	16
24	4, 4	0, 0	16
32	0, 0	0, 0	32
32	8, 8	8, 8	0
40	4, 4	8, 8	16
40	0, 0	4, 4	32
48	4, 4	4, 4	32
64	8, 8	8, 8	32
72	4, 4	16, 16	32
80	8, 8	16, 16	32
96	16, 16	16, 16	32
128	16, 16	32, 32	32
192	32, 32	32, 32	64

PCI Bus

The fully synchronous 30/33 MHz PCI bus originates in the chipset. Features of the PCI bus are:

- Zero wait state microprocessor-to-PCI write interface for high performance graphics
- Built-in PCI bus arbiter with support for up to five masters
- Microprocessor-to-PCI memory write posting with 4 Dword deep buffers
- Converts back-to-back sequential microprocessor-to-PCI memory write to PCI burst write
- PCI-to-DRAM posting 12 Dwords
- PCI-to-DRAM up to 133 MB/sec bandwidth
- Multi-transaction timer to support multiple short PCI transactions within one PCI arb cycle
- PCI 2.1 compliant

Bus Master IDE Interface

The system board incorporates a PCI-to-IDE interface that complies with the *AT Attachment Interface with Extensions*. The subsystem that controls direct access storage devices (DASD) is integrated with the IDE interface.

The chipset functions as a *bus master* for the IDE interface. The chipset is PCI 2.1 compliant; it connects directly to the PCI bus and is designed to allow concurrent operations on the PCI bus and IDE bus. The chipset is capable of supporting PIO mode 0-4 devices and IDE DMA mode 0-2 devices.

A ribbon cable provided with the computer can attach up to four IDE devices to the IDE connectors on the system board. The IDE devices receive their power through a four-position power cable containing +5, +12, and ground voltage. When adding devices to the IDE interface, one device is designated as the primary or master device and another is designated as the secondary or subordinate device. These designations are determined by switches or jumpers on each device.

For the IDE interface, no resource assignments are given in the system memory or the direct memory access (DMA) channels. For information on the resource assignments, see “Input/Output Address Map” on page 46 and Figure 60 on page 51 (for IRQ assignments).

Two connectors are provided on the system board for the IDE interface. For information on the connector pin assignments, see “IDE Connectors” on page 36.

PCI to ISA Bridge

On the system board, the chipset provides the interface between the peripheral component interface (PCI) and industry standard architecture (ISA) buses. The chipset is used to convert PCI bus cycles to ISA bus cycles; the chipset also includes all the subsystems of the ISA bus, including two cascaded interrupt controllers, two DMA controllers with four 8-bit and three 16-bit channels, three counters equivalent to a programmable interval timer, and power management. The ISA bus operates at speeds of 7.5 MHz with a 60 MHz microprocessor bus and 8.25 MHz with a 66 MHz microprocessor bus (one-quarter of the PCI bus speed).

For the ISA bus, no resource assignments are given in the system memory or the DMA channels. For information on resource assignments, see “Input/Output Address Map” on page 46 and Figure 60 on page 51 (for IRQ assignments).

USB Interface

Universal serial bus (USB) technology is a standard feature of the computer. Using the chipset, the system board provides the USB interface with two connectors. A USB-enabled device can attach to each connector, and if that device is a hub, multiple peripherals can attach to the hub and be used by the system. The USB connectors use Plug and Play technology for installed devices. The speed of the USB is up to 12 Mb/s with a maximum of 127 peripherals.

Features provided by USB technology include:

- Hot pluggable
- Support for concurrent operation of multiple devices
- Suitable for different device bandwidths
- Up to five meters length from host to hub or hub to hub
- Guaranteed bandwidth and low latencies appropriate for specific devices
- Wide range of packet sizes
- Limited power to hubs

For information on the connector pin assignments for the USB interface, see “USB Connectors” on page 36.

Video Subsystem

The video subsystem on the system board includes the *S3 Trio 64V+* chip, up to 2 MB of EDO DRAM, and the video local peripheral bus (LPB) interface.

S3 Trio64V+ Chip

The S3 Trio64V+ chip supports all video graphics array (VGA) modes and is compliant with super video graphics array (SVGA) modes, Video Electronics Standards Association (VESA) 1.2. Some enhanced features of the chip are:

- Plug and Play support
- 50 or 60 nanosecond (ns) single-cycle EDO DRAM support
- Rapid Resume power-down support
- 24-bit packed pixel mode
- Color space conversion
- Hardware scaling

The chip is connected to the PCI bus and is PCI 2.1 compliant. The S3 video subsystem supports the VESA Display Data Channel (DDC) standard 1.1 and uses DDC1 and DDC2B to determine optimal values during automatic monitor detection.

For information on resource assignments, see Appendix B, “System Address Maps” on page 46 and Appendix C, “IRQ and DMA Channel Assignments” on page 51.

The video subsystem provides a video port on the system board; one connector is provided for attaching a monitor. For information on connector pin assignments, see “Monitor Connector” on page 38.

Video Memory

The system is shipped standard with two video memory modules that total 1 MB and create a 32-bit data path to video memory. An upgrade is available that increases the total video memory to four modules or 2 MB and creates a 64-bit data path to video memory. The maximum amount of video memory that can be used with the video subsystem is 2 MB.

The video memory modules used are 256 KB x 16 (512 KB total), 50 or 60 ns, EDO DRAMs. When adding video memory, 50 or 60 ns DRAMs can be used. If the computer has 50 ns DRAMs preinstalled and 60 ns DRAMs are added, the video subsystem will run at 60 ns. Likewise, if the computer has 60 ns DRAMs preinstalled and 50 ns DRAMs are added, the video subsystem will run at 60 ns.

Video Local Peripheral Bus Interface

The video local bus peripheral (LPB) interface is implemented on the system board. The LPB interface can be programmed for various modes of operation. The LPB provides an interface to the standard 8-bit VESA connector.

The LPB interface is composed of a 2 x 13-pin berg strip connector plus a 6-pin extension for the additional signals required by various LPB modes; this connector is J39 on the system board. The 6-pin extension is offset from the connector to allow room for the 2 x 13 cable header when the 6-pin extension is not used. Also included is a 2 x 8-pin berg strip connector that provides power, resets, and interrupts; this connector is J34 on the system board. To locate jumpers on the system board, see “System Board” on page 15. For information on the pin assignments, see “Video VESA/LPB Connectors” on page 37.

Input/Output Controller

Control of the integrated input/output (I/O) ports and diskette drive controller is provided by a single chip, the National Semiconductor PC87306. This chip, which supports Plug and Play, controls the following features:

- Diskette drive support
- Serial port
- Parallel port
- Keyboard and mouse ports
- Infrared port
- General purpose I/O ports
- Real-time clock

The chip requires an external 24 MHz frequency.

Diskette Drive Support

A maximum of two diskette drives and one tape backup drive is supported on the system board. The actual number of diskette drives that can be installed is dependent upon the system unit size (the PC 330 has three drive bays for installing devices and the PC 350 has five drive bays for installing internal devices). The following is a list of devices that the diskette drive subsystem supports:

- 1.44 MB, 3.5" diskette drive
- 2.88 MB, 3.5" diskette drive
- 1.2 MB, 5.25" diskette drive
- 1 Mbps, 500 Kbps, or 250 Kbps tape drive

One connector is provided on the system board for diskette drive support. For information on the connector pin assignments, see “Diskette Drive Connector” on page 38.

Serial Port

Integrated into the system board is one universal asynchronous receiver/transmitter (UART) serial port. The serial port includes a 16-byte data, first-in first-out (FIFO) buffer, and has programmable baud rate generators. The serial port is NS16450 and PC16550A compatible.

Note: Current loop interface is not supported.

The following figure shows the serial port assignments used in configuration.

Figure 5. Serial Port Assignments

Port Assignment	Address Range	IRQ Level
Serial 1	03F8h–03FFh	IRQ4
Serial 2	02F8h–02FFh	IRQ3
Serial 3	03E8h–03FFh	IRQ4
Serial 4	02E8h–02FFh	IRQ3

On the system board, one connector is provided for the UART serial port. For information on the connector pin assignments, see “Serial Port Connector” on page 39.

Parallel Port

Integrated in the system board is support for extended capabilities port (ECP), enhanced parallel port (EPP) and standard parallel port (SPP) modes. The modes of operation are selected through the Configuration/Setup Utility program with the default mode set to SPP.

The following figure shows the parallel port assignments used in configuration.

Figure 6. Parallel Port Assignments

Port Assignment	Address Range	IRQ Level
Parallel 1	03BCh–03BEh	IRQ7
Parallel 2	0378h–037Fh	IRQ5
Parallel 3	0278h–027Fh	IRQ5

The system board has one connector for the parallel port. For information on the connector pin assignments, see “Parallel Port Connector” on page 39.

Keyboard and Mouse Ports

The keyboard and mouse subsystem is controlled by a general purpose 8-bit microcontroller; it is compatible with 8042AH. The controller consists of 256 bytes of data memory and 2 KB of read only memory (ROM).

The controller has two logical devices: one controls the keyboard and the other controls the mouse. The keyboard has two fixed I/O addresses and a fixed IRQ line and can operate without the mouse. The mouse cannot operate without the keyboard because, although it has a fixed IRQ line, the mouse relies on the addresses of the keyboard for operation. For the keyboard and mouse interfaces, no resource assignments are given in the system memory addresses or DMA channels. For information on the resource assignments, see “Input/Output Address Map” on page 46 and Figure 60 on page 51 (for IRQ assignments).

The system board has one connector for the keyboard port and one connector for the mouse port. For information on the connector pin assignments, see “Keyboard and Mouse Port Connectors” on page 40.

Infrared Port

The computer comes with an infrared (IR) port for connecting an optional infrared transceiver module. The infrared transceiver allows wireless communication between the computer and other infrared-capable devices.

The transceiver plugs into this connector and provides a link of up to one meter at a rate of 115 kilobits-per-second (Kbps). The IR connector uses any of the same four port assignments as the serial port.

The system board has one connector for the infrared port. For information on the connector pin assignments for the infrared port, see “Infrared Port Connector” on page 40.

General Purpose I/O Ports

The system board has up to 16 general purpose input/output (GPIO) pins which are implemented by two 8-bit GPIO ports. The use of GPIO pins is dependent upon system design. Features of the GPIO ports are:

- Open-drain outputs with internal pull-ups and transistor-transistor logic (TTL) inputs
- Base address is software configurable
- Direction is programmable
- Occupies 4-byte I/O address

Real-Time Clock and CMOS

The real-time clock is a low-power clock that provides a time-of-day clock and a calendar. The clock settings are maintained by an external battery source of 3 V.

The system uses 242 bytes of memory to store complementary metal-oxide semiconductor (CMOS) memory. Moving a jumper (J18) on the system board erases CMOS memory.

To locate the battery or J18, see “System Board” on page 15.

Flash EEPROM

The system board uses a flash electrically-erasable, programmable, read-only memory (EEPROM) chip to store the basic input/output system (BIOS), video BIOS, IBM logo, Configuration/Setup Utility, and Plug and Play data.

If necessary, the EEPROM can be easily updated using a standalone utility program that is available on a 3.5" diskette.

Riser Card

The system board uses a riser card to route PCI and ISA bus signals to the expansion connectors. Each ISA-expansion connector is 16-bits, and each PCI-expansion connector is 32-bits. PCI-expansion connectors support the 32-bit 5-V dc local-bus signalling environment that is defined in *PCI Local Bus Specification 2.1*. The ISA bus is buffered to provide sufficient drive for the ISA-expansion connectors, assuming two low-power Schottky (LS) loads per slot.

The system board uses one of two riser cards. Different riser cards provide a different configuration of PCI and ISA connectors and are representative of the different mechanical sizes. The following figure summarizes the characteristics of the two riser cards.

Figure 7. Riser Card Characteristics

Expansion Slots	3x3 Riser Card	5x5 Riser Card
Shared ISA/PCI	3	3
Dedicated ISA	0	2
Dedicated PCI	0	0

For information on the connector pin assignments, see “ISA Connectors” on page 41 and “PCI Connector” on page 42.

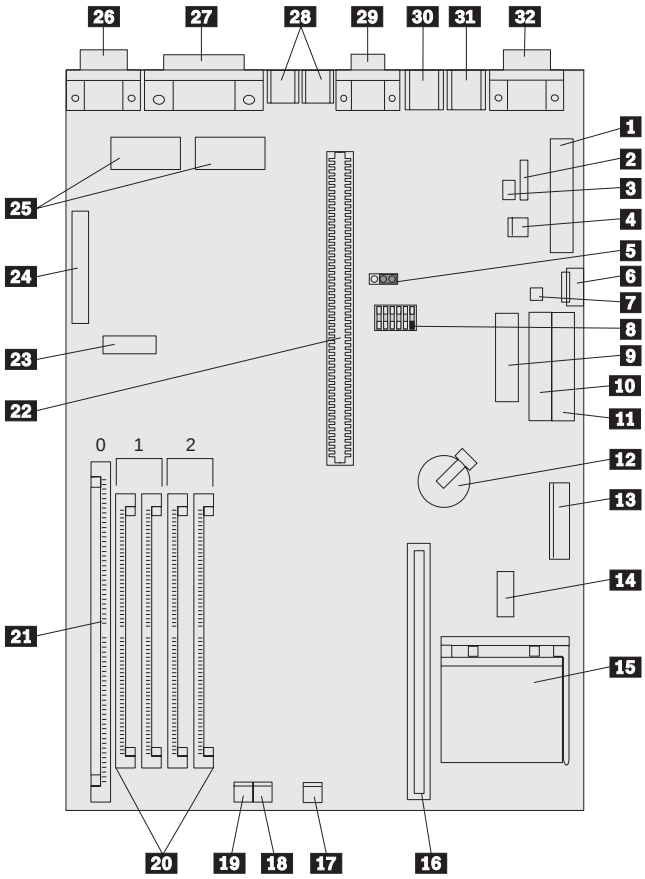
Physical Layout

The system board might look slightly different from the one shown.

Note: A diagram of the system board, including switch and jumper settings, is attached to the underside of the computer cover.

System Board

1 Power connector (5 V, 12 V)
2 J6 Modem ring
3 J11 LAN Wake Up
4 J7 Modem ring
5 J18 Password jumper (CMOS clear)
6 J1 Auxiliary power
7 On/Off switch
8 Configuration switch (SW1)
9 Diskette connector
10 Primary IDE connector
11 Secondary IDE connector
12 Battery
13 Power connector (3.3 V)
14 J12 VRM connector
15 Processor/upgrade socket
16 L2 cache module connector
17 Fan connector
18 Power LED connector
19 Hard disk access LED connector
20 SIMM connectors (Bank 1/2)
21 DIMM connector (Bank 0)
22 Riser connector
23 J34 video VESA/LPB feature
24 J39 video VESA/LPB feature
25 Video memory upgrade sockets
26 Monitor port
27 Parallel port
28 USB ports (1, 2)
29 Serial (A) port
30 Mouse port
31 Keyboard port
32 Infrared port



Jumpers

Jumpers on the system board are used for custom configurations. The following figures show the description of pin numbers for specific jumpers. To locate these jumpers, see “System Board” on page 15.

Figure 8. J1 Auxiliary Power

Pin	Description
1	Auxiliary (+5 V)
2	Switch input to power management circuit
3	Ground

Figure 9. J6 Modem Ring

Pin	Description
1	Auxiliary (+5 V)
2	Key
3	External Wake Up on Ring
4	Ground

Figure 10. J7 Modem Ring

Pin	Description
1	Ground
2	External Wake Up on Ring

Figure 11. J11 LAN Wake Up

Pin	Description
1	Ground
2	External LAN Wake-Up/Ring

Figure 12. J18 Password Jumper/CMOS Clear

Pins	Description
1 and 2	Normal
2 and 3	Clear Password/CMOS

Switches

The switches (SW1) are used for setting the microprocessor speed and diskette-write protection.

The following figure shows the configuration of switches 1–4 for the different microprocessor speeds.

Figure 13. Microprocessor Speed (SW1 1-4)

Switch	100 MHz	120 MHz	133 MHz	150 MHz	166 MHz	200 MHz
1	Off	On	On	On	On	Off
2	Off	Off	Off	On	On	On
3	Off	On	Off	On	Off	Off
4	On	Off	On	Off	On	On

The following figure shows the configuration of switch 6 for diskette-write protection.

Figure 14. Diskette-Write Protection (SW1 6)

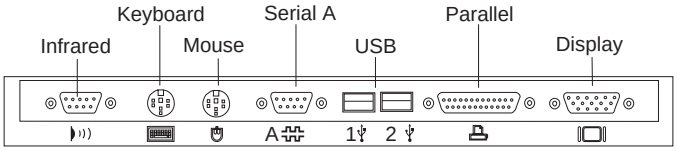
Switch	Diskette Write-Enabled	Diskette Write-Protected
6	Off	On

Back-Panel Connectors

The standard connectors are on a panel at the back of the computer. The standard connectors are:

- Keyboard connector
- Mouse connector
- Serial connector
- Infrared transceiver module connector
- Parallel port connector
- Monitor (display) connector
- Two USB connectors

Each connector is identified by a symbol, as shown in the following figure.



Note: If adapters are installed, other connectors might appear in the expansion slots above the back-panel connector.

Chapter 3. Physical Specifications

This section lists the physical specifications for the PC 330 and the PC 350. The PC 330 has three expansion slots and three drive bays, and the PC 350 has five expansion slots and five drive bays.

Note:

- The maximum altitude for both the PC 330 and PC 350 is 2133.6 m (7000 ft.). This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.
- Both PC 330 and PC 350 are electromagnetic compatible with FCC Class B.

PC 330

The following figures list the physical attributes for the PC 330.

Figure 15. Size (PC 330)	
Description	**Measurement**
Width	360 mm (14.2 in)
Depth	465 mm (18.3 in)
Height	130 mm (5.1 in)

Figure 16. Weight (PC 330)	
Description	**Measurement**
Minimum configuration	8.6 kg (19.0 lb)
Maximum configuration (fully populated with typical options)	10.4 kg (23.0 lb)

Figure 17. Cables (PC 330)	
Description	**Measurement**
Power cable	1.8 m (6 ft)
Keyboard cable	2 m (6 ft 6.7 in)

Figure 18. Air Temperature (PC 330)	
Description	**Measurement**
System on	10.0 to 32.0°C (50 to 90°F)
System off	10.0 to 43.0°C (50 to 110°F)

Figure 19. Humidity (PC 330)	
Description	**Measurement**
System on	8% to 80%
System off	8% to 80%

Figure 20. Heat Output (PC 330)	
Description	**Measurement**
Minimum configuration	35 W (120 Btu per hour)
Maximum configuration (based on 145-watt maximum capacity of the power supply)	200 W (685 Btu per hour)

Figure 21. Electrical (PC 330)	
Description	**Measurement**
Low range	90 (min) to 137 (max) V ac
High range	180 (min) to 265 (max) V ac
Frequency	50 ± 3 Hz or 60 ± 3 Hz
Input, Minimum configuration	0.08 kVA
Input, Maximum configuration	0.30 kVA

PC 350

The following figures list the physical attributes for the PC 350.

Figure 22. Size (PC 350)

Description	Measurement
Width	420 mm (16.5 in)
Depth	455 mm (17.9 in)
Height	160 mm (6.3 in)

Figure 23. Weight (PC 350)

Description	Measurement
Minimum configuration	12.7 kg (28.0 lb)
Maximum configuration (fully populated with typical options)	14.1 kg (31.1 lb)

Figure 24. Cables (PC 350)

Description	Measurement
Power cable	1.8 m (6 ft)
Keyboard cable	2 m (6 ft 6.7 in)

Figure 25. Air Temperature (PC 350)	
Description	**Measurement**
System on	10.0 to 32.0°C (50 to 90°F)
System off	10.0 to 43.0°C (50 to 110°F)

Figure 26. Humidity (PC 350)	
Description	**Measurement**
System on	8% to 80%
System off	8% to 80%

Figure 27. Heat Output (PC 350)	
Description	**Measurement**
Minimum configuration	35 W (120 Btu per hour)
Maximum configuration (based on 200-watt maximum capacity of the power supply)	310 W (1060 Btu per hour)

Figure 28. Electrical (PC 350)	
Description	**Measurement**
Low range	90 (min) to 137 (max) V ac
High range	180 (min) to 265 (max) V ac
Frequency	50 ± 3 Hz or 60 ± 3 Hz
Input, Minimum configuration	0.08 kVA
Input, Maximum configuration	0.52 kVA

Chapter 4. Power Supply

The power supply requirements are supplied by a 145-watt (PC 330) or 200-watt (PC 350) power supply. The power supply converts the ac input voltage into four dc output voltages and provides power for the following:

- System board
- Adapters
- Internal DASD drives
- Keyboard and auxiliary devices

A logic signal on the power connector controls the power supply; the front panel switch is not directly connected to the power supply.

Power Input

The following figure shows the input power specifications. The power supply has a manual switch to select the correct input voltage.

Figure 29. Power Input Requirements

Specification	Measurements
Input voltage, low range	90 (min)–137 (max) V ac
Input voltage, high range	180 (min)–265 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz

Power Output

The power supply outputs shown in the following figures include the current supply capability of all the connectors, including system board, DASD, PCI, and auxiliary outputs.

Note: Simultaneous loading of +5 V and +3.52 V must not exceed 90 watts.

PC 330

Figure 30. Power Output (145 Watt)

Output Voltage	Regulation	Minimum Current	Maximum Current
+5 volts	+5% to -4%	1.5 A	18.0 A
+12 volts	+5% to -5%	0.2 A	4.2 A
-12 volts	+10% to -9%	0.0 A	0.4 A
-5 volts	+10% to -10%	0.0 A	0.3 A
+3.52 volts	+2% to -2%	0.0 A	10.0 A
+5 volt (auxiliary)	+5% to -10%	0.0 A	.02 A
+5 volt (LAN Wake-Up)	+5% to -10%	0.0 A	.30 A

PC 350

Figure 31. Power Output (200 Watt)

Output Voltage	Regulation	Minimum Current	Maximum Current
+5 volts	+5% to -4%	1.5 A	20.0 A
+12 volts	+5% to -5%	0.2 A	8.0 A
-12 volts	+10% to -9%	0.0 A	0.5 A
-5 volts	+10% to -10%	0.0 A	0.5 A
+3.52 volts	+2% to -2%	0.0 A	20.0 A
+5 volt (auxiliary)	+5% to -10%	0.0 A	.02 A
+5 volt (Wake on LAN)	+5% to -10%	0.0 A	.30 A

Component Outputs

The power supply provides separate voltage sources for the system board and internal storage devices. The following figures show the approximate power that is provided for specific system components. Many components draw less current than the maximum shown.

Figure 32. System Board

Supply Voltage	Maximum Current	Regulation Limits
+3.52 V dc	3000 mA	+2% to –2.0%
+5.0 V dc	4000 mA	+5.0% to –4.0%
+12.0 V dc	25.0 mA	+5.0% to –5.0%
–12.0 V dc	25.0 mA	+10.0% to –9.0%

Figure 33. Keyboard Port

Supply Voltage	Maximum Current	Regulation Limits
+5.0 V dc	275 mA	+5.0% to –4.0%

Figure 34. Auxiliary Device Port

Supply Voltage	Maximum Current	Regulation Limits
+5.0 V dc	300 mA	+5.0% to –4.0%

Figure 35. ISA-Bus Adapters (Per Slot)

Supply Voltage	Maximum Current	Regulation Limits
+5.0 V dc	4500 mA	+5.0% to –4.0%
–5.0 V dc	200 mA	+5.0% to –5.0%
+12.0 V dc	1500 mA	+5.0% to –5.0%
–12.0 V dc	300 mA	+10.0% to –9.0%

Figure 36. PCI-Bus Adapters (Per Slot)

Supply Voltage	Maximum Current	Regulation Limits
+5.0 V dc	5000 mA	+5.0% to –4.0%
+3.52 V dc	5000 mA	+5.0% to –4.0%

Note: For each PCI connector, the maximum power consumption is rated at 25 watts for +5 V and +3.52 V combined.

Figure 37. Internal DASD		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V dc	1400 mA	+5.0% to –5.0%
+12.0 V dc	1500 mA	+5.0% to –5.0%

Note: Some adapters and hard disk drives draw more current than the recommended limits. These adapters and drives can be installed in the system; however, the power supply will shut down if the total power used exceeds the maximum power that is available.

Output Protection

The power supply protects against output overcurrent, overvoltage, and short circuits. Please see the power supply specifications for details.

A short circuit that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply. If this shutdown state occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Connector Description

The power supply for the PC 330 has three 4-pin connectors and the PC 350 has five 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in “Component Outputs” on page 25. For information on the pin assignments for the different connectors, see Appendix A, “Connector Pin Assignments” on page 33.

Chapter 5. System Software

This section briefly describes some of the system software included with the computer.

BIOS

The system uses the IBM SurePath basic input/output system (BIOS), which is stored in flash electrically erasable programmable read only memory (EEPROM). Some features of the BIOS are:

- PCI support according to PCI BIOS Specification 2.0
- Plug and Play support according to Plug and Play BIOS Specification 1.1
- Advanced Power Management (APM) support according to APM BIOS Interface Specification 1.1
- PCI Bus Master IDE interface with device specific performance tuning
- IDE LBA support
- S3 video BIOS for the video chip
- Bootable CD-ROM support

Plug and Play

Support for Plug and Play conforms to the following:

- Plug and Play BIOS Specification 1.1 and 1.0
- Plug and Play BIOS Extension Design Guide 1.0
- Plug and Play BIOS Specification, Errata and Clarifications 1.0
- Guide to Integrating the Plug and Play BIOS Extensions with system BIOS 1.2
- Plug and Play Kit for DOS and Windows

POST

IBM power-on self test (POST) code is used. Also, initialization code is included for the Intel 54C microprocessor, the 82430HX chipset, the I/O chip, and the video chip.

POST error codes include text messages for determining the cause of an error. For more information, see Appendix D, “Error Codes” on page 52.

Configuration/Setup Utility

The Configuration/Setup Utility program provides menus for selecting options for devices, I/O ports, date and time, system security, start options, advanced setup, ISA legacy resources, and power management.

More information on using the Configuration/Setup Utility program is provided in *Using Your Personal Computer*.

Advanced Power Management (APM)

The PC 330 and PC 350 come with built-in energy-saving capabilities. Advanced Power Management (APM) is a feature that reduces the power consumption of systems when they are not being used. When enabled, APM initiates reduced-power modes for the monitor, microprocessor, and hard disk drive after a specified period of inactivity.

The BIOS supports APM 1.1. This enables the system to enter a power managed state, which reduces the power drawn from the ac wall outlet. Advanced Power Management is enabled through the Configuration/Setup Utility program and is controlled by the individual operating system.

For more information on APM, see *Using Your Personal Computer* and *Understanding Your Personal Computer*.

Flash Update Utility

The flash update utility is a standalone program to support flash code updates. This utility program updates the BIOS code in flash and the MRI to different languages.

The flash update utility program is available on a 3.5" diskette.

Diagnostic Programs

Two diagnostic products are supplied with the PC 330 and PC 350: QAPlus/WIN-WIN, a Windows program which provides the best software coverage, and QAPlus/PRO for DOS which provides the best hardware coverage.

For more information on these diagnostic programs, see *Using Your Personal Computer*.

Chapter 6. System Compatibility

This chapter discusses some of the hardware, software, and BIOS compatibility issues for the computer. Refer to *PC 300 Systems (6577/6587) Compatibility Report* for a list of compatible hardware and software options.

Hardware Compatibility

This section discusses hardware, software, and BIOS compatibility issues that must be considered when designing application programs.

Many of the interfaces are the same as those used by the IBM Personal Computer AT. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces are compatible with the following interfaces:

- The Intel 8259 interrupt controllers (edge-triggered mode)
- The National Semiconductor NS16450 and NS16550A serial communication controllers
- The Motorola MC146818 Time of Day Clock command and status (CMOS reorganized)
- The Intel 8254 timer, driven from a 1.193 MHz clock (channels 0, 1, and 2)
- The Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions; the Mode register is partially supported
- The Intel 8272 or 82077 diskette drive controllers
- The Intel 8042 keyboard controller at addresses 0060h and 0064h
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode

Use the following information to develop application programs. Whenever possible, use the BIOS as an interface to hardware to provide maximum compatibility and portability of applications among systems.

Hardware Interrupts

Hardware interrupts are level sensitive for PCI interrupts and edge sensitive for ISA interrupts. The interrupt controller clears its in-service register bit when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI command is sent regardless of whether the incoming interrupt request to the controller is active or inactive.

The interrupt-in-progress latch is readable at an I/O-address bit position. This latch is read during the interrupt service routine and might be reset by the read operation or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

With level-sensitive interrupts, the interrupt controller requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler:

1. Clears the interrupt
2. Waits one I/O delay
3. Sends the EOI
4. Waits one I/O delay
5. Enables the interrupt through the Set Interrupt Enable Flag command

Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt 0Ah. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.
2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.
3. When the interrupt occurs, the system microprocessor passes control to the IRQ9 (interrupt 71h) interrupt handler.
4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt 0Ah) interrupt handler.
5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

Diskette Drives and Controller

The following figures show the reading, writing, and formatting capabilities of each type of diskette drive.

Figure 38. 5.25-Inch Diskette Drive Reading, Writing, and Formatting Capabilities

Diskette Drive Type	250/500 KB Mode	300/500 KB Mode	1 MB Mode
Single sided (48 TPI)	RWF	—	—
Double sided (48 TPI)	RWF	RWF	—
High capacity (1.2 MB)	RWF	RWF	RWF

Figure 39. 3.5-Inch Diskette Drive Reading, Writing, and Formatting Capabilities

Diskette Drive Type	720 KB Mode	1.44 MB Mode	2.88 MB Mode
1.44 MB drive	RWF	RWF	—
2.88 MB drive	RWF	RWF	RWF

Notes:

1. Do not use 5.25-inch diskettes that are designed for the 1.2MB mode in either a 250/500 KB or 300/500 KB diskette drive.
2. Low-density 5.25-inch diskettes that are written to or formatted by a high-capacity 1.2 MB diskette drive can be reliably read only by another 1.2 MB diskette drive.
3. Do not use 3.5-inch diskettes that are designed for the 2.88 MB mode in a 1.44MB diskette drive.

Copy Protection

The following methods of copy protection might not work in systems using the 3.5-inch 1.44 MB diskette drive.

- Bypassing BIOS routines:
  - Data transfer rate: BIOS selects the proper data transfer rate for the media being used.
  - Diskette parameter table: Copy protection, which creates its own diskette parameter table, might not work in these drives.
- Diskette drive controls:
  - Rotational speed: The time between two events in a diskette drive is a function of the controller.
  - Access time: Diskette BIOS routines must set the track-to-track access time for the different types of media that are used in the drives.
  - 'Diskette change' signal: Copy protection might not be able to reset this signal.
- Write-current control: Copy protection that uses write-current control does not work, because the controller selects the proper write current for the media that is being used.

Hard Disk Drives and Controller

Reading from and writing to the hard disk is initiated in the same way as in IBM Personal Computer products; however, new functions are supported.

Software Compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02F*x* or 06F*x*, where *x* is the interrupt level) does not create interference.

Software Interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-Sensitive Programs

Programs can select machine-specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H).

Appendix A. Connector Pin Assignments

The following figures show the pin assignments for various system board connectors.

SIMM Connectors

Figure 40. 72-Pin Assignments for the SIMM Connector

Pin	Signal	Pin	Signal
1	Ground	37	Parity 1
2	Data 0	38	Parity 3
3	Data 16	39	Ground
4	Data 1	40	Column address strobe 0
5	Data 17	41	Column address strobe 2
6	Data 2	42	Column address strobe 3
7	Data 18	43	Column address strobe 1
8	Data 3	44	Row address strobe 0
9	Data 19	45	Row address strobe 1
10	+5 V dc	46	Reserved
11	Reserved	47	Write enable
12	Address 0	48	Reserved
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Address 10	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 V dc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Address 11	65	Data 15
30	+5 V dc	66	Reserved
31	Address 8	67	Reserved
32	Address 9	68	Reserved
33	Row address strobe 3	69	Reserved
34	Row address strobe 2	70	Reserved
35	Parity 2	71	Reserved
36	Parity 0	72	Ground

DIMM Connector

Figure 41 (Page 1 of 2). 168-Pin Assignments for the DIMM Connector

Pin	Signal	Pin	Signal
1	GND	85	GND
2	MD0	86	MD32
3	MD1	87	MD33
4	MD2	88	MD34
5	MD3	89	MD35
6	VDD	90	VDD
7	MD4	91	MD36
8	MD5	92	MD37
9	MD6	93	MD38
10	MD7	94	MD39
11	PAR0	95	PAR4
12	GND	96	GND
13	MD16	97	MD48
14	MD17	98	MD49
15	MD18	99	MD50
16	MD19	100	MD51
17	MD20	101	MD52
18	VDD	102	VDD
19	MD21	103	MD53
20	MD22	104	MD54
21	MD23	105	MD55
22	PAR2	106	PAR6
23	GND	107	GND
24	NC	108	NC
25	NC	109	NC
26	VDD	110	VDD
27	WE0	111	NC
28	CAS0	112	CAS2
29	CAS2	113	CAS3
30	RAS0	114	RAS1
31	OE0	115	NC
32	GND	116	GND
33	A0A	117	A1
34	A2	118	A3
35	A4	119	A5
36	A6	120	A7
37	A8	121	A9
38	A10	122	A11
39	A12	123	A13
40	VDD	124	VDD
41	NC	125	NC

Figure 41 (Page 2 of 2). 168-Pin Assignments for the DIMM Connector

Pin	Signal	Pin	Signal
42	NC	126	B0
43	GND	127	GND
44	OE1	128	NC
45	RAS2	129	RAS3
46	CAS4	130	CAS6
47	CAS5	131	CAS7
48	WE1	132	PDE
49	VDD	133	VDD
50	NC	134	NC
51	NC	135	NC
52	MD8	136	MD40
53	MD9	137	MD41
54	GND	138	GND
55	MD10	139	MD42
56	MD11	140	MD43
57	MD12	141	MD44
58	MD13	142	MD45
59	VDD	143	VDD
60	MD14	144	MD46
61	NC	145	NC
62	DU	146	NC
63	NC	147	NC
64	NC	148	GND
65	MD15	149	MD47
66	PAR1	150	PAR5
67	MD24	151	MD56
68	GND	152	GND
69	MD25	153	MD57
70	MD26	154	MD58
71	MD27	155	MD59
72	MD28	156	MD60
73	VDD	157	VDD
74	MD29	158	MD61
75	MD30	159	MD62
76	MD31	160	MD63
77	PAR3	161	PAR7
78	GND	162	GND
79	PD1	163	PD2
80	PD3	164	PD4
81	PD5	165	PD6
82	PD7	166	PD8
83	ID0	167	ID1
84	VDD	168	VDD

IDE Connectors

Figure 42. 40-Pin Assignments for the IDE Connectors

Pin	Signal	Pin	Signal
1	-RESET	2	Ground
3	Data bus bit 7	4	Data bus bit 8
5	Data bus bit 6	6	Data bus bit 9
7	Data bus bit 5	8	Data bus bit 10
9	Data bus bit 4	10	Data bus bit 11
11	Data bus bit 3	12	Data bus bit 12
13	Data bus bit 2	14	Data bus bit 13
15	Data bus bit 1	16	Data bus bit 14
17	Data bus bit 0	18	Data bus bit 15
19	Ground	20	Key (Reserved)
21	DRQ0/DRQ1	22	Ground
23	-IO Write	24	Ground
25	-IO Read	26	Ground
27	IO Channel Ready	28	No Connect
29	DACK0/DACK1	30	Ground
31	IRQ14/IRQ15	32	No Connect
33	Device address A1	34	No Connect
35	Device address A0	36	Device address A2
37	-HFCS0	38	-HFCS1
39	Activity LED	40	Ground

USB Connectors

Figure 43. 4-Pin Assignments for the USB Connectors

Pin	Signal
1	VCC
2	-Data
3	+Data
4	Ground

Video VESA/LPB Connectors

Figure 44. 34-Pin Assignments for the VESA/LPB Connector - J39

Pin	Signal	I/O	Pin	Signal	I/O
1	Ground	N/A	2	PA0/LPB0	I/O
3	Ground	N/A	4	PA1/LPB1	I/O
5	Ground	N/A	6	PA2/LPB2	I/O
7	EVIDEO/GREQ#/GRDY	I/O	8	PA3/LPB3	I/O
9	ESYNC	I	10	PA4/LPB4	I/O
11	EVCLK/DREQ#/DRDY	I	12	PA5/LPB5	I/O
13	NC	N/A	14	PA6/LPB7	I/O
15	Ground	N/A	16	PA7/LPB7	I/O
17	Ground	N/A	18	VPXLCLK/LCLK	I/O
19	Ground	N/A	20	BLANK#	I/O
21	Ground	N/A	22	HSYNC	I/O
23	NC	N/A	24	VSYNC	I/O
25	NC	N/A	26	Ground	N/A
27	KEY	N/A	28	KEY	N/A
29	Ground	N/A	30	IICCLK	I/O
31	NC	N/A	32	IICDAT	I/O
33	GOP1	O	34	GOP0	O

Figure 45. 16-Pin Assignments for the VESA/LPB Connector - J34

Pin	Signal	I/O	Pin	Signal	I/O
1	PCIRST#	0	2	GROUND	N/A
3	MIRQ1	I	4	GROUND	N/A
5	NC	N/A	6	GROUND2	N/A
7	NC	N/A	8	NC	N/A
9	NC	N/A	10	+5 V	N/A
11	+5 V	N/A	12	NC	N/A
13	+12 V	N/A	14	+5 V	N/A
15	NC	N/A	16	NC	N/A

Monitor Connector

Figure 46. 15-Pin Assignments for the Monitor Connector

Pin	Signal	I/O	Pin	Signal	I/O
1	Red	O	2	Green	O
3	Blue	O	4	Not used	I
5	Ground	N/A	6	Red ground	N/A
7	Green ground	N/A	8	Blue ground	N/A
9	+5 V, used by DDC2B	N/A	10	Ground	N/A
11	Not used	I	12	DDC2B serial data	I/O
13	Horizontal sync	O	14	Vertical sync	O
15	DDC2B clock	O			

Diskette Drive Connector

Figure 47. 34-Pin Assignments for the Diskette Drive Connector

Pin	Signal	Pin	Signal
1	Reserved	2	High density select
3	Not connected	4	Not connected
5	Ground	6	Data rate 0
7	Ground	8	Index#
9	Reserved	10	Motor enable 0
11	Ground	12	Drive select 1
13	Ground	14	Drive select 0
15	Ground	16	Motor enable 1
17	MSEN1	18	Direction in#
19	Ground	20	Step#
21	Ground	22	Write data#
23	Ground	24	Write enable#
25	Ground	26	Track0#
27	MSEN0	28	Write protect#
29	Ground	30	Read data#
31	Ground	32	Head 1 select#
33	Data rate 1	34	Diskette change#

Serial Port Connector

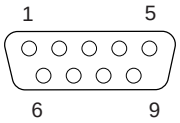


Figure 48. 9-Pin Assignments for the Serial Port Connector

Pin	Signal	I/O	Pin	Signal	I/O
1	Data carrier detect	I	2	Receive data#	I
3	Transmit data#	O	4	Data terminal read	O
5	Ground	NA	6	Data set ready	I
7	Request to send	O	8	Clear to send	I
9	Ring indicator	I			

Parallel Port Connector

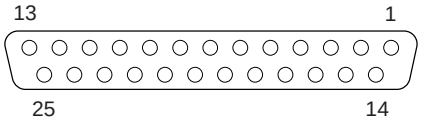


Figure 49. 25-Pin Assignments for the Parallel Port Connector

Pin	Signal	I/O	Pin	Signal	I/O
1	STROBE#	I/O	2	Data bit 0	I/O
3	Data bit 1	I/O	4	Data bit 2	I/O
5	Data bit 3	I/O	6	Data bit 4	I/O
7	Data bit 5	I/O	8	Data bit 6	I/O
9	Data bit 7	I/O	10	ACK#	I
11	BUSY	I	12	PE	I
13	SLCT	I	14	AUTO FD XT#	O
15	ERROR#	I	16	INIT#	O
17	SLCT IN#	O	18	Ground	N/A
19	Ground	N/A	20	Ground	N/A
21	Ground	N/A	22	Ground	N/A
23	Ground	N/A	24	Ground	N/A
25	Ground	N/A			

Keyboard and Mouse Port Connectors

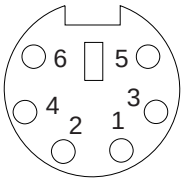


Figure 50. 6-Pin Assignments for the Keyboard Connector

Pin	Signal	I/O	Pin	Signal	I/O
1	Data	I/O	2	Aux data	I/O
3	Ground	NA	4	+5 V dc	NA
5	Clock	I/O	6	Aux clock	I/O

Figure 51. 6-Pin Assignments for the Mouse Connector

Pin	Signal	I/O	Pin	Signal	I/O
1	Data	I/O	2	Reserved	N/A
3	Ground	N/A	4	+5 V dc	N/A
5	Clock	I/O	6	Reserved	N/A

Infrared Port Connector

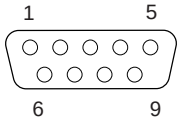


Figure 52. 9-Pin Assignments for the Infrared Connector

Pin	Signal	Pin	Signal
1	IR transmitted data (output)	2	Ground
3	Reserved	4	IR module select 2
5	IR module select 1	6	IR received data (input)
7	Voltage (5 V)	8	IR module select 0
9	No connect		

ISA Connectors

Note: The ISA connectors are part of the riser card.

Figure 53 (Page 1 of 2). 98-Pin Assignments for the ISA Connector

Pin	Signal	Pin	Signal
1 B	GROUND	1 A	IOCHCK#
2 B	RESET DRV	2 A	SD7
3 B	+5 V dc	3 A	SD6
4 B	IRQ2	4 A	SD5
5 B	-5 V dc	5 A	SD4
6 B	DRQ2	6 A	SD3
7 B	-12 V dc	7 A	SD2
8 B	OWS#	8 A	SD1
9 B	+12 V dc	9 A	SD0
10 B	GROUND	10 A	IOCHRDY
11 B	SMEMW#	11 A	AEN
12 B	SMEMR#	12 A	SA19
13 B	IOW#	13 A	SA18
14 B	IOR#	14 A	SA17
15 B	DACK3#	15 A	SA16
16 B	DRQ3	16 A	SA15
17 B	DACK1#	17 A	SA14
18 B	DRQ1	18 A	SA13
19 B	REFRESH#	19 A	SA12
20 B	CLK	20 A	SA11
21 B	IRQ7	21 A	SA10
22 B	IRQ6	22 A	SA9
23 B	IRQ5	23 A	SA8
24 B	IRQ4	24 A	SA7
25 B	IRQ3	25 A	SA6
26 B	DACK2#	26 A	SA5
27 B	TC	27 A	SA4
28 B	BALE	28 A	SA3
29 B	+5 V dc	29 A	SA2
30 B	OSC	30 A	SA1
31 B	GROUND	31 A	SA0
1 D	MEMCS16#	1 C	SBHE#
2 D	IOCS16#	2 C	LA23
3 D	IRQ10	3 C	LA22
4 D	IRQ11	4 C	LA21
5 D	IRQ12	5 C	LA20
6 D	IRQ15	6 C	LA19
7 D	IRQ14	7 C	LA18

Figure 53 (Page 2 of 2). 98-Pin Assignments for the ISA Connector

Pin	Signal	Pin	Signal
8 D	DACK0#	8 C	LA17
9 D	DRQ0	9 C	MEMR#
10 D	DACK5#	10 C	MEMW#
11 D	DRQ5	11 C	SD8
12 D	DACK6#	12 C	SD9
13 D	DRQ6	13 C	SD10
14 D	DACK7#	14 C	SD11
15 D	DRQ7	15 C	SD12
16 D	+5 V dc	16 C	SD13
17 D	MASTER#	17 C	SD14
18 D	GROUND	18 C	SD15

PCI Connector

Note: The PCI connectors are part of the riser card.

Figure 54 (Page 1 of 2). 124-Pin Assignments for the PCI Connector

Pin	Signal	Pin	Signal
A1	TRST#	B1	–12 V dc
A2	+12 V dc	B2	TCK
A3	TMS	B3	Ground
A4	TDI	B4	TDO
A5	+5 V dc	B5	+5 V dc
A6	INTA#	B6	+5 V dc
A7	INTC#	B7	INTB#
A8	+5 V dc	B8	INTD#
A9	Reserved	B9	PRSNT1#
A10	+5 V dc (I/O)	B10	Reserved
A11	Reserved	B11	PRSNT2
A12	Ground	B12	Ground
A13	Ground	B13	Ground
A14	Reserved	B14	Reserved
A15	RST#	B15	Ground
A16	+5 V dc (I/O)	B16	CLK
A17	GNT#	B17	Ground
A18	Ground	B18	REQ#
A19	Reserved	B19	+5 V dc (I/O)
A20	Address/Data 30	B20	Address/Data 31
A21	+3.3 V dc	B21	Address/Data 29
A22	Address/Data 28	B22	Ground
A23	Address/Data 26	B23	Address/Data 27
A24	Ground	B24	Address/Data 25
A25	Address/Data 24	B25	+3.3 V dc

Figure 54 (Page 2 of 2). 124-Pin Assignments for the PCI Connector

Pin	Signal	Pin	Signal
A26	IDSEL	B26	C/BE 3#
A27	+3.3 V dc	B27	Address/Data 23
A28	Address/Data 22	B28	Ground
A29	Address/Data 20	B29	Address/Data 21
A30	Ground	B30	Address/Data 19
A31	Address/Data 18	B31	+3.3 V dc
A32	Address/Data 16	B32	Address/Data 17
A33	+3.3 V dc	B33	C/BE 2#
A34	FRAME#	B34	Ground
A35	Ground	B35	IRDY#
A36	TRDY#	B36	+3.3 V dc
A37	Ground	B37	DEVSEL#
A38	STOP#	B38	Ground
A39	+3.3 V dc	B39	LOCK#
A40	SDONE	B40	PERR#
A41	SBO#	B41	+3.3 V dc
A42	Ground	B42	SERR#
A43	PAR	B43	+3.3 V dc
A44	C/BE(1)#	B44	C/BE 1#
A45	Address/Data 14	B45	Address/Data 14
A46	Ground	B46	Ground
A47	Address/Data 12	B47	Address/Data 12
A48	Address/Data 10	B48	Address/Data 10
A49	Ground	B49	Ground
A50	Key	B50	Key
A51	Key	B51	Key
A52	Address/Data 8	B52	Address/Data 8
A53	Address/Data 7	B53	Address/Data 7
A54	+3.3 V dc	B54	+3.3 V dc
A55	Address/Data 5	B55	Address/Data 5
A56	Address/Data 3	B56	Address/Data 3
A57	Ground	B57	Ground
A58	Address/Data 1	B58	Address/Data 1
A59	+5 V dc (I/O)	B59	+5 V dc (I/O)
A60	ACK64#	B60	ACK64#
A61	+5 V dc	B61	+5 V dc
A62	+5 V dc	B62	+5 V dc

Power Supply Connectors

Figure 55. Pin Assignments for Power Supply Connectors

Connector	Location	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6
P1	System Board	PWRGOOD	+5 V	+12 V	-12 V	GND	GND
P2	System Board	GND	GND	-5 V	+5 V	+5 V	+5 V
P3	3.5" Diskette Drive	+5 V	GND	GND	+12 V	–	–
P4	–	+12 V	GND	GND	+5 V	–	–
P5	DASD	+12 V	GND	GND	+5 V	–	–
P6 [1]	DASD	+12 V	GND	GND	+5 V	–	–
P7 [1]	DASD	+12 V	GND	GND	+5 V	–	–
P8 [1]	DASD	+12 V	GND	GND	+5 V	–	–
P9 [2]	System Board	+5 V	CONTROL	GND	–	–	–
P10	Riser 3 V	+3.3 V	+3.3 V	+3.3 V	GND	GND	GND
P11	System Board 3 V	+3.3 V	+3.3 V	+3.3 V	GND	GND	GND
P12	LAN	+5 V	CONTROL	GND	–	–	–

Voltage Regulator Module Connector

Figure 56 (Page 1 of 2). 15-Pin Assignments for the VRM Connector

Pin	Row A	Row B	Pin
1	V_{SS}	V_{SS}	1
2	V_{SS}	V_{SS}	2
3	ND	V_{IO}	3
4	V_{IO}	V_{IO}	4
5	+3.3 V	+3.3 V	5
6	+3.3 V	+3.3 V	6
7	V_{CORE}	V_{CORE}	7
8	V_{CORE}	V_{CORE}	8
9	V_{SS}	V_{CORE}	9
10	V_{CORE}	V_{CORE}	10
11	Power Good	UPVRM#	11
12	Sense	Disable	12
13	V_{SS}	V_{SS}	13

1 Connectors provided only with the 200W power supply.

2 AUX 5

Figure 56 (Page 2 of 2). 15-Pin Assignments for the VRM Connector

Pin	Row A	Row B	Pin
14	+5.0 V	+5.0 V	14
15	+5.0 V	+5.0 V	15

Appendix B. System Address Maps

System Memory Map

The first 640 KB of system board RAM is mapped starting at address 0000000h. A 256-byte area and a 1 KB area of this RAM are reserved for BIOS data areas. Memory can be mapped differently if POST detects an error.

Figure 57. System Memory Map

Address Range (hex)	Size	Description
00000000–0007FFFF	512 KB	Conventional
00080000–0009FBFF	127 KB	Extended conventional
0009FC00–0009FFFF	1 KB	Extended BIOS data
000A0000–000BFFFF	128 KB	S3 Trio64V+
000C0000–000C7FFF	32 KB	S3 Trio64V+ ROM BIOS (shadowed)
000D8000–000DFFFF	96 KB	ISA/PCI space; available to ISA adapter ROMs
000E0000–000FFFFF	128 KB	System ROM BIOS (ISA bus, shadowed)
00100000–00FFFFFF	15 MB	ISA/PCI space
01000000–39FFFFFF	912 MB	PCI space
40000000–43FFFFFF	64 MB	S3 Trio64V+ linear frame buffer
44000000–FFFDFFFF	3154 MB	PCI space
FFFE0000–FFFFFFFF	128 KB	System ROM BIOS (ISA bus)

Input/Output Address Map

The following figure lists resource assignments for the I/O address map. Any addresses that are not shown are reserved.

Figure 58 (Page 1 of 3). I/O Address Map

Address (Hex)	Device
0000–001F	DMA 1
0020–003F	Interrupt controller 1
0040–0043	Timer 1
0044–0047	Available I/O for ISA/PCI bus
0048–0049	Power Management
004A–005F	Available I/O for ISA/PCI bus
0060	Keyboard controller data byte
0061	System Port B
0062–0063	Available I/O for ISA/PCI bus
0064	Keyboard controller, command and status byte
0065–006F	Available I/O for ISA/PCI bus
0070, bit 7	Enable/disable NMI
0070, bits 6:0	Real time clock address
0071	Real time clock data

Figure 58 (Page 2 of 3). I/O Address Map

Address (Hex)	Device
0072–0076	Available I/O for ISA/PCI bus
0077	Reserved
0078	GPIO CPU speed detect
0079	National 87306 GPIO
007A-007B	Available to ISA bus
007C–007F	L2 Cache ID, SMI/PCI IRQ enable
0080	POST Checkpoint register
0080-008F	DMA page register
0090–009F	Available I/O for ISA/PCI bus
00A0–00B1	Interrupt controller 2
00B2–00B3	Power management
00B4–00BF	Interrupt controller 2
00C0–00DF	DMA 2
00E0–00EF	Available I/O for ISA/PCI bus
00F0	Coprocessor busy–Clear
00F1	Coprocessor reset
00F2–00FF	Available I/O for ISA/PCI bus
0100–016F	Available I/O for ISA/PCI bus
0170–0177	IDE channel 1
01F0–01F7	IDE channel 0
01F8–021F	Available I/O for ISA/PCI bus
0220–0227	National 87306, serial port 3 or 4
0228–0277	Available I/O for ISA/PCI bus
0278–027F	National 87306, parallel port 3
0280–02E7	Available I/O for ISA/PCI bus
02E8–02EF	National 87306, serial port 3 or 4
02F0–02F7	Available I/O for ISA/PCI bus
02F8–02FF	National 87306, serial port 2
0300–0337	Available I/O for ISA/PCI bus
0338–033F	National 87306, serial port 3 or 4
0340–0373	Available I/O for ISA/PCI bus
0374–0377	IDE channel 1
0377, bit 7	IDE, diskette change
0378–037F	National 87306, parallel port 2
03B4–03B5	S3 Trio64V+
03BA	S3 Trio64V+
03BC–03BE	National 87306, parallel port 1 (system board)
03C0–03CA	S3 Trio64V+
03CC	S3 Trio64V+
03CE–03CF	S3 Trio64V+
03D4–03D5	S3 Trio64V+
03DA	S3 Trio64V+
03E8–03EF	National 87306, serial port 3 or 4

Figure 58 (Page 3 of 3). I/O Address Map

Address (Hex)	Device
03F0–03F5	National 87306, diskette channel 0
03F6	IDE channel 0
03F7, bit 7	IDE, diskette change
03F7, bits 6:0	IDE channel 0
03F8–03FF	National 87306, serial port 1 (system board)
0400–04CF	Available I/O for ISA/PCI bus
04D0–04D1	Interrupt control level
04D2–0CF7	Available I/O for ISA/PCI bus
0530–0537	Available I/O for ISA/PCI bus
0CF8–0CFB	PCI configuration address register
0CFC–0CFF	PCI configuration data registers
42E8–42E9	S3 Trio64V+
4AE8–4AE9	S3 Trio64V+
8180–81A3	S3 Trio64V+
81C0–81FF	S3 Trio64V+
82E8–82EB	S3 Trio64V+
86E8–86EB	S3 Trio64V+
8AE8–8AEB	S3 Trio64V+
8EE8–8EEB	S3 Trio64V+
92E8–92EB	S3 Trio64V+
96E8–96EB	S3 Trio64V+
9AE8–9AEB	S3 Trio64V+
9EE8–9EE9	S3 Trio64V+
A2E8–A2EB	S3 Trio64V+
A6E8–A6EB	S3 Trio64V+
AAE8–AAEB	S3 Trio64V+
B2E8–B2EB	S3 Trio64V+
B6E8–B6E9	S3 Trio64V+
BAE8–BAE9	S3 Trio64V+
BEE8–BEE9	S3 Trio64V+
E2E8–E2EB	S3 Trio64V+
EAE8–EAE9	S3 Trio64V+
FF00–FF37	S3 Trio64V+
FF40–FF5F	S3 Trio64V+

DMA I/O Address Map

The following figure lists resource assignments for the DMA address map. Any addresses that are not shown are reserved.

Figure 59 (Page 1 of 2). DMA I/O Addresses

Address (Hex)	Description	Bits	Byte Pointer
0000	Channel 0, Memory Address register	00–15	Yes
0001	Channel 0, Transfer Count register	00–15	Yes
0002	Channel 1, Memory Address register	00–15	Yes
0003	Channel 1, Transfer Count register	00–15	Yes
0004	Channel 2, Memory Address register	00–15	Yes
0005	Channel 2, Transfer Count register	00–15	Yes
0006	Channel 3, Memory Address register	00–15	Yes
0007	Channel 3, Transfer Count register	00–15	Yes
0008	Channels 0–3, Read Status/Write Command register	00–07	
0009	Channels 0–3, Write Request register	00–02	
000A	Channels 0–3, Write Single Mask register bits	00–02	
000B	Channels 0–3, Mode register (write)	00–07	
000C	Channels 0–3, Clear byte pointer (write)	N/A	
000D	Channels 0–3, Master clear (write)/temp (read)	00–07	
000E	Channels 0–3, Clear Mask register (write)	00–03	
000F	Channels 0–3, Write All Mask register bits	00–03	
0081	Channel 2, Page Table Address register [3]	00–07	
0082	Channel 3, Page Table Address register [3]	00–07	
0083	Channel 1, Page Table Address register [3]	00–07	
0087	Channel 0, Page Table Address register [3]	00–07	
0089	Channel 6, Page Table Address register [3]	00–07	
008A	Channel 7, Page Table Address register [3]	00–07	
008B	Channel 5, Page Table Address register [3]	00–07	
008F	Channel 4, Page Table Address/Refresh register	00–07	
00C0	Channel 4, Memory Address register	00–15	Yes
00C2	Channel 4, Transfer Count register	00–15	Yes
00C4	Channel 5, Memory Address register	00–15	Yes
00C6	Channel 5, Transfer Count register	00–15	Yes
00C8	Channel 6, Memory Address register	00–15	Yes
00CA	Channel 6, Transfer Count register	00–15	Yes
00CC	Channel 7, Memory Address register	00–15	Yes
00CE	Channel 7, Transfer Count register	00–15	Yes
00D0	Channels 4–7, Read Status/Write Command register	00–07	
00D2	Channels 4–7, Write Request register	00–02	
00D4	Channels 4–7, Write Single Mask register bit	00–02	
00D6	Channels 4–7, Mode register (write)	00–07	
00D8	Channels 4–7, Clear byte pointer (write)	N/A	
00DA	Channels 4–7, Master clear (write)/temp (read)	00–07	

Figure 59 (Page 2 of 2). DMA I/O Addresses

Address (Hex)	Description	Bits	Byte Pointer
00DC	Channels 4–7, Clear Mask register (write)	00–03	
00DE	Channels 4–7, Write All Mask register bits	00–03	
00DF	Channels 5–7, 8- or 16-bit mode select	00–07	

[3] Upper byte of memory address register.

Appendix C. IRQ and DMA Channel Assignments

The following figures list the interrupt request (IRQ) and direct memory access (DMA) channel assignments.

Figure 60. IRQ Channel Assignments

IRQ	System Resource
NMI	Critical system error
SMI	System/power management interrupt
0	Reserved (internal timer)
1	Reserved (keyboard)
2	Reserved (cascade interrupt from slave)
3	Serial port 2 [4]
4	Serial port 1 [4]
5	Parallel port 2 [4]
6	Diskette controller [4]
7	Parallel port 1 [4]
8	Reserved (real-time clock)
9	Video adapter [4]
10	ISA/PCI bus
11	ISA/PCI bus
12	Mouse port [4]
13	Reserved (math coprocessor)
14	IDE Channel 1 [4]
15	IDE Channel 2 [4]

Figure 61. DMA Channel Assignments

DMA Channel	Data Width	System Resource
0	ISA bus	8 bits
1	ISA bus	8 bits
2	Reserved (diskette drive)	8 bits
3	ECP parallel port [5]	8 bits
4	Reserved (cascade channel)	–
5	ISA bus	16 bits
6	ISA bus	16 bits
7	ISA bus	16 bits

[4] If not assigned, this resource is available for the ISA/PCI bus.

[5] If not assigned, this resource is available for the ISA bus.

Appendix D. Error Codes

The following figures list the POST error codes and beep error codes for the computer.

POST Error Codes

POST error messages appear when POST finds problems with the hardware during power-on or when a change in the hardware configuration is found. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages. An *x* in an error message can represent any number.

Figure 62 (Page 1 of 2). POST Error Codes

Code	Description
101	Interrupt failure
102	Timer failure
103	Timer-interrupt failure
104	protected mode failure
105	last 8042 command not accepted –keyboard failure
106	System board failure
108	Timer bus failure
109	low MB chip select test
110	System board parity error 1 (system board parity latch set)
111	I/O parity error 2 (I/O channel check latch set)
112	I/O channel check error
113	I/O channel check error
114	external ROM checksum error
115	DMA error
116	System board port read/write error
120	Microprocessor test error
121	Hardware error
151	Real time clock failure
161	Bad CMOS Battery
162	CMOS RAM checksum/configuration error
163	Clock not updating
164	CMOS RAM memory size does not match
167	Clock not updating
175	Riser card or system board error
176	System cover has been removed
177	Corrupted administrator password
178	Riser card or system board error
183	Administrator password has been set and must be entered
184	Password removed due to checksum error
185	Corrupted boot sequence
186	System board or hardware security error
189	More than three password attempts were made to access system
201	Memory date error

Figure 62 (Page 2 of 2). POST Error Codes

Code	Description
202	Memory address line error 00-15
203	Memory address line error 16-23
221	ROM to RAM remapping error
225	Unsupported memory type installed or memory pair mismatch
301	Keyboard error
302	Keyboard error
303	Keyboard to system board interface error
304	Keyboard clock high
305	No keyboard +5 V
601	Diskette drive or controller error
602	Diskette IPL boot record not valid
604	Unsupported diskette drive installed
605	POST cannot unlock diskette drive
662	Diskette drive configuration error
762	Math coprocessor configuration error
11xx	Serial port error (xx = serial port number)
1762	Hard disk configuration error
1780	Hard disk 0 failed
1781	Hard disk 1 failed
1782	Hard disk 2 failed
1783	Hard disk 3 failed
1800	PCI adapter has requested an unavailable hardware interrupt
1801	PCI adapter has requested an unavailable memory resource
1802	PCI adapter has requested an unavailable I/O address space, or a defective adapter
1803	PCI adapter has requested an unavailable memory address space, or a defective adapter
1804	PCI adapter has requested unavailable memory addresses
1805	PCI adapter ROM error
1962	Boot sequence error
2401	System board video error
8601	System board - keyboard/pointing device error
8602	Pointing device error
8603	Pointing device or system board error
12092	Level 1 cache error (Processor chip)
12094	Level 2 cache error
16101	Riser card battery is dead
I9990301	Hard disk failure
I9990305	No operating system found

Beep Codes

For the following beep codes, the numbers indicate the sequence and number of beeps. For example, a "2-3-2" error symptom (a burst of two beeps, three beeps, then a burst of two beeps) indicates a memory module problem.

Figure 63. Beep Codes

Beep Code	Probable Cause
1-1-3	CMOS write/read failure
1-1-4	BIOS ROM checksum failure
1-2-1	Programmable interval timer test failure
1-2-2	DMA initialization failure
1-2-3	DAM page register write/read test failure
1-2-4	RAM refresh verification failure
1-3-1	1st 64 K RAM test failure
1-3-2	1st 64 K RAM parity test failure
2-1-1	Slave DMA register test in progress or failure
2-1-2	Master DMA register test in progress or failure
2-1-3	Master interrupt mask register test failure
2-1-4	Slave interrupt mask register test failure
2-2-2	Keyboard controller test failure
2-3-2	Screen memory test in progress or failure
2-3-3	Screen retrace tests in progress or failure
3-1-1	Timer tick interrupt test failure
3-1-2	Interval timer channel 2 test failure
3-1-4	Time-of-Day clock test failure
3-2-4	Comparing CMOS memory size against actual
3-3-1	Memory size mismatch occurred

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Part Number: 78H5083

Printed in U.S.A.